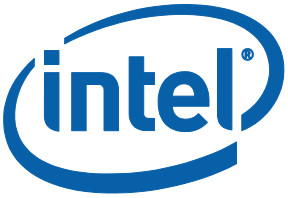

Titan Ridge DD
Thunderbolt Interface Controller

Datasheet

Revision 1.41
December 2018

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Revision History

Date	Revision	Description
August 21, 2016	0.65	Initial Titan Ridge DD Release
December 12, 2016	0.75	Update of Flash Memory Updates in Programming Interface Insertion of Electrical Specifications Chapter Insertion of Power Up and Wake Flows Chapter Insertion of In-line Functionality Chapter Insertion of Appendices
December 14, 2016	0.76	Updates in Programming Interface
April 20, 2017	0.8	Updates in Electrical Specifications
May 25th, 2017	0.82	Updates in Programming Interface Updates in Inline Functionality
May 29th, 2017	0.83	Updates in Programming Interface
June 27th, 2017	0.84	Updates in Programming Interface Updates in Mechanical Specifications Updates in Pin Interface
August 17th, 2017	0.85	Updates in Pin Interface Updates in Inline Functionality
October 31st, 2017	0.86	Updates in Electrical Specifications (Power Values)
December 12th, 2017	0.87	Updates in Electrical Specifications (Power Values)
February 5th, 2018	1.0	Updates in the supported types of flash memory Updates in the CIO Phy NVM configuration section Addition of the DP Phy NVM configuration section
October 8th, 2018	1.1	Updates in Programming Interface (Capability registers) Updates in Electrical Specifications (addition of the Trace Length Design Considerations section) Updates in Flash Memory (supported types) Updates in Testability (additions to the Thermal Diode section) Updates in Electrical Specifications (SVR parameters)

Date	Revision	Description
November 19th, 2018	1.2	Updates in Inline Functionality (Display Port Phy Eye Monitor and CIO Eye Monitor activation flow) Updates in Flash Memory (supported types) Updates in Electrical Specifications (Internal Voltage Regulator specifications and Recommended Operating Conditions)
December 12th, 2018	1.3	Updates in Flash Memory (supported types) Updates in the Introduction (Router Chip Specifications)
December 18th, 2018	1.41	Updates in Power Up and Wake Flows (Host S5 Handling)

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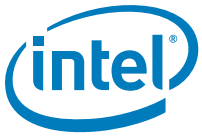

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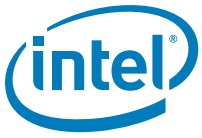

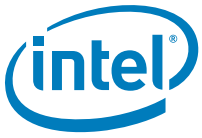

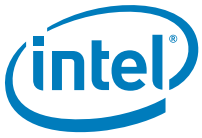

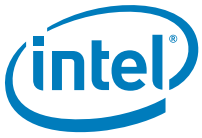

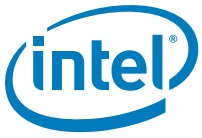

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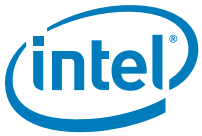


1.0 Introduction

The Titan Ridge DD is a Thunderbolt controller (see block diagram in Figure 1) that acts as a point of entry or a point of exit in the Thunderbolt domain. The Thunderbolt domain is built as a daisy chain of Thunderbolt enabled products for the encapsulated protocols - PCIe and DisplayPort. These protocols are encapsulated into the Thunderbolt fabric and can be tunneled across the Thunderbolt domain. The Titan Ridge DD Thunderbolt controller also acts as a flexible re-timer for DP protocol, or a re-timer for USB3.1.

Titan Ridge DD can be implemented in various devices such as storage, docks, displays, home entertainment, cameras, computer peripherals, high end video editing systems, and any other PCIe based device that can be used to extend system capabilities outside of the system's box.

Titan Ridge DD Thunderbolt connection data rate is 20Gbps per lane and is compatible with Thunderbolt 3 specification enabling Thunderbolt link at up to 2x20Gbps, as well as backward compatible with Thunderbolt 1 (10Gbps) and Thunderbolt 2 (2x10Gbps) specifications.

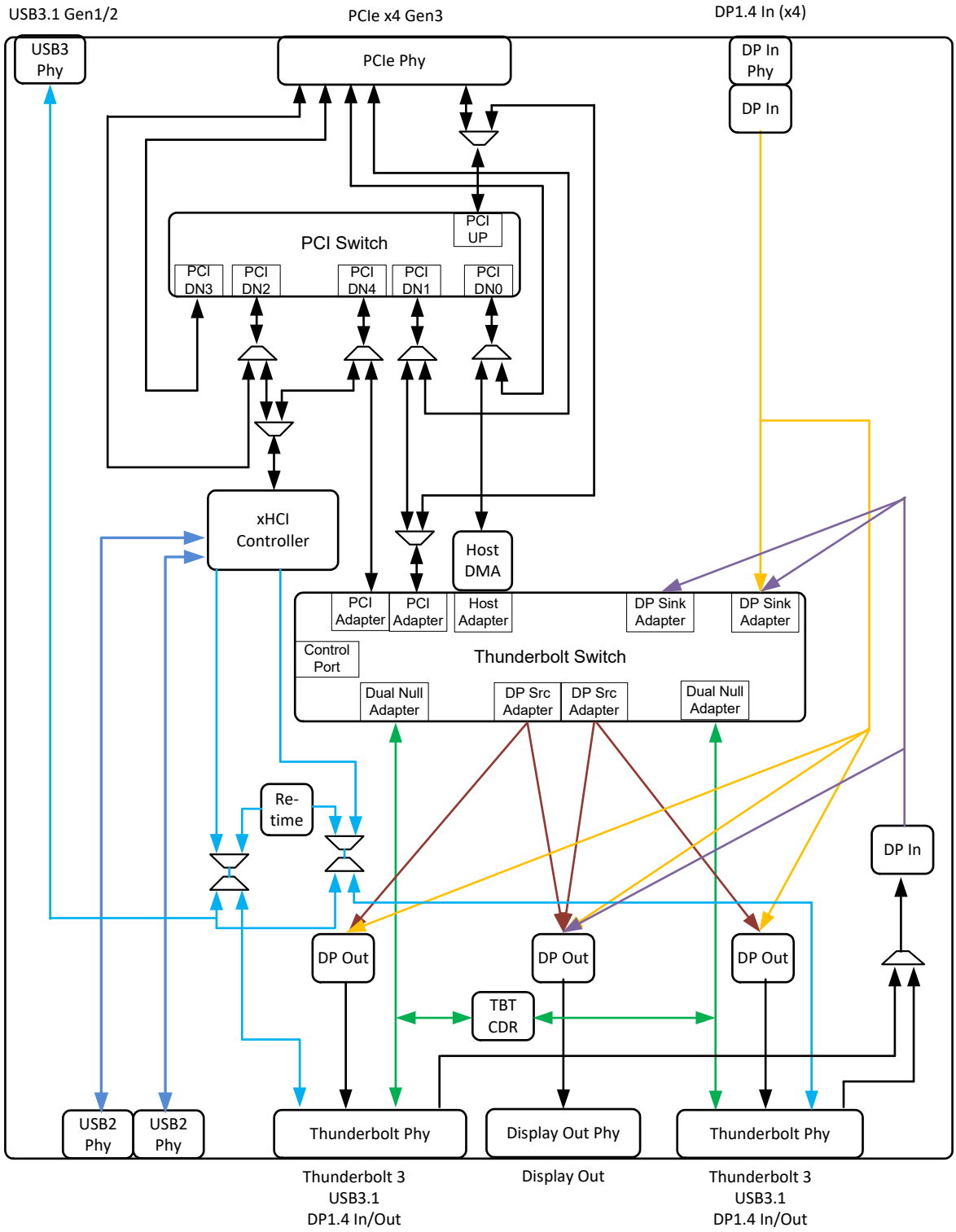
Titan Ridge DD supports the following standard protocol IOs:

- PCIe Gen3
- DisplayPort (DP) 1.4a
- USB 3.1
- USB 2.0
- SPI
- JTAG
- I2C

Titan Ridge DD port connectivity is through USB-C connector supporting the following modes:

Connection Type	Mode	USB-C Port Details
USB	Native	Single SSP/SS + Single HS/FS/LS USB connection
Thunderbolt	Alternate	Dual Thunderbolt lanes running at 10Gpbs/20Gbps
Display Port	Alternate	x1/x2/x4 Display Port lanes running at 1.62Gbps/ 2.7Gbps/5.4Gbps/8.1Gbps signaling rate
MultiFunction DP	Alternate	Single SSP/SS + Single HS/FS/LS USB connection + x2 Display Port lanes running at 1.62Gbps/2.7Gbps/5.4Gbps/ 8.1Gbps signaling rate

Figure 1. Titan Ridge DD Controller Block Diagram



1.1 Router Chip Specifications

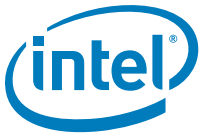
Titan Ridge DD implements the following interfaces:

- 1 DisplayPort sink interface connected on board or through a cable compliant with:
  - The DisplayPort 1.4a specification for tunneling:
    - —1.62 Gbps or 2.7 Gbps or 5.4 Gbps or 8.1 Gbps signaling rate
    - —x1, x2 or x4 lane operation
  - The DisplayPort 1.4a specification:
    - —1.62 Gbps or 2.7 Gbps or 5.4Gbps or 8.1 Gbps signaling rate
    - —x1, x2 or x4 lane operation
    - —Support for DSC compression
    - —LTTPR
- 4 lane PCI Express interface
  - PCI Express 3.0 compliant @ 8.0 GT/s
  - In Device mode, interface can be configured to one of the following:
    - —1x4 - One Device of four lanes
    - —4x1 - Four Devices of one lane each
    - —2x2 - Two devices of two lanes each
    - —1x2 + 2x1 - One device of two lanes and two devices of one lane each
  - Each separate link can be Gen3 or Gen2 or Gen1
- 2 USB-C connectors, each one supports either:
  - Thunderbolt alternate mode -2x2 CIO channels:
    - —20 paths per port target
    - —Each port streams x2 SERDES with 20.625/20.0 Gbps or 10.3125/10.0 Gbps signaling rate
    - —16 counters per port

    OR
  - Display Port alternate mode
    - —1.62 Gbps or 2.7 Gbps or 5.4 Gbps or 8.1 Gbps signaling rate

    OR
  - USB3.1 Gen1/Gen2 channel and USB2 channel
    - —high speed channel can operate at USB3.1 Gen1 (SS) or Gen2 (SSP)
    - —low speed channel can operate at USB HS, FS, LS

    OR
  - 1 Multi function DP alternate mode
- 1 USB3.1 Gen1/Gen2 channel
  - —Each high speed channel can operate at USB3.1 Gen1 (SS) or Gen2 (SSP)
- CIO Host Interface:
  - PCI Express 3.0 compliant endpoint
  - Supports simultaneous transmit and receive on 12 paths



  - Raw mode and frame mode operation configurable on a per-path basis
  - MSI and MSI-X support
  - Interrupt moderation support
- CIO Time Management Unit (TMU):
  - Router implements a time synchronization protocol based on 802.1AS
  - Time accuracy between adjacent routers: 8ns
  - Hardware support in the form of an input pin to enable the TMU to be slaved to an external Grand Master clock
  - Hardware support in the form of an output pin to enable the TMU clock to provide time reference to an external device
- 3.3V supply
  - Internal SVR and control for power domains

2.0 Pin Interface

Signal names are subject to change without notice. Verify with your local Intel sales office that you have the latest information before finalizing a design.

2.1 Signal Description

2.1.1 Signal Type Definitions

The signals are electrically defined in Table 1

Table 1. Signal Definitions

Name	Definition
In	Input Pin
Out	Output Pin
I/O	Bi-directional Input / Output Pin
OD O	Open Drain Output Pin
I/OD	Bi-directional Input/Open Drain Output Pin
A-in	Analog input signals
A-out	Analog output signals
A-inout	Bi-directional analog signals
LC	Link Controller power domain
POC	Power on Control power domain
ANA	Analog common power domain
PCIe	PCIe power domain
DP	Display Port power domain
USB	USB power domain

2.1.2 PCIe Interface

Table 2. PCIe Signal and Pin Information

Signal	Pin Number	Type	Power domain	Description
PCIE_RX3_N	H22	A-in		PCIe Receiver Differential Pair Lane 3
PCIE_RX3_P	H23	A-in		PCIe Receiver Differential Pair Lane 3
PCIE_RX2_N	M22	A-in		PCIe Receiver Differential Pair Lane 2
PCIE_RX2_P	M23	A-in		PCIe Receiver Differential Pair Lane 2
PCIE_RX1_N	T22	A-in		PCIe Receiver Differential Pair Lane 1
PCIE_RX1_P	T23	A-in		PCIe Receiver Differential Pair Lane 1
PCIE_RX0_N	Y22	A-in		PCIe Receiver Differential Pair Lane 0
PCIE_RX0_P	Y23	A-in		PCIe Receiver Differential Pair Lane 0

Signal	Pin Number	Type	Power domain	Description
PCIE_TX3_N	F22	A-out		PCIe Transmitter Differential Pair Lane 3
PCIE_TX3_P	F23	A-out		PCIe Transmitter Differential Pair Lane 3
PCIE_TX2_N	K22	A-out		PCIe Transmitter Differential Pair Lane 2
PCIE_TX2_P	K23	A-out		PCIe Transmitter Differential Pair Lane 2
PCIE_TX1_N	P22	A-out		PCIe Transmitter Differential Pair Lane 1
PCIE_TX1_P	P23	A-out		PCIe Transmitter Differential Pair Lane 1
PCIE_TX0_N	V22	A-out		PCIe Transmitter Differential Pair Lane 0
PCIE_TX0_P	V23	A-out		PCIe Transmitter Differential Pair Lane 0

2.1.3 Thunderbolt Ports

Table 3. Thunderbolt Ports Signal and Pin Information

Signal	Pin Number	Type	Power domain	Description
ASSRXn1	A21	A-inout		High speed serial lane
ASSRXp1	B21	A-inout		High speed serial lane
ASSRXn2	B15	A-inout		High speed serial lane
ASSRXp2	A15	A-inout		High speed serial lane
ASSTXn1	B19	A-inout		High speed serial lane
ASSTXp1	A19	A-inout		High speed serial lane
ASSTXn2	B17	A-inout		High speed serial lane
ASSTXp2	A17	A-inout		High speed serial lane
ASBU1	H4	A-inout		Port A SBU signaling
ASBU2	J4	A-inout		Port A SBU signaling
BSSRXn1	B13	A-inout		High speed serial lane
BSSRXp1	A13	A-inout		High speed serial lane
BSSRXn2	A7	A-inout		High speed serial lane
BSSRXp2	B7	A-inout		High speed serial lane
BSSTXn1	B11	A-inout		High speed serial lane
BSSTXp1	A11	A-inout		High speed serial lane
BSSTXn2	B9	A-inout		High speed serial lane
BSSTXp2	A9	A-inout		High speed serial lane
BSBU1	L4	A-inout		Port B SBU signaling
BSBU2	L5	A-inout		Port B SBU signaling

Note: For Display Port Type-C pin assignment mapping, see Section 8.14

2.1.4 Display Port

Table 4. Display Port Signal and Pin Information

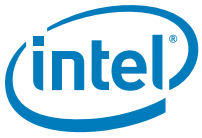
Signal	Pin Number	Type	Power domain	Description
DPSNK1_ML3_N	AC13	A-in		DP Sink 1 Main Link Receiver Differential Pair Lane 3
DPSNK1_ML3_P	AB13	A-in		DP Sink 1 Main Link Receiver Differential Pair Lane 3
DPSNK1_ML2_N	AB11	A-in		DP Sink 1 Main Link Receiver Differential Pair Lane 2

Signal	Pin Number	Type	Power domain	Description
DPSNK1_ML2_P	AC11	A-in		DP Sink 1 Main Link Receiver Differential Pair Lane 2
DPSNK1_ML1_N	AC9	A-in		DP Sink 1 Main Link Receiver Differential Pair Lane 1
DPSNK1_ML1_P	AB9	A-in		DP Sink 1 Main Link Receiver Differential Pair Lane 1
DPSNK1_ML0_N	AB7	A-in		DP Sink 1 Main Link Receiver Differential Pair Lane 0
DPSNK1_ML0_P	AC7	A-in		DP Sink 1 Main Link Receiver Differential Pair Lane 0
NC_E1	E1	A-in		This pin is not connected
NC_E2	E2	A-in		This pin is not connected
NC_C1	C1	A-in		This pin is not connected
NC_C2	C2	A-in		This pin is not connected
NC_A3	A3	A-in		This pin is not connected
NC_B3	B3	A-in		This pin is not connected
NC_B5	B5	A-in		This pin is not connected
NC_A5	A5	A-in		This pin is not connected
NC_P1	P1	A-inout		This pin is not connected
NC_P2	P2	A-inout		This pin is not connected
DPSNK1_AUX_N	N2	A-inout		DP Sink 1 Aux Channel Differential Pair
DPSNK1_AUX_P	N1	A-inout		DP Sink 1 Aux Channel Differential Pair
DPSRC_ML3_N	AB15	A-out		DP Source 0 Main Link transmitter Differential Pair Lane 3
DPSRC_ML3_P	AC15	A-out		DP Source 0 Main Link transmitter Differential Pair Lane 3
DPSRC_ML2_N	AC17	A-out		DP Source 0 Main Link transmitter Differential Pair Lane 2
DPSRC_ML2_P	AB17	A-out		DP Source 0 Main Link transmitter Differential Pair Lane 2
DPSRC_ML1_N	AB19	A-out		DP Source 0 Main Link transmitter Differential Pair Lane 1
DPSRC_ML1_P	AC19	A-out		DP Source 0 Main Link transmitter Differential Pair Lane 1
DPSRC_ML0_N	AC21	A-out		DP Source 0 Main Link transmitter Differential Pair Lane 0
DPSRC_ML0_P	AB21	A-out		DP Source 0 Main Link transmitter Differential Pair Lane 0
DPSRC_AUX_N	N5	A-inout		DP Source 0 Aux Chanel Differential Pair
DPSRC_AUX_P	N4	A-inout		DP Source 0 Aux Chanel Differential Pair

2.1.5 USB Interface

Table 5. USB Signal and Pin Information

Signal	Pin Number	Type	Power domain	Description
PA_USB2_D_N	D20	A-inout		Port A: USB2 Differential Pair
PA_USB2_D_P	E20	A-inout		Port A: USB2 Differential Pair
PB_USB2_D_N	D19	A-inout		Port B: USB2 Differential Pair
PB_USB2_D_P	E19	A-inout		Port B: USB2 Differential Pair
U0_SSRXn1	AB3	A-inout		USB port Differential Receiver



Signal	Pin Number	Type	Power domain	Description
U0_SSRXp1	AC3	A-inout		USB port Differential Receiver
U0_SSTXn1	AB5	A-inout		USB port Differential Receiver
U0_SSTXp1	AC5	A-inout		USB port Differential Receiver

2.1.6 JTAG Interface

Table 6. JTAG and TEST Signal and Pin Information

Signal	Pin Number	Type	Power domain	Description
TDI	W20	In	LC	JTAG Test Data Input
TMS	Y20	In	LC	JTAG Test Mode Select
TCK	W19	In	LC	JTAG Test Clock
TDO	Y19	OD O	LC	JTAG Test Data Output
TEST_EN	R4	In	POC	Test Enable (Connected to GND on func Board)
TEST_PWR_GOOD	W5	In	LC	Add an external 100 OHm to GND
USB2_ATEST	B23	A-out		Testability for US2B analog
PCIE_ATEST	AB23	A-out		Testability for PCIE analog
MONDC_SVR	D5	A-inout		Force/monitor options in the SVR analog

2.1.7 Flash Memory Interface

Table 7. Flash Memory Signal and Pin Information

Signal	Pin Number	Type	Power domain	Description
EE_DI	Y18	Out	LC	Data in to Flash device
EE_DO	W16	In	LC	Data out from FLASH device
EE_CS_N	W18	Out	LC	FLASH chip select
EE_CLK	Y16	Out	LC	FLASH clock

2.1.8 Clocks

Table 8. Clocks Signal and Pin Information

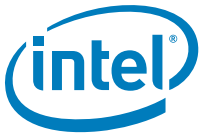
Signal	Pin Number	Type	Power domain	Description
PCIE_REFCLK_100_IN_N	T19	A-in		100 MHz Ref Clock for both CIO and PCIe sub-units
PCIE_REFCLK_100_IN_P	V19	A-in		100 MHz Ref Clock for both CIO and PCIe sub-units
XTAL_25_IN	D22	A-in		Input clock 25 MHz
XTAL_25_OUT	D23	A-inout		Output 25 MHz clock in XTal mode, Input in external differential clock mode

2.1.9 Miscellaneous

Table 9. Miscellaneous Signal and Pin Information

Signal	Pin Number	Type	Power domain	Description
I2C_SCL	V2	I/O	POC	i2c master clock

Signal	Pin Number	Type	Power domain	Description
I2C_SDA	V1	I/O	POC	i2c master data
POC_GPIO_2	V5	I/O	POC	usb_vbus_enable
FORCE_PWR	V4	I/O	POC	(input) force CIO and CIO EMEP on
WAKE_N	U2	I/O	POC	(input) - pcie wake_n
PM_S3_EN	U1	I/O	POC	(output) - s3 indication
POC_GPIO_6	T5	I/O	POC	General purpose I/O
POC_GPIO_7	T4	I/O	POC	General purpose I/O
PA_HPD	T2	I/O	POC	Port A HPD signaling
PB_HPD	T1	I/O	POC	Port B HPD signaling
DPSRC_HPD	R5	I/O	POC	Hot plug detect Input
PA_USB2_MXCTL	R2	I/O	POC	Port A/B external USB2 mux control
PB_USB2_MXCTL	R1	I/O	POC	Port A/B external USB2 mux control
GPIO_0	W1	I/O	LC	General purpose I/O
GPIO_1	W2	I/O	LC	General purpose I/O
EE_WP_N	W4	I/O	LC	(output) - flash write protect
TMU_CLKOUT	Y1	I/O	LC	(output) - tmu clock output
PM_S0_EN	Y2	I/O	LC	S0 enable indication
DEV_PERST_N	AA1	I/O	LC	pcie device reset
SNK1_HPD	AA2	I/O	LC	HPD signaling for DPSNK1
GPIO_7	Y4	I/O	LC	General purpose I/O
TMU_CLKIN	W6	I/O	LC	TMU clock input
GPIO_9	Y6	OD O	LC	General purpose I/O
RESET_N	E5	I/O	POC	Main power reset signal
RBIAS	J6	A-in		External resistor for CIO Resistor value 4.75KOhm +/- 0.5%
RSENSE	J5	A-in		External resistor for CIO/PE Resistor value 4.75KOhm +/- 0.5%
PCIE_RBIAS	N16	A-in		External resistor for pcie. Resistor value 3.01KOhm +/- 1%
TEST_EDM	D4	In		Testability signal, connect to GND
PB_USB2_RBIAS	F19	A-in		External resistor for USB2 Resistor value 200 Ohm +/- 1%
PA_USB2_RBIAS	H19	A-in		External resistor for USB2 Resistor value 200 Ohm +/- 1%
THERMDA	V8	A-out	LC	Thermal Diode pin (anode)
USB_MONDC	AC1	A-in		Force/monitor options in the DPSNK analog
PC_MONDC	AC23	A-in		Force/monitor options in the DPSNK analog
PA_MONDC	A23	A-inout		Force/monitor options in the CIO analog
PB_MONDC	A1	A-inout		Force/monitor options in the CIO analog
ATEST_N	J11	A-inout		Analog DFT
ATEST_P	J9	A-inout		Analog DFT
PA_I2C_INT	M4	A-inout		Port A/B I2C interrupt line
PB_I2C_INT	M5	A-inout		Port A/B I2C interrupt line
VGA_RES	H5	A-inout		Analog DFT



2.1.10 Power and Ground

Table 10. Power and Ground Signals

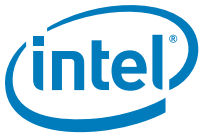
Name	Pin number	Description
VCC3P3_SX	F18, R6	VCC 3.3v main power supply in Sx mode. System sustain rail.
VCC3P3_S0	L6	VCC 3.3v main power supply in active modes. System S0 rail.
VCC3P3_LC	V6	VCC 3.3v output, should be connected to JTAG PUs. Total Capacitance on this pin must not exceed 1uF.
VCC3P3A	E6	VCC 3.3v power supply input for SVR connected to VCC3P3_S0 rail.
VCC0P9_SVR_BRD_SENSE	E8	DFT sense for SVR
VCC3P3_ANA	E16	Analog supply. Connect via capacitor to ground.
VCC0P9_SVR_PAB_ANA	H9, H11, H12, H13, H15, H16	Analog supply. Connect to VCC0P9_SVR and via capacitor to ground.
VCC3P3_ANA_USB2	H18	USB2 analog supply. Connect via capacitor to ground.
VCC0P9_SVR_DPAUX_ANA	N6	Analog supply. Connect to VCC0P9_SVR and via capacitor to ground.
VCC3P3_SVR	G1, G2, H2	VCC 3.3v SVR input connected to VCC3P3_S0 rail.
VCC0P9_LC	J8	Connect via capacitor to ground
SVR_IND	K1, K2, L1, L2	Connect via inductor to VCC0P9_SVR_SENSE
FUSE_VQPS_64	L8	Testability signal, connect to GND
VCC3P3_ANA_PCIE	L16	VCC 3.3v for PCIE analog. Connect via capacitor to ground.
VCC0P9_PCIE	J18	VCC 0.9v for PCIE analog. Connect via capacitor to ground.
VCC0P9_ANA_PCIE_2	L18, M16, M18	VCC 0.9v for PCIE analog. Connect via capacitor to ground.
VCC0P9_ANA_PCIE_1	L19, M19	VCC 0.9v for PCIE analog. Connect via capacitor to ground.
VCC0P9_LVR	H8	VCC 0.9v from LVR. Connect via capacitor to ground.
VCC0P9_LVR_SENSE	H6	Connect to VCC0P9_LVR
VCC0P9_SVR	J13, L11, L13, M11, M13, M8, N11, N13, N8, R11, R13, R16, R8, T16, T8	VCC 0.9v SVR output

Name	Pin number	Description
VCC0P9_SVR_USB_ANA	T11, T9	Analog supply. Connect to VCC0P9_SVR and via capacitor to ground.
VCC0P9_SVR_PC_ANA	T12, T13, T15	Analog supply. Connect to VCC0P9_SVR and via capacitor to ground.
SVR_VSS	H1, J1, J2	VSS for SVR
VSS	F4, L12, L15, L9, M1, M12, M15, M2, M9, N12, N15, N9, R12, R15, R9, T18, T6, V16, V18	VSS for digital
VSS_ANA	A10, A12, A14, A16, A18, A2, A20, A22, A4, A6, A8, AA22, AA23, AB1, AB10, AB12, AB14, AB16, AB18, AB2, AB20, AB22, AB4, AB6, AB8, AC10, AC12, AC14, AC16, AC18, AC2, AC20, AC22, AC4, AC6, AC8, B1, B10, B12, B14, B16, B18, B2, B20, B22, B4, B6, B8, C22, C23, D1, D11, D12, D13, D15, D16, D18, D2, D6, D8, D9, E11, E12, E13, E15, E18, E22, E23, E4, E9, F1, F11, F12, F13, F15, F16, F2, F20, F5, F6, F8, F9, G22, G23, H20, J12, J15, J16, J19, J20, J22, J23, L20, L22, L23, M20, M6, N18, N19, N20, N22, N23, R18, R19, R20, R22, R23, T20, U22, U23, V11, V12, V13, V15, V20, V9, W11, W12, W13, W15, W22, W23, W8, W9, Y11, Y12, Y13, Y15, Y5, Y8, Y9	VSS for analog

2.1.11 Alphabetical Pinout/Signal Name

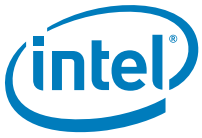
Table 11. Signal Name Associated with Each Pin

Pin Name	Signal Name	Pin Name	Signal Name
A1	PB_MONDC	H6	VCC0P9_LVR_SENSE
A10	VSS_ANA	H8	VCC0P9_LVR
A11	BSSTXp1	H9	VCC0P9_SVR_PAB_ANA
A12	VSS_ANA	J1	SVR_VSS
A13	BSSRXp1	J11	ATEST_N
A14	VSS_ANA	J12	VSS_ANA
A15	ASSRXp2	J13	VCC0P9_SVR
A16	VSS_ANA	J15	VSS_ANA
A17	ASSTXp2	J16	VSS_ANA
A18	VSS_ANA	J18	VCC0P9_PCIE
A19	ASSTXp1	J19	VSS_ANA
A2	VSS_ANA	J2	SVR_VSS
A20	VSS_ANA	J20	VSS_ANA
A21	ASSRXn1	J22	VSS_ANA
A22	VSS_ANA	J23	VSS_ANA
A23	PA_MONDC	J4	ASBU2
A3	NC_A3	J5	RSENSE
A4	VSS_ANA	J6	RBIAS
A5	NC_A5	J8	VCC0P9_LC



Pin Name	Signal Name	Pin Name	Signal Name
A6	VSS_ANA	J9	ATEST_P
A7	BSSRXn2	K1	SVR_IND
A8	VSS_ANA	K2	SVR_IND
A9	BSSTXp2	K22	PCIE_TX2_N
AA1	DEV_PERST_N	K23	PCIE_TX2_P
AA2	SNK1_HPD	L1	SVR_IND
AA22	VSS_ANA	L11	VCC0P9_SVR
AA23	VSS_ANA	L12	VSS
AB1	VSS_ANA	L13	VCC0P9_SVR
AB10	VSS_ANA	L15	VSS
AB11	DPSNK1_ML2_N	L16	VCC3P3_ANA_PCIE
AB12	VSS_ANA	L18	VCC0P9_ANA_PCIE_2
AB13	DPSNK1_ML3_P	L19	VCC0P9_ANA_PCIE_1
AB14	VSS_ANA	L2	SVR_IND
AB15	DPSRC_ML3_N	L20	VSS_ANA
AB16	VSS_ANA	L22	VSS_ANA
AB17	DPSRC_ML2_P	L23	VSS_ANA
AB18	VSS_ANA	L4	BSBU1
AB19	DPSRC_ML1_N	L5	BSBU2
AB2	VSS_ANA	L6	VCC3P3_S0
AB20	VSS_ANA	L8	FUSE_VQPS_64
AB21	DPSRC_ML0_P	L9	VSS
AB22	VSS_ANA	M1	VSS
AB23	PCIE_ATEST	M11	VCC0P9_SVR
AB3	U0_SSRXn1	M12	VSS
AB4	VSS_ANA	M13	VCC0P9_SVR
AB5	U0_SSTXn1	M15	VSS
AB6	VSS_ANA	M16	VCC0P9_ANA_PCIE_2
AB7	DPSNK1_ML0_N	M18	VCC0P9_ANA_PCIE_2
AB8	VSS_ANA	M19	VCC0P9_ANA_PCIE_1
AB9	DPSNK1_ML1_P	M2	VSS
AC1	USB_MONDC	M20	VSS_ANA
AC10	VSS_ANA	M22	PCIE_RX2_N
AC11	DPSNK1_ML2_P	M23	PCIE_RX2_P
AC12	VSS_ANA	M4	PA_I2C_INT
AC13	DPSNK1_ML3_N	M5	PB_I2C_INT
AC14	VSS_ANA	M6	VSS_ANA
AC15	DPSRC_ML3_P	M8	VCC0P9_SVR
AC16	VSS_ANA	M9	VSS
AC17	DPSRC_ML2_N	N1	DPSNK1_AUX_P

Pin Name	Signal Name	Pin Name	Signal Name
AC18	VSS_ANA	N11	VCC0P9_SVR
AC19	DPSRC_ML1_P	N12	VSS
AC2	VSS_ANA	N13	VCC0P9_SVR
AC20	VSS_ANA	N15	VSS
AC21	DPSRC_ML0_N	N16	PCIE_RBIAS
AC22	VSS_ANA	N18	VSS_ANA
AC23	PC_MONDC	N19	VSS_ANA
AC3	U0_SSRXp1	N2	DPSNK1_AUX_N
AC4	VSS_ANA	N20	VSS_ANA
AC5	U0_SSTXp1	N22	VSS_ANA
AC6	VSS_ANA	N23	VSS_ANA
AC7	DPSNK1_ML0_P	N4	DPSRC_AUX_P
AC8	VSS_ANA	N5	DPSRC_AUX_N
AC9	DPSNK1_ML1_N	N6	VCC0P9_SVR_DPAUX_ANA
B1	VSS_ANA	N8	VCC0P9_SVR
B10	VSS_ANA	N9	VSS
B11	BSSTXn1	P1	NC_P1
B12	VSS_ANA	P2	NC_P2
B13	BSSRXn1	P22	PCIE_TX1_N
B14	VSS_ANA	P23	PCIE_TX1_P
B15	ASSRXn2	R1	PB_USB2_MXCTL
B16	VSS_ANA	R11	VCC0P9_SVR
B17	ASSTXn2	R12	VSS
B18	VSS_ANA	R13	VCC0P9_SVR
B19	ASSTXn1	R15	VSS
B2	VSS_ANA	R16	VCC0P9_SVR
B20	VSS_ANA	R18	VSS_ANA
B21	ASSRXp1	R19	VSS_ANA
B22	VSS_ANA	R2	PA_USB2_MXCTL
B23	USB2_ATEST	R20	VSS_ANA
B3	NC_B3	R22	VSS_ANA
B4	VSS_ANA	R23	VSS_ANA
B5	NC_B5	R4	TEST_EN
B6	VSS_ANA	R5	DPSRC_HPD
B7	BSSRXp2	R6	VCC3P3_SX
B8	VSS_ANA	R8	VCC0P9_SVR
B9	BSSTXn2	R9	VSS
C1	NC_C1	T1	PB_HPD
C2	NC_C2	T11	VCC0P9_SVR_USB_ANA
C22	VSS_ANA	T12	VCC0P9_SVR_PC_ANA



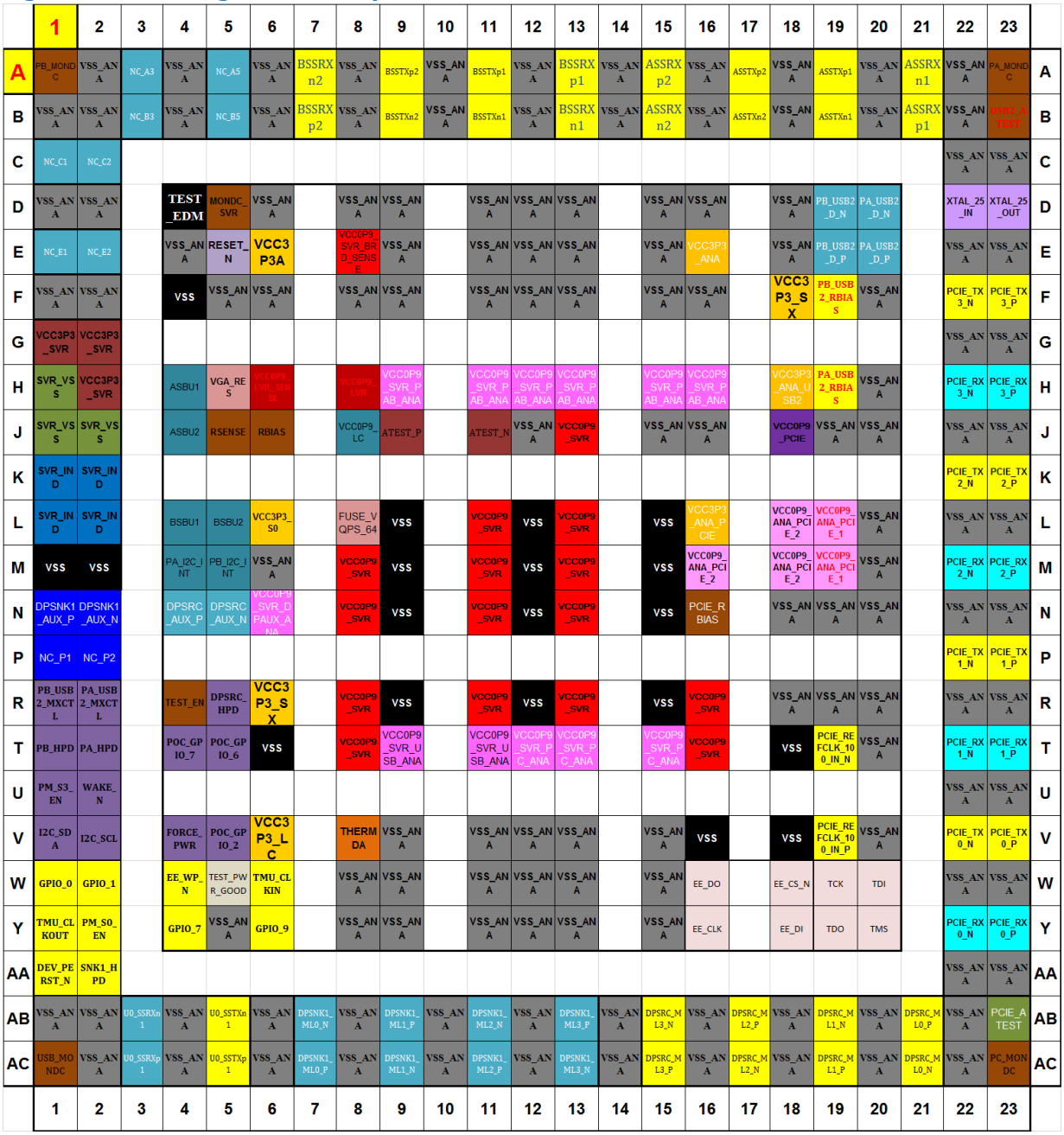
Pin Name	Signal Name	Pin Name	Signal Name
C23	VSS_ANA	T13	VCC0P9_SVR_PC_ANA
D1	VSS_ANA	T15	VCC0P9_SVR_PC_ANA
D11	VSS_ANA	T16	VCC0P9_SVR
D12	VSS_ANA	T18	VSS
D13	VSS_ANA	T19	PCIE_REFCLK_100_IN_N
D15	VSS_ANA	T2	PA_HPD
D16	VSS_ANA	T20	VSS_ANA
D18	VSS_ANA	T22	PCIE_RX1_N
D19	PB_USB2_D_N	T23	PCIE_RX1_P
D2	VSS_ANA	T4	POC_GPIO_7
D20	PA_USB2_D_N	T5	POC_GPIO_6
D22	XTAL_25_IN	T6	VSS
D23	XTAL_25_OUT	T8	VCC0P9_SVR
D4	TEST_EDM	T9	VCC0P9_SVR_USB_ANA
D5	MONDC_SVR	U1	PM_S3_EN
D6	VSS_ANA	U2	WAKE_N
D8	VSS_ANA	U22	VSS_ANA
D9	VSS_ANA	U23	VSS_ANA
E1	NC_E1	V1	I2C_SDA
E11	VSS_ANA	V11	VSS_ANA
E12	VSS_ANA	V12	VSS_ANA
E13	VSS_ANA	V13	VSS_ANA
E15	VSS_ANA	V15	VSS_ANA
E16	VCC3P3_ANA	V16	VSS
E18	VSS_ANA	V18	VSS
E19	PB_USB2_D_P	V19	PCIE_REFCLK_100_IN_P
E2	NC_E2	V2	I2C_SCL
E20	PA_USB2_D_P	V20	VSS_ANA
E22	VSS_ANA	V22	PCIE_TX0_N
E23	VSS_ANA	V23	PCIE_TX0_P
E4	VSS_ANA	V4	FORCE_PWR
E5	RESET_N	V5	POC_GPIO_2
E6	VCC3P3A	V6	VCC3P3_LC
E8	VCC0P9_SVR_BRD_SENSE	V8	THERMDA
E9	VSS_ANA	V9	VSS_ANA
F1	VSS_ANA	W1	GPIO_0
F11	VSS_ANA	W11	VSS_ANA
F12	VSS_ANA	W12	VSS_ANA
F13	VSS_ANA	W13	VSS_ANA
F15	VSS_ANA	W15	VSS_ANA

Pin Name	Signal Name	Pin Name	Signal Name
F16	VSS_ANA	W16	EE_DO
F18	VCC3P3_SX	W18	EE_CS_N
F19	PB_USB2_RBIAS	W19	TCK
F2	VSS_ANA	W2	GPIO_1
F20	VSS_ANA	W20	TDI
F22	PCIE_TX3_N	W22	VSS_ANA
F23	PCIE_TX3_P	W23	VSS_ANA
F4	VSS	W4	EE_WP_N
F5	VSS_ANA	W5	TEST_PWR_GOOD
F6	VSS_ANA	W6	TMU_CLKIN
F8	VSS_ANA	W8	VSS_ANA
F9	VSS_ANA	W9	VSS_ANA
G1	VCC3P3_SVR	Y1	TMU_CLKOUT
G2	VCC3P3_SVR	Y11	VSS_ANA
G22	VSS_ANA	Y12	VSS_ANA
G23	VSS_ANA	Y13	VSS_ANA
H1	SVR_VSS	Y15	VSS_ANA
H11	VCC0P9_SVR_PAB_ANA	Y16	EE_CLK
H12	VCC0P9_SVR_PAB_ANA	Y18	EE_DI
H13	VCC0P9_SVR_PAB_ANA	Y19	TDO
H15	VCC0P9_SVR_PAB_ANA	Y2	PM_S0_EN
H16	VCC0P9_SVR_PAB_ANA	Y20	TMS
H18	VCC3P3_ANA_USB2	Y22	PCIE_RX0_N
H19	PA_USB2_RBIAS	Y23	PCIE_RX0_P
H2	VCC3P3_SVR	Y4	GPIO_7
H20	VSS_ANA	Y5	VSS_ANA
H22	PCIE_RX3_N	Y6	GPIO_9
H23	PCIE_RX3_P	Y8	VSS_ANA
H4	ASBU1	Y9	VSS_ANA
H5	VGA_RES		

2.2 Pin Map

Figure 2 shows the pin assignments for the package. This is a top view, looking from the die to the PCB.

Figure 2. Titan Ridge DD Pin Map



3.0 Flash Memory

3.1 Flash Types Supported

Table 12. Supported types of Flash Memory

Manufacturer	Type	Volume, Mbit	Supply, V
AMIC	A25L080	8.0	3.0-3.6
Giga Device	GD25Q80C	8.0	2.7-3.6
Giga Device	GD25Q80CTIG	8.0	3.3
EON	EN25Q80B	8.0	2.7-3.6
FMSH	FM25Q08	8.0	2.7-3.6
Macronix	MX25L8006EM1I	8.0 (150mil, 8-SOP)	2.7-3.6
Winbond	W25Q80DL	8.0	2.3-3.6

Additional requirements:

- At least 50.0 MHz clock rate support
- 3.3 V operating voltage
- 4KB sector size
- Minimum instruction set list required:
    - 0x06 - Write Enable (WREN)
    - 0x04 - Write Disable (WRDI)
    - 0x05 – Read Status Register (RDSR)
    - 0x0B – Fast Read (FR)
    - 0x02 – Page Program (PP)
    - 0x20 – Sector Erase (SE)

3.2 Flash Memory Map

The Titan Ridge DD uses flash memory for initialization of various internal parameters, enable/disable bits, analog modules configuration, and internal microcontrollers' ucode patches.

The flash memory map is divided into sections, which are contiguous and expected in the defined order. Each section starts with a length (length units are different for each section) and is followed by data.

The flash memory map is described in Figure 3 and Table 13.

Figure 3. Flash Content Structure

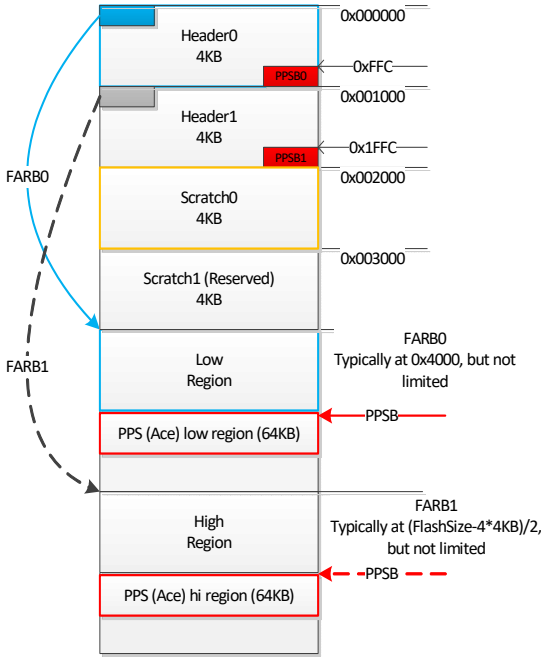


Table 13. Flash Memory Map

ADDRESS, B	DATA	COMMENT
0x000000	FARB0	Flash Active Region Base Pointer 0 – contains **Digital_Base_Pointer** (if doesn't equal to 0x000000 or 0xFFFFFF)
0x000004…..	Security FW	If security enabled – Security FW
0x1FFC	PPSB0	Pointer to PPS section in relative active region
0x001000	FARB1	Flash Active Region Base Pointer 1 – contains **Digital_Base_Pointer** (if doesn't exist FARB1 or doesn't equal to 0x000000 or 0xFFFFFF)
0x001004…..	Security FW	If security enabled – Security FW
0x2FFC	PPSB1	Pointer to PPS section in relative active region
0x2000	Scratch_region_0 (4KB)	Scratch section
0x3000	Scratch_region_1 (4KB)	Scratch section
Digital_Base_Pointer = FARB0/FARB1	Digital section Size Byte 0	Contains **Digital_section_Size[7:0]** (Digital Section Size)
Digital_Base_Pointer + 1	Digital section Size Byte 1	Contains **Digital_section_Size[15:8]** (Digital Section Size)
Digital_Base_Pointer + 2	Start of Digital Section Data	
….	Digital Section Data	
Digital_Base_Pointer + Digital_Size + 1	End of Digital Section Data	

Table 13. Flash Memory Map

ADDRESS, B	DATA	COMMENT
SVR_Ana_Base_Pointer = Digital_Base_Pointer + Digital_Size + 2	SVR_ANASection Size Byte 0	Contains SVR_Ana_Size[7:0] (SVR Analog Section Size)
SVR_Ana_Base_Pointer + 1	SVR_ANA Section Size Byte 1	Contains **Svr_Ana_Size[15:8]** (Switch voltage Regulator Analog Section Size)
SVR_Ana_Base_Pointer + 2	Start of SVR_ANA Section Data	
…	SVR_ANA Section Data	
Svr_Ana_Base_Pointer + Svr_Ana_Size * 2 + 1	End of SVR_ANA Section Data	
…	Don’t care data	
DROM_base_pointer = ee_drom_start_addr[32:0] + Digital_Base_Pointer	DROM Size Byte 0,1,2,3	Contains DROM_Size[31:0] (DROM Section Size)
DROM_base_pointer + 4	Start of DROM Section Data	
…..	DROM section data	
DROM_base_pointer + (4 X DROM_size)-1	end of DROM Section Data	DROM Size in amount of Dword's
…	Don't care data	
Arc_param_base_pointer = ee_arc_ee_base[31:0] + Digital_Base_Pointer	arc_param Size Byte 0,1,2,3	Contains arc_param_Size[31:0] (arc_param Section Size)
Arc_param_base_pointer + 4	Start of arc_param Section Data	
…	Arc_param section data	
Arc_param_base_pointer + 4 + (4 x arc_param_size)-1	End of arc_param Section Data	Arc_param Size in amount of Dword's
…	Don't care data	
EE2TAR_*_Base_pointer = ee_to_tar_*_base[23:0] + Digital_Base_Pointer	Start of EE2TAR_* Section Data	"*" = { total 16 possible ee2tar for different use in the chip}
…..	EE2TAR_* section data	
EE2TAR_*_Base_pointer + (ee_to_tar_*_size[7:0] * 2 * 4)-1	End of EE2TAR_* Section Data	EE_2_TAR's sections Size in amount of tuples (tuple = two Dword)
…	Don’t care data	
Cp_Ucode_Base_Pointer = ee_ucode_start_addr + Digital_Base_Pointer	CP_UCODE Section Size Byte 0	Contains **Cp_Ucode_Size[7:0]** (Control Port uCode Patch Section Size), **ee_ucode_start_addr[15:0]** – relative pointer from Digital Section
Cp_Ucode_Base_Pointer + ee_read_ctrl_ucode	CP_UCODE Section Size Byte 1	Contains **Cp_Ucode_Size[15:8]** (Control Port uCode Patch Section Size)
Cp_Ucode_Base_Pointer + 2 * ee_read_ctrl_ucode	Start of CP_UCODE Section Data	
…	CP_UCODE Section Data	
Cp_Ucode_Base_Pointer + (Cp_Ucode_Size * 4 + 1) * ee_read_ctrl_ucode	End of CP_UCODE Section Data	

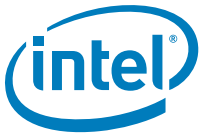


Table 13. Flash Memory Map

ADDRESS, B	DATA	COMMENT
Hdp_Out_Ucode_Base_Pointer = Cp_Ucode_Base_Pointer + (Cp_Ucode_Size * 4 + 2) * ee_read_ctrl_ucode	HDP_OUT_UCODE Section Size Byte 0	Contains **Hdp_Out_Ucode_Size[7:0]** (Display Port Out uCode Patch Section Size)
Hdp_Out_Ucode_Base_Pointer + ee_read_dp_out_ucode	HDP_OUT_UCODE Section Size Byte 1	Contains **Hdp_Out_Ucode_Size [15:8]** (Display Port Out uCode Patch Section Size)
Hdp_Out_Ucode_Base_Pointer + 2 * ee_read_dp_out_ucode	Start of HDP_OUT_UCODE Section Data	
…	HDP_OUT_UCODE Section Data	
Hdp_Out_Ucode_Base_Pointer + (Hdp_Out_Ucode_Size * 4 + 1) * ee_read_dp_out_ucode	End of HDP_OUT_UCODE Section Data	
Hdp_In_Ucode_Base_Pointer = Hdp_Out_Ucode_Base_Pointer + (Hdp_Out_Ucode_Size * 4 + 2) * ee_read_dp_out_ucode	HDP_IN_UCODE Section Size Byte 0	Contains **Hdp_Out_Ucode_Size[7:0]** (Display Port Out uCode Patch Section Size)
Hdp_In_Ucode_Base_Pointer + ee_read_dp_in_ucode	HDP_IN_UCODE Section Size Byte 1	Contains **Hdp_In_Ucode_Size [15:8]** (Display Port In uCode Patch Section Size)
Hdp_In_Ucode_Base_Pointer + 2 * ee_read_dp_in_ucode	Start of HDP_IN_UCODE Section Data	
…	HDP_IN_UCODE Section Data	
Hdp_In_Ucode_Base_Pointer + (Hdp_In_Ucode_Size * 4 + 1) * ee_read_dp_in_ucode	End of HDP_IN_UCODE Section Data	
Lc_iram_Ucode_Base_Pointer = Hdp_In_Ucode_Base_Pointer + (Hdp_In_Ucode_Size * 4 + 2) * ee_read_dp_in_ucode	LC_iram_UCODE Section Size Byte 0	Contains **Lc_iram_Ucode_Size[7:0]** (Display Link Controller uCode Patch Section Size)
Lc_iram_Ucode_Base_Pointer + ee_read_iram_dram_ucode	LC_iram_UCODE Section Size Byte 1	Contains **Lc_iram_Ucode_Size [15:8]** (Link Controller uCode Patch Section Size)
Lc_iram_Ucode_Base_Pointer + 2 * ee_read_lc_iram_dram_ucode	Start of LC_iram_UCODE Section Data	
…	LC_iram_UCODE Section Data	
Lc_iram_Ucode_Base_Pointer + (Lc_iram_Ucode_Size * 4 + 1) * ee_read_lc_iram_dram_ucode	End of LC_iram_UCODE Section Data	
Lc_dram_Ucode_Base_Pointer = Lc_iram_Ucode_Base_Pointer + (Lc_iram_Ucode_Size * 4 + 2) * ee_read_dp_in_ucode	LC_dram_UCODE Section Size Byte 0	Contains **Lc_dram_Ucode_Size[7:0]** (Display Link Controller uCode Patch Section Size)
Lc_dram_Ucode_Base_Pointer + ee_read_iram_dram_ucode	LC_dram_UCODE Section Size Byte 1	Contains **Lc_dram_Ucode_Size [15:8]** (Link Controller uCode Patch Section Size)
Lc_dram_Ucode_Base_Pointer + 2 * ee_read_lc_iram_dram_ucode	Start of LC_dram_UCODE Section Data	
…	LC_dram_UCODE Section Data	
Lc_dram_Ucode_Base_Pointer + (Lc_dram_Ucode_Size * 4 + 1) * ee_read_lc_iram_dram_ucode	End of LC_dram_UCODE Section Data	

Table 13. Flash Memory Map

ADDRESS, B	DATA	COMMENT
Arc_Ucode_Base_Pointer = Lc_Ucode_Base_Pointer + (Lc_Ucode_Size * 4 + 2) * ee_read_clc_ucode	ARC_UCODE Section Size Byte 0	Contains **Arc_Ucode_Size[7:0]** (Display Arc Controller uCode Patch Section Size)
Arc_Ucode_Base_Pointer + ee_read_arc_ucode	ARC_UCODE Section Size Byte 1	Contains **Arc_Ucode_Size [15:8]** (Arc Controller uCode Patch Section Size)
Arc_Ucode_Base_Pointer + 2 * ee_read_arc_ucode	Start of ARC_UCODE Section Data	
…	ARC_UCODE Section Data	
Arc_Ucode_Base_Pointer + (Arc_Ucode_Size * 4 + 1) * ee_read_arc_ucode	End of ARC_UCODE Section Data	
cio_iram_0_Ucode_Base_Pointer = Arc_Ucode_Base_Pointer + (arc_Ucode_Size * 4 + 2) * ee_read_arc_ucode	CIO_IRAM_0_UCODE Section Size Byte 0	Contains cio_iram_0_Ucode_Size[7:0] (Display cio_iram_0 Controller uCode Patch Section Size)
cio_iram_0_Ucode_Base_Pointer + ee_read_cio_iram_dram_0_ucode	CIO_IRAM_0_UCODE Section Size Byte 0	Contains cio_iram_0_Ucode_Size [15:8] (cio_iram_0 Controller uCode Patch Section Size)
cio_iram_0_Ucode_Base_Pointer + 2 * ee_read_cio_iram_dram_0_ucode	Start of CIO_IRAM_0_UCODE Section Data	
…	CIO_IRAM_0_UCODE Section Data	
cio_iram_0_Ucode_Base_Pointer + (cio_iram_0_Ucode_Size * 4 + 1) * ee_read_cio_iram_dram_ucode	End of CIO_IRAM_0_UCODE Section Data	
cio_dram_0_Ucode_Base_Pointer = cio_iram_0_Ucode_Base_Pointer + (cio_iram_0_Ucode_Size * 4 + 2) * ee_read_cio_iram_dram_0_ucode	CIO_DRAM_0_UCODE Section Size Byte 0	Contains cio_dram_0_Ucode_Size[7:0] (Display cio_dram_0 Controller uCode Patch Section Size)
cio_dram_0_Ucode_Base_Pointer + ee_read_cio_iram_dram_0_ucode	CIO_DRAM_0_UCODE Section Size Byte 1	Contains cio_dram_0_Ucode_Size [15:8] (cio_dram_0 Controller uCode Patch Section Size)
cio_dram_0_Ucode_Base_Pointer + 2 * ee_read_cio_iram_dram_0_ucode	Start of CIO_DRAM_0_UCODE Section Data	
…	CIO_DRAM_0_UCODE Section Data	
cio_dram_0_Ucode_Base_Pointer + (cio_dram_0_Ucode_Size * 4 + 1) * ee_read_cio_iram_dram_0_ucode	End of CIO_DRAM_0_UCODE Section Data	
cio_iram_1_Ucode_Base_Pointer = cio_dram_0_Ucode_Base_Pointer + (cio_dram_0_Ucode_Size * 4 + 2) * ee_read_cio_iram_dram_1_ucode	CIO_IRAM_1_UCODE Section Size Byte 0	Contains cio_iram_1_Ucode_Size[7:0] (Display cio_iram_1 Controller uCode Patch Section Size)
cio_iram_1_Ucode_Base_Pointer + ee_read_cio_iram_dram_1_ucode	CIO_IRAM_1_UCODE Section Size Byte 0	Contains cio_iram_1_Ucode_Size [15:8] (cio_iram_0 Controller uCode Patch Section Size)
cio_iram_1_Ucode_Base_Pointer + 2 * ee_read_cio_iram_dram_0_ucode	Start of CIO_IRAM_1_UCODE Section Data	
…	CIO_IRAM_1_UCODE Section Data	

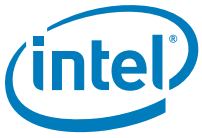


Table 13. Flash Memory Map

ADDRESS, B	DATA	COMMENT
cio_iram_1_Ucode_Base_Pointer + (cio_iram_1_Ucode_Size * 4 + 1) * ee_read_cio_iram_dram_ucode	End of CIO_IRAM_1_UCODE Section Data	
cio_dram_1_Ucode_Base_Pointer = cio_iram_1_Ucode_Base_Pointer + (cio_iram_1_Ucode_Size * 4 + 2) * ee_read_cio_iram_dram_1_ucode	CIO_DRAM_1_UCODE Section Size Byte 0	Contains cio_dram_1_Ucode_Size[7:0] (Display cio_dram_1 Controller uCode Patch Section Size)
cio_dram_1_Ucode_Base_Pointer + ee_read_cio_iram_dram_1_ucode	CIO_DRAM_1_UCODE Section Size Byte 1	Contains cio_dram_1_Ucode_Size [15:8] (cio_dram_1 Controller uCode Patch Section Size)
cio_dram_1_Ucode_Base_Pointer + 2 * ee_read_cio_iram_dram_1_ucode	Start of CIO_DRAM_1_UCODE Section Data	
…	CIO_DRAM_1_UCODE Section Data	
cio_dram_1_Ucode_Base_Pointer + (cio_dram_1_Ucode_Size * 4 + 1) * ee_read_cio_iram_dram_1_ucode	End of CIO_DRAM_1_UCODE Section Data	
…	Don’t care data	
cio_iram_2_Ucode_Base_Pointer = cio_dram_1_Ucode_Base_Pointer + (cio_dram_1_Ucode_Size * 4 + 2) * ee_read_cio_iram_dram_1_ucode	CIO_IRAM_2_UCODE Section Size Byte 0	Contains cio_iram_2_Ucode_Size[7:0] (Display cio_iram_2 Controller uCode Patch Section Size)
cio_iram_2_Ucode_Base_Pointer + ee_read_cio_iram_dram_2_ucode	CIO_IRAM_2_UCODE Section Size Byte 0	Contains cio_iram_2_Ucode_Size [15:8] (cio_iram_1 Controller uCode Patch Section Size)
cio_iram_2_Ucode_Base_Pointer + 2 * ee_read_cio_iram_dram_0_ucode	Start of CIO_IRAM_2_UCODE Section Data	
…	CIO_IRAM_2_UCODE Section Data	
cio_iram_2_Ucode_Base_Pointer + (cio_iram_2_Ucode_Size * 4 + 1) * ee_read_cio_iram_dram_ucode	End of CIO_IRAM_2_UCODE Section Data	
cio_dram_2_Ucode_Base_Pointer = cio_iram_2_Ucode_Base_Pointer + (cio_iram_2_Ucode_Size * 4 + 2) * ee_read_cio_iram_dram_1_ucode	CIO_DRAM_2_UCODE Section Size Byte 0	Contains cio_dram_2_Ucode_Size[7:0] (Display cio_dram_2 Controller uCode Patch Section Size)
cio_dram_2_Ucode_Base_Pointer + ee_read_cio_iram_dram_2_ucode	CIO_DRAM_2_UCODE Section Size Byte 1	Contains cio_dram_2_Ucode_Size [15:8] (cio_dram_2 Controller uCode Patch Section Size)
cio_dram_2_Ucode_Base_Pointer + 2 * ee_read_cio_iram_dram_2_ucode	Start of CIO_DRAM_2_UCODE Section Data	
…	CIO_DRAM_2_UCODE Section Data	
cio_dram_2_Ucode_Base_Pointer + (cio_dram_2_Ucode_Size * 4 + 1) * ee_read_cio_iram_dram_2_ucode	End of CIO_DRAM_2_UCODE Section Data	
…	Don’t care data	
Arc_Cache_Base_Pointer = arc_cache_rd_addr	Start of ARC_CACHE Data	**arc_cache_rd_addr[23:0]** – absolute pointer from Arc Cache Read i/f
…	ARC_CACHE Data	

Table 13. Flash Memory Map

ADDRESS, B	DATA	COMMENT
Arc_Cache_Base_Pointer + Arc_Cache_Size - 1	End of ARC_CACHE Data	Arc_Cache_Size = **arc_cache_rd_length[15:0]** – data from Arc Cache Read i/f
…	Don’t care data	
pps_Base_Pointer = PPSB0/PPSB1	PPS section	

3.2.1 Flash memory Read Flow

The Flash memory read procedure is as follows:

- LC domain Auto-load data caused by car_power_good_e (power good reset) de-assertion
  - — Detection of valid data recorded in the Flash Memory
    - —Read the first 24 bits from Flash Memory
      - — If 0xFFFFFF, no FARB (Flash Active Base Pointer) found ' try to read from 4K offset (Flash Address 0x1000)
      - — Else the content reflects FARB ' go start to read Digital section from this pointer
    - —Read 24 bits from 4K offset (Flash Address 0x1000)
      - — If 0xFFFFFF, no FARB (Flash Active Base Pointer) found, no valid Flash memory attached or no valid data recorded on Flash Memory ' done
      - — Else the content reflects FARB ' go start to read Digital section from this pointer
  - — Read Digital section according to section size (length (16 bits) is number of bytes)
  - — Read SVR Analog section according to section size (length (16 bits) is number of address (8 bits)/data (8 bits) tuples)
  - — - If enabled by repressive bit in digital section, read the scratch ram section from flash to internal memory, size 256 bytes.
  - — If enabled by the respective bit in the digital section, read the CLC ucode patch section, according to section size (length in DWs - 16bit field).
- Read upon request, per each power_domain above LC domain (such as: ana_comm, dp, pcie, cio and usb), LC FW request relevant section to be loaded from flash. Section includes (uCode's and ee2tars'), ee2tar's are loaded upon triggers align to domain power_up.
- Ucode load sections are:
  - — If enabled by the respective bit in the digital section and requested by LC FW, read the "*_ucode" patch section, according to section size (length in DWs - 16bit field).
  - — "*" = {CP, DP_OUT, DP_IN, LC_IRAM, LC_DRAM, ARC, CIO_IRAM_0, CIO_DRAM_0, CIO_IRAM_1, CIO_DRAM_1},
  - — Both CIO_IRAM and CIO_DRAM must load together
- Ee2tar's load sections are:
  - — If triggered by the respective reset in the ee2tar_fsm, read the "*_ee2tar" section, according to section address and size (length in amount of tuples = two Dword).
  - — "*" = {total 16 possible ee2tar for different use in the chip}.
- After any CIO Reset de-assertion
  - — Control Port initializes PCIe and other parameters from the ee_to_tar section, according to section length (length (8 bits) is number of data (32 bits)/ address (32 bits) tuples)

3.3 Target Bus Access via Flash Memory (ee to tar Section)

As part of the Control Port initialization sequence after CIO Reset, the set of registers pre-configured in the flash memory can be written. This can be done to fix default values or execute a custom workaround/configuration.

In steady state (after initial read), the flash block is ready to accept "by address" reads from the ee2tar_fsm (DW aligned offset, DW per read). These are used for reading address/data tuples from flash memory and writing them onto the Target Bus.

ee_to_tar_base - Base address from which the address/data tuples are read by the ee2tar_fsm.

ee_to_tar_size[7:0] - Size in amount of tuples; 0 = nothing to do.

Note: As the ee_to_tar_size is 8 bit wide, this mechanism is limited to 255 data / command tuples.

The command register parameters are decoded by the Control Port as shown in Table 14:

Table 14. Command Register Parameters

31 24	23 21	20 19	18 13	12 0
Reserved	CMD	CS	Port#	DW Index

Field	Bit(s)	Description	
DW Index	12:0	Sets DW Index Target bus value	
Port#	18:13	Sets Port# Target bus value	
CS	20:19	Sets CS Target bus value, as follows:	
		CS Value	**Configuration space**
		00	Path Config. Space
		01	Port Config. Space
		10	Device Config. Space
		11	Counters Config. Space
CMD	21	0: Read command 1: Write command	
	22	0: Regular Target bus access 1: Access to CIO Switch registers – See below	
	23	0: Regular Target bus access 1: Access to PCIe Switch registers – See below	
Reserved	31:24	Reserved – set to 0	

For PCIe Switch register configuration, the lower 21 bits of the command are regarded in a different fashion than they are at regular Target Access via Flash ():

Table 15. PCIe Switch Command Register Parameters

31 24	23 21	20 19	18 10	9 6	5 0
Rsvd	CMD	Rsvd	Choose Bridge	Ex Reg #	Reg #

Each write access can be made to several ports simultaneously. For this, use encoding of chosen ports, where:

- DMA EMEP_cnfg= Choose_bridge[8]
- xHC EMEP_cnfg = Choose_bridge[6]
- Dn4_cnfg = Choose_bridge[5]
- Dn0_cnfg = Choose_bridge[1]
- Up0_cnfg = Choose_bridge[0]

3.4 Flash Programming Interface

SW fills SPI command, address and [write/read data] using below registers in the below order (i.e. data first, control last).

HW shifts them out accordingly, where data is either shifted out [write] or in [read].

3.4.1 Registers

- SPI_DATA<15:0> // 16 * 32bit registers - total 64B
  - SPI_DATA<15>
  - SPI_DATA<14>
  - . . .
  - SPI_DATA<1>
  - SPI_DATA<0>

  Plain RW registers that either shift-in or shift-out depending on spi_shift_in1_out0
- SPI_CMD_ADDR
  - [23:0] - SPI 24bit address
  - [31:24] - command
- SPI_CONTROL
  - [7:0] spi_data_bytes_amount // amount of bytes to shift in/out
  - [11:8] spi_dummy_bytes_amount // amount of dummy bytes to shift out after 24bit address, before shifting in/out the data
  - [28] nvm_accesses_allowed // secure_en indication read-only value
  - at should be an input signal from flash controller common logic
  - [29] spi_address_present // 1: need to shift out address from SPI_CMD_ADDR after command; 0: command without address
  - [30] spi_shift_in1_out0 // in: read, out:write
  - [31] req1_ack0 // SW to set to 1, HW to clear upon completion
  - Remaining bits are plain r/w for future use

The registers are mapped to flash_ctrl_reg16…flash_ctrl_reg33 (0x40F…0x421 of Flash Controller area in Device Space) in the above order, at consecutive offsets, so that multiple-DW access from CIO will fill it in one single write packet.

Before any write or erase operation, SW/FW should ensure that HW accesses to NVM (thru ee_read_arbiter) are stalled. That is done by setting EEC.bitbang_request and polling EEC.bitbang_ready. After write/erase is completed, EEC.bitbang_request should be cleared.

3.4.2 Examples (based on Winbond W25X10BL/20BL/40BL)

3.4.2.1 Example 1: Read ID - (0x90)

a. Write (possibly using single CIO packet)

SPI_CMD_ADDR = 0x90_000000 // opcode_addr

SPI_CONTROL = 0x00000000 |

1 << 31 | // req1_ack0 = REQ

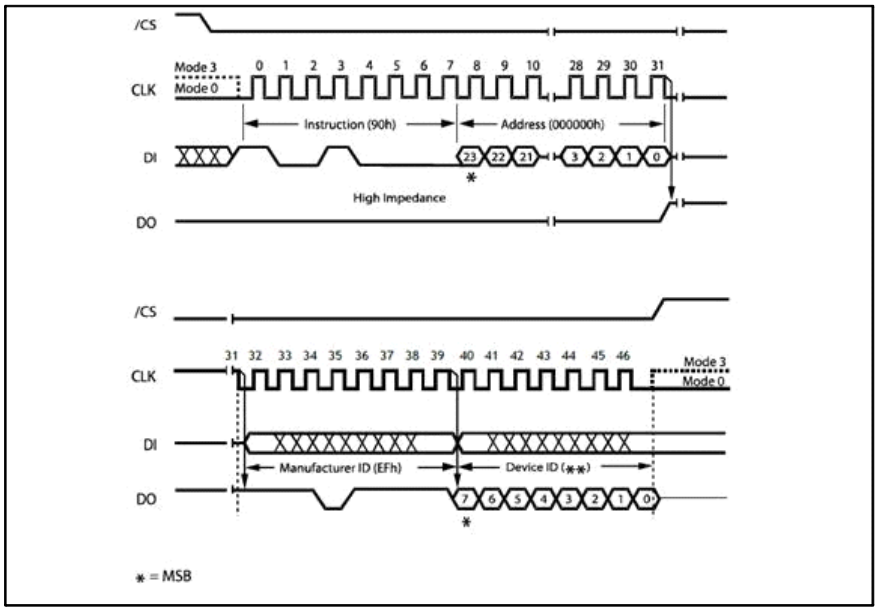
1 << 30 | // spi_shift_in1_out0 = IN/READ

1 << 29 | // spi_address_present = YES

2 << 0 | // spi_data_bytes_amount = 2

That should cause the waveforms in Figure 4.

Figure 4. Read Manufacturer/Device ID diagram



b. While (req1_ack0 from chip)=1 or timeout {

Read (possibly using single CIO packet)

SPI_DATA<0>

SPI_CMD_ADDR

SPI_CONTROL

}

c. ID's are in SPI_DATA<0>[15:0]

3.4.2.2 Example 2: Write Enable - (0x06)

a. Write (possibly using single CIO packet)

SPI_CMD_ADDR = 0x06_000000 // opcode_addr

SPI_CONTROL = 0x00000000 |

1 << 31 | // req1_ack0 = REQ

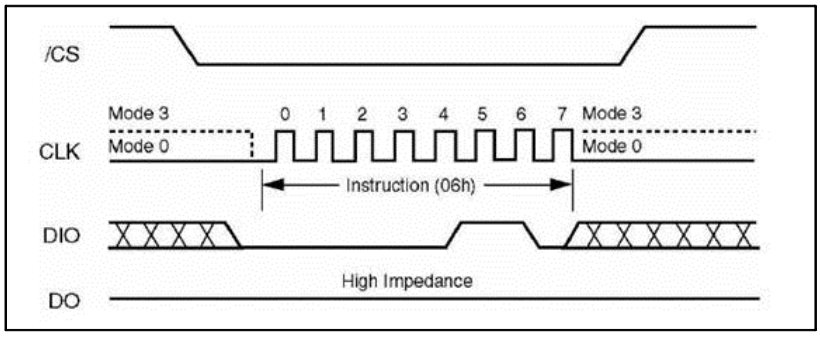
0 << 30 | // spi_shift_in1_out0 = N/A

0 << 29 | // spi_address_present = NO

0 << 0 | // spi_data_bytes_amount = 0

That should cause the waveforms in Figure 5.

Figure 5. Write Enable Instruction Sequence diagram



b. While (req1_ack0 from chip)=1 or timeout {

Read SPI_CONTROL

}

c. Flash is writeable (can be confirmed by reading status)

3.4.2.3 Example 3: Sector Erase - (0x20)

a. Write (possibly using single CIO packet)

SPI_CMD_ADDR = 0x20_000000 // opcode_addr

SPI_CONTROL = 0x00000000 |

1 << 31 | // req1_ack0 = REQ

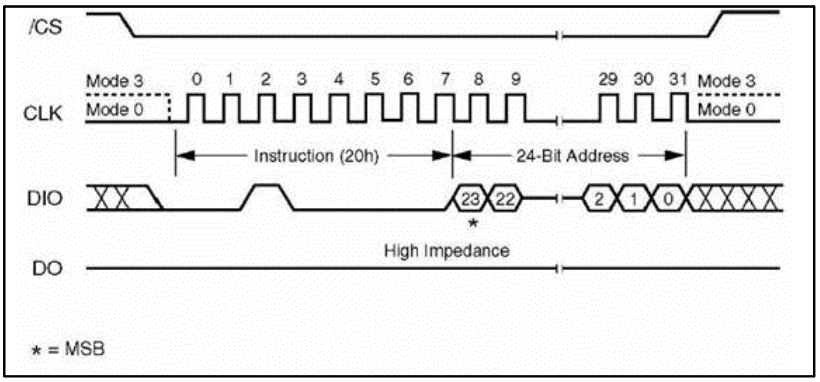
0 << 30 | // spi_shift_in1_out0 = N/A

1 << 29 | // spi_address_present = YES

0 << 0 | // spi_data_bytes_amount = 0

That should cause the waveforms in Figure 6.

Figure 6. Sector Erase Instruction Sequence diagram



b. While (req1_ack0 from chip)=1 or timeout {

Read SPI_CONTROL

}

c. Done erasing

3.4.2.4 Example 4: Page Program - (0x02)

example for 7 Bytes write

a. Write (possibly using single CIO packet)

SPI_DATA<1> = 0x00070605

SPI_DATA<0> = 0x04030201

SPI_CMD_ADDR = 0x02_A3A2A1 // opcode_addr

SPI_CONTROL = 0x00000000 |

1 << 31 | // req1_ack0 = REQ

0 << 30 | // spi_shift_in1_out0 = OUT/WRITE

1 << 29 | // spi_address_present = YES

7 << 0 | // spi_data_bytes_amount = 7

b. That should cause

<02><A3><A2><A1><01><02>...<07>

c. While (req1_ack0 from chip)=1 or timeout {

Read SPI_CONTROL

}

d. Done writing

Note: Before next operation (after write and few others), BUSY should be checked in the status register.

For example:

```
Poll_BUSY() {
SPI_CMD_ADDR = 0x05_000000
do {
   SPI_CONTROL  = 0xC0000001
   While (req1_ack0 from chip)=1 or timeout {
      Read    SPI_CONTROL
   }
   BUSY = SPI_DATA<0>[0]
} while (BUSY or timeout)
}
```

Also Write Enable should be re-issued after EACH Page Program!

3.4.2.5 Example 5: Read Data - (0x03)

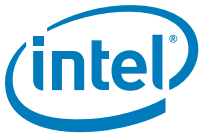
Example for 7 Bytes read

a. Write (possibly using single CIO packet)

```
SPI_CMD_ADDR  = 0x03_A3A2A1  // opcode_addr
SPI_CONTROL   = 0x00000000 |
            1 << 31    | // req1_ack0 = REQ
            1 << 30    | // spi_shift_in1_out0 = IN/READ
            1 << 29    | // spi_address_present = YES
            7 << 0     | // spi_data_bytes_amount = 7
```

b. That should cause

<03><A3><A2><A1><01><02>...<07>



c. While (req1_ack0 from chip)=1 or timeout {

Read (possibly using single CIO packet)

SPI_DATA<1>

SPI_DATA<0>

SPI_CMD_ADDR

SPI_CONTROL

}

d. Read data is placed like in the write command above

3.5 Flash Programming High Level Procedure

To program the next active region, SW/FW should follow the following general procedure:

1 Compute the next (non-active) FARB pointer, next_FARB.

For example, assuming active region immediately follows the headers, that can be done in the following manner:

read Manufacturer/Device ID from the flash chip to determine its size (flash_size)

if (active FARB == 16K) // low region is active

next_FARB = (16KB+(flash_size-16KB)/2) // pointing to the middle of the flash space after headers

else // high region is active

next_FARB = 16KB // Pointing after headers

2 Make sure that next desired active region content size is <= (flash_size-16KB)/2 ; abort otherwise

3 Program the next desired active region content starting at next_FARB offset

4 Program the other (non-active) header's FARB to point to next_FARB

5 Erase the active header sector

6 New image will be used starting from the next LC domain power-cycle

3.6 Flash Active Region Byte Description

Note: updates are expected in this section.

See Table 16.

Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x0000	to 0x0001	Bytes to Read [7:0]	Length of digital configuration (number of Bytes, not including self)	N/A

Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x0001	to 0x0001	Bytes to Read [15:8]	Length of digital configuration (number of Bytes, not including self)	N/A
0x0002	0	Read DP IN Ucode	0: Don't read ucode patch for DP in 1: Read ucode patch for DP in	N/A
0x0002	1	Read DP Out Ucode	0: Don't read ucode patch for DP out 1: Read ucode patch for DP out	N/A
0x0002	2	Read Ctrl Ucode	0: Don't read ucode patch for ctrl_port 1: Read ucode patch for ctrl_port	N/A
0x0002	3	Read ARC ucode	0: Don't read ucode patch for ARC 1: Read ucode patch for ARC	N/A
0x0002	4	Read CLC ucode	0: Don't read ucode patch for CLC 1: Read ucode patch for CLC	N/A
0x0002	5	Read CIO_0 Ana iram ucode	0: Don't read ucode patch for CIO ana iram 1: Read ucode patch for CIO ana iram	N/A
0x0002	6	Read CIO_1 Ana dram ucode	0: Don't read ucode patch for CIO ana dram 1: Read ucode patch for CIO ana dram	N/A
0x0002	7	Read CIO_2 Ana dram ucode	0: Don't read ucode patch for CIO ana dram 1: Read ucode patch for CIO ana dram	N/A
0x0003	to 0x0004	Ucode Start Address [7:0]	Base address (in Bytes) from which the ucode to the ctrl_port is being read (in bytes, points to the size field).	N/A
0x0004	to 0x0004	Ucode Start Address [15:8]	Base address (in Bytes) from which the ucode to the ctrl_port is being read (in bytes, points to the size field).	N/A
0x0005	to 0x0007	Used for SW	DeviceID, SI Stepping	
0x0006	to 0x0007	Used for SW	DeviceID, SI Stepping	
0x0007	to 0x0007	Used for SW	DeviceID, SI Stepping	
0x0008	to 0x000A	Eeprom Revision [7:0]	EEPROM Revision. See datasheet for field decoding.Not used by hw.	N/A
0x0009	to 0x000A	Eeprom Revision [15:8]	EEPROM Revision. See datasheet for field decoding.Not used by hw.	N/A
0x000A	0x000A	Eeprom Revision [23:16]	EEPROM Revision. See datasheet for field decoding.Not used by hw.	N/A
0x000B	[7:0]	ee_cp_control	Generic configuration bits for CP See Top Level MAS for details	EEC[16:9]
0x000C	to 0x000E	Reserved	Reserved	N/A
0x000D	to 0x000E	Reserved	Reserved	N/A
0x000E	to 0x000E	Reserved	Reserved	N/A
0x000F	[7:0]	Reserved	Reserved	N/A
0x0010	0	Disables MSI-x capability	0: MSI-X supported 1: MSI-X is disabled	N/A
0x0010	1	Router/Switch Config	0: chip is in switch/endpoint configuration 1: chip is in Host Router configuration	DFT1[7]
0x0010	2	Reserved	Reserved	N/A
0x0010	3	PCIe Lanes Mode	0: 4 x1 - 4 Endpoints, one lane each 1: 1 x4 - 1 Endpoint of four lanes	N/A

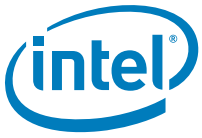


Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x0010	4	Sel Gen2 De-emphasis	0: de-emphasis setting is -6dB. 1: de-emphasis setting is -3.5dB.	N/A
0x0010	5	Reserved	Reserved	N/A
0x0010	6	CIO Ctrl Rst Req Dis	0: cio ctrl reset request is enabled 1: cio ctrl reset request is disabled	N/A
0x0010	7	Reserved	Reserved	N/A
0x0011	[7:0]	Reserved	Reserved	N/A
0x0012	[5:0]	Reserved	Reserved	N/A
0x0012	6	CIO Null Sel Pre Resume	Minimum period of LSLE pin to be low before driving a resume pulse. 0: 2us 1: 15us	N/A
0x0012	7	Enable DMA	0: DMA is gated 1: DMA is enabled	N/A
0x0013	0	ee_pcie_clk_stable	0: pcie_clocks are gated 1: pcie_clocks are ungeted.	N/A
0x0013	1	CIO Perst Pwgd Sel	0: power_good only 1: power_good && perst_n	N/A
0x0013	2	PCIe Perst Pwgd Sel	0: power_good only 1: power_good && perst_n	N/A
0x0013	3	TMU Perst Pwgd Sel	0: power_good only 1: power_good && perst_n	N/A
0x0013	4	HDP IN 1 PWDN	1: HDPI_1 is disabled 0: HDPI_1 port is enabled	N/A
0x0013	5	HDP IN 0 PWDN	1: HDPI_0 is disabled 0: HDPI_0 port is enabled	N/A
0x0013	6	HDPO PWDN	1: HDPO is disabled 0: HDPO port is enabled	N/A
0x0013	7	PCIe PLL Powerdown	0: PCIE active 1: PCIE not active	N/A
0x0014	[7:0]	Reserved	Reserved	N/A
0x0015	[6:0]	Reserved	Reserved	N/A
0x0015	7	ee_tl_rx_flow_ctrl_cb	When 1 will cancel tl rx flow control fix	N/A
0x0016	[6:0]	Reserved	Reserved	N/A
0x0016	7	Flash Clock Full Frequency Enable	Enables usage of full frequency for car_eep_clock. Disabled on reset. Effective in CAR after eep_done (digital section load). 0: car_eep_clk = poc_osc_50_clk/2 1: car_eep_clk = poc_osc_50_clk	N/A
0x0017	[7:0]	Reserved	Reserved	N/A
0x0018	[7:0]	US Port	Upstream Port. Bit 6 Reserved. Bit 7 is load enable.	DEVICE_CS_1[13:8]
0x0019	0	Credit Sync TX Disable	0: SYNC packets are sent by spec 1: SYNC packets are NOT sent at all	DFT1[0]

Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x0019	1	Tar Timeout Disable	0: Tartget bus transaction will auto-ack in 1msec 1: Target bus will wait for ack forever	DFT1[1]
0x0019	[6:2]	Plug Event Control	Functionality (per bit): 0. When set to 1, enables full plug events mechanism, including HDP ports. When 0, uses legacy LR implementation (CIO only) 1. if bit[0]=0 Disable plug events from CIO Port#1 (LR); if bit[0]=1 Disable plug events from any CIO null Port (1,2,3,4) 2. if bit[0]=0 Disable plug events from CIO Port#2 (LR); if bit[0]=1 Disable plug events from HDP#10 3. if bit[0]=0 Disable plug events from CIO Port#3 (LR); if bit[0]=1 Disable plug events from HDP#11 4. if bit[0]=0 Disable plug events from CIO Port#4 (LR); if bit[0]=1 Disable plug events from HDP#12	DFT1[6:2]
0x0019	7	Ctrl Ignore CRC	0: Regular mode 1: Control Port will ignore CRC result and process the packet	N/A
0x001A	[5:0]	CIO Null Phy RX Active Delay	Indicate the delay between LSOE rise and rx analog phy when exiting from CL1	N/A
0x001A	6	CIO Null Dis TL Clk Gate	Disable clock gating to cio transport layer; this will be 1 for power on only	N/A
0x001A	7	Disable Self Teardown	When set to 1, disables "self-teardown" by hardware as described in enable/disable flows in Top Level MAS	N/A
0x001B	0	PCIe Ad5 Rst Req Dis	0: pcie ADP5 reset request is enabled 1: pcie ADP5 reset request is disabled	N/A
0x001B	1	PCIe EP Rst Req Dis	0: pcie EP reset request is enabled 1: pcie EP reset request is disabled	N/A
0x001B	2	Security Enable	default SV image will change strapping of the security option	N/A
0x001B	3	PCIe L0 Rst Req Dis	0: pcie_l0 reset request is enabled 1: pcie_l0 reset request is disabled	N/A
0x001B	4	PCIe L1 Rst Req Dis	0: pcie_l1 reset request is enabled 1: pcie_l1 reset request is disabled	N/A
0x001B	5	PCIe L2 Rst Req Dis	0: pcie_l2 reset request is enabled 1: pcie_l2 reset request is disabled	N/A
0x001B	6	PCIe L3 Rst Req Dis	0: pcie_l3 reset request is enabled 1: pcie_l3 reset request is disabled	N/A
0x001B	7	No Port Error Event	0: Regular mode 1: Control Port will not generate error events with codes 1, 12, 13	N/A
0x001C	[2:0]	Reserved	Reserved	N/A
0x001C	3	CIO Dis FC Timer	0: default per spec 1: disable periodic CIO FC grant updates	N/A

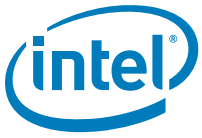


Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x001C	4	ee_pcie_two_low_lanes	0: Lanes 0,1 are 2x1 1: Lanes 0,1 are 1x2	N/A
0x001C	5	ee_pcie_two_high_lanes	0: Lanes 2,3 are 2x1 1: Lanes 2,3 are 1x2	N/A
0x001C	6	Ctrl Ignore FC	When set, CP will ignore credits check when sending control packets	N/A
0x001C	7	Reserved	Reserved	N/A
0x001D	[7:0]	Reserved	Reserved	N/A
0x001E	0	CIO Null Dis Hec Err Retrain	0: CIO port will retrain link upon hec error 1: CIO port won't retrain link upon hec error	N/A
0x001E	1	CIO Null Force Connected	0: CIO port will behave normally 1: CIO port will skip connect detection	N/A
0x001E	2	CIO Null Force Link Up	0: CIO port will behave normally 1: CIO port will skip training	N/A
0x001E	[7:3]	CIO Null Min Os Size	Number of min OS to send in link FSM	N/A
0x001F	[2:0]	CIO Null Num RX Connect Pulse	Specify amount of connect pulses to decide on connected state	N/A
0x001F	[5:3]	Reserved	Reserved	N/A
0x001F	[7:6]	Delay to read next data for ANA section	Specify the delay before next strobe to ana regs. Supposing 100 MHz oscillator clock - d0: 0.80 us d1: 0.96 us d2: 1.12 us d3: 1.28 us	N/A
0x0020	to 0x0021	TMU TX Time To Wire Port 1 [7:0]	Specify the time duration between the instant the timestamp is taken and when the first bit of the TSNOS is received/transmitted on the wire.	port 1, TMU_PORT_CS_1 [27:16]
0x0021	to 0x0021	TMU TX Time To Wire Port 1 [11:8]	Specify the time duration between the instant the timestamp is taken and when the first bit of the TSNOS is received/transmitted on the wire.	port 1, TMU_PORT_CS_1 [27:16]
0x0021	7:4	Reserved	Reserved	N/A
0x0022	to 0x0023	TMU TX Time To Wire Port 2 [7:0]	Specify the time duration between the instant the timestamp is taken and when the first bit of the TSNOS is received/transmitted on the wire.	port 2, TMU_PORT_CS_1 [27:16]
0x0023	to 0x0023	TMU TX Time To Wire Port 2 [11:8]	Specify the time duration between the instant the timestamp is taken and when the first bit of the TSNOS is received/transmitted on the wire.	port 2, TMU_PORT_CS_1 [27:16]
0x0023	[6:4]	cl1 exit period scale	value for RO phy reg CL1 exit period scale	
0x0023	7	ee_cio_null_port_c_cio_1_hdpin_1	select cio or hdpin mode port C	
0x0024	to 0x0025	TMU TX Time To Wire Port 3 [7:0]	Specify the time duration between the instant the timestamp is taken and when the first bit of the TSNOS is received/transmitted on the wire.	port 3, TMU_PORT_CS_1 [27:16]

Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x0025	to 0x0025	TMU TX Time To Wire Port 3 [11:8]	Specify the time duration between the instant the timestamp is taken and when the first bit of the TSNOS is received/transmitted on the wire.	port 3, TMU_PORT_CS_1 [27:16]
0x0025	[6:4]	cl2 exit period scale	value for RO phy reg CL2 exit period scale	
0x0025	7	Reserved	Reserved	N/A
0x0026	to 0x0027	Reserved	Reserved	N/A
0x0027	to 0x0027	Reserved	Reserved	N/A
0x0027	4	ee_tmu_enable_uni_mode_1	Enable TMU uni directional mode for PA	
0x0027	5	ee_tmu_enable_uni_mode_2	Enable TMU uni directional mode for PB	
0x0027	6	ee_tmu_enable_uni_mode_3	Enable TMU uni directional mode for PC	
0x0027	7	ee_pcie_phy_core_stable_legacy1_new0	new feature to enable pcie clks when no PLL to work on 100Mhz poc clk. "1" - legacy - "0" new mode if stable=1 --> PCIE PLL, if stable =0 -> 100 POC	N/A
0x0028	0x0028	TMU RX Time To Wire Port 1 [7:0]	Specify the time duration between the instant the timestamp is taken and when the first bit of the TSNOS is received/transmitted on the wire.	port 1, TMU_PORT_CS_2 [27:16]
0x0029	0x0029	TMU RX Time To Wire Port 1 [11:8]	Specify the time duration between the instant the timestamp is taken and when the first bit of the TSNOS is received/transmitted on the wire.	port 1, TMU_PORT_CS_2 [27:16]
0x0029	4	ee_car_cio_usb_hs_div_visa_cb	chicken bits to enable visa on high speed clks, those clks are divided from original freq to be able to reflect on digital IO. "1" enable", 0" - module in rst	
0x0029	5	ee_car_pcie_hs_div_visa_cb	chicken bits to enable visa on high speed clks, those clks are divided from original freq to be able to reflect on digital IO. "1" enable", 0" - module in rst	
0x0029	6	ee_car_tmu_hs_div_visa_cb	chicken bits to enable visa on high speed clks, those clks are divided from original freq to be able to reflect on digital IO. "1" enable", 0" - module in rst	
0x0029	7	ee_car_cio_usb_legacy_500_pll_en	chicken bit to enable usb gen1 to work w/ legacy 500Mhz PLL instead of using div5 from 625 pll	
0x002A	to 0x002B	TMU RX Time To Wire Port 2 [7:0]	Specify the time duration between the instant the timestamp is taken and when the first bit of the TSNOS is received/transmitted on the wire.	port 2, TMU_PORT_CS_2 [27:16]
0x002B	to 0x002B	TMU RX Time To Wire Port 2 [11:8]	Specify the time duration between the instant the timestamp is taken and when the first bit of the TSNOS is received/transmitted on the wire.	port 2, TMU_PORT_CS_2 [27:16]
0x002B	[7:4]	ee_hdp_in_swizzle_en	changing the order of bits as they go out to the phy MSB<->LSB	

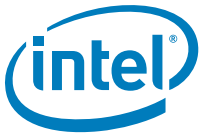


Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x002C	to 0x002D	TMU RX Time To Wire Port 3 [7:0]	Specify the time duration between the instant the timestamp is taken and when the first bit of the TSNOS is received/transmitted on the wire.	port 3, TMU_PORT_CS_2 [27:16]
0x002D	to 0x002D	TMU RX Time To Wire Port 3 [11:8]	Specify the time duration between the instant the timestamp is taken and when the first bit of the TSNOS is received/transmitted on the wire.	port 3, TMU_PORT_CS_2 [27:16]
0x002D	[3:0]	ee_cio_null_max_link_speed	use to reduce max link speed capability	cio phy
0x002E	to 0x002F	Reserved	Reserved	N/A
0x002F	to 0x002F	Reserved	Reserved	N/A
0x002F	4	DP_IN Enhanced-Framing capability	DP_IN Enhanced-Framing capability: 0: no supported 1: supported	
0x002F	5	DP_OUT Enhanced-Framing capability	DP_OUT Enhanced-Framing capability: 0: no supported 1: supported	
0x002F	6	DP_IN TPS3 capability	DP_IN TPS3 capability: 0: no supported 1: supported	
0x002F	7	DP_OUT TPS3 capability	DP_OUT TPS3 capability: 0: no supported 1: supported	
0x0030	[7:0]	HDMI In Frequency restoration control	Controls parameters in TMU_HDMI_IN	N/A
0x0031	[7:0]	HDMI Out Frequency restoration control	Controls parameters in TMU_HDMI_OUT	N/A
0x0032	[7:0]	HDMI Out Frequency restoration control	Controls parameters in TMU_HDMI_OUT	N/A
0x0033	[7:0]	DP pre-emphasis initial values	[1:0] – initial pre-emphasis to request from GPU at speed of 1.62GHz [3:2] – initial pre-emphasis to request from GPU at speed of 2.7GHz [5:4] – initial pre-emphasis to request from GPU at speed of 5.4GHz [7:6] – reserved	Reg in DP IN 8051 subsystem space. Address 0xc828,c829,c82a,c82b[1:0]
0x0034	[7:0]	DP swing initial values	[1:0] – initial swing to request from GPU at speed of 1.62GHz [3:2] – initial swing to request from GPU at speed of 2.7GHz [5:4] – initial swing to request from GPU at speed of 5.4GHz [7:6] – reserved	Reg in DP IN 8051 subsystem space. Address 0xc828,c829,c82a,c82b[3:2]

Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x0035	[7:0]	reserved for pa/pb use. Default 0 [5:4] determines iecs lane_en for pa of a dpd working as bus powered (when working self powered, value is according to ~ee_clc_lane_disabled)	Reserved	DEV.SEC6.CHICKEN_BITS
0x0036	[7:0]	reserved for pa/pb use. Default 0 [5:4] determines iecs lane_en for pa of a dpd working as bus powered (when working self powered, value is according to ~ee_clc_lane_disabled)	Reserved	DEV.SEC6.CHICKEN_BITS
0x0037	[6:0]	I2C_Slave ID	7-bit address for slave ID	N/A
0x0037	7	CIO SW Extended bus mode	When 1 cause TLs and cio switch working in extended buss mode	N/A
0x0038	to 0x39	part of port micro uuid register	value is read in port micro register 6	DEV.SEC6.UUID3[7:0]
0x0039	to 0x39	part of port micro uuid register	value is read in port micro register 6	DEV.SEC6.UUID3[15:8]
0x003A	[6:0]	port micro HVReq[6:0] register	value is read in port micro register 15	DEV.SEC6.HVREQ[6:0]
0x003A	7	Reserved	Reserved	N/A
0x003B	[7:0]	reserved for pa/pb use. Default 0	Reserved	DEV.SEC6.CHICKEN_BITS
0x003C	[7:0]	ee_arc_config	Configuration bits for ARC subsystem	ARC Memory mapped register (EE_ARC_CONFIG[7:0])
0x003D	[7:0]	ee_arc_config	Configuration bits for ARC subsystem	ARC Memory mapped register (EE_ARC_CONFIG[15:8])
0x003E	[7:0]	ee_arc_config	Configuration bits for ARC subsystem	ARC Memory mapped register (EE_ARC_CONFIG[23:16])
0x003F	[7:0]	ee_arc_config	Configuration bits for ARC subsystem	ARC Memory mapped register (EE_ARC_CONFIG[31:24])
0x0040	0	TMU Disable 1G Sync	0: Sampling on 1g frequency is enabled 1: Sampling on 125M is enabled	N/A
0x0040	1	TMU Serial Mode is Slave	0: TMU serial interface acts as master 1: TMU serial interface acts as slave	N/A

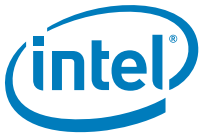


Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x0040	2	TMU Disable All Traffic	0: TMU will work normally 1: TMU will not send any traffic	N/A
0x0040	3	TMU Disable DP Ssc	0: Enable support of SCC in DP 1: Disable support of SCC in DP	N/A
0x0040	4	TMU Disable Port 1	0: TMU port # will work normally 1: TMU port # will not send sync packets	N/A
0x0040	5	TMU Disable Port 2	0: TMU port # will work normally 1: TMU port # will not send sync packets	N/A
0x0040	6	TMU Disable Port 3	0: TMU port # will work normally 1: TMU port # will not send sync packets	N/A
0x0040	7	Reserved	Reserved	N/A
0x0041	[5:0]	Reserved	Reserved	N/A
0x0041	6	ee_gtc_disable_freq_calc	0: Do the frequency offset adjustment in GTC 1: Don't do the frequency offset adjustment in GTC	N/A
0x0041	7	ee_gtc_disable_gtc_modify	0: Do the GTC compensation calc 1: Don't change the GTC. Pass it as is	N/A
0x0042	[5:0]	Reserved	Reserved	N/A
0x0042	6	ee_iram_always_rd_en_cb	Always assert read_en to dp_8051 inrenal RAM	N/A
0x0042	7	CIO Null Dis Scrambling	When set to 1, disables scrambling for debug	N/A
0x0043	[5:0]	Reserved	Reserved	N/A
0x0043	[7:6]	USB source reset control	0: PCIE Reset + HotReset + LinkDown + D3 to D0 1: PCIE Reset + HotReset + LinkDown 2:PCIE Reset + D3 to D0 3:PCIE Reset	N/A
0x0044	[7:0]	Reserved	Reserved	N/A
0x0045	[2:0]	FLASH size coded	Defines FLASH size as follows: Value Memory size, Mb 0x0 1 0x1 2 0x2 4 … … 0x6 64	N/A
0x0045	[5:3]	Reserved	Reserved	N/A
0x0045	6	ee_cio_phy_halt_on_reset_pa	cause the cio controller wake on halt state allowing control from debugger	
0x0045	7	ee_cio_phy_halt_on_reset_pb	cause the cio controller wake on halt state allowing control from debugger	
0x0046	[7:0]	Reserved	Reserved	N/A
0x0047	[7:0]	Reserved	Reserved	N/A
0x0048	[7:0]	Reserved for pa/pb use. Default 0	Reserved	DEV.SEC6.CHICKEN_BITS
0x0049	1	Stand Alone (under Router)	1’b1 – Stand Alone	

Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x0049	1	USB Only (no PCIE Switch)	1'b0 – USB Only	
0x0049	[3:2]	Limit lane width of Physical Up/ Dn	2'b0 – x1 2'b1 – x2 2'b2 – x4	
0x0049	[5:4]	Rate Capability (Switch / CIO)	2'b0 – Gen1 2'b1 – Gen2 2'b2 – Gen3	
0x0049	[7:6]	Rate Capability (Endpoints)	2'b0 – Gen1 2'b1 – Gen2 2'b2 – Gen3	
0x004A	0	HDP OUT type select	0: DP, 1: HDMI	HDP vendor specific register in adapter. Port#10 Offset 0x6e, bit 0
0x004A	1	ee_hdp_hdmi1_dp0_h1	0: DP, 1: HDMI	HDP vendor specific register in adapter. Port#11 Offset 0x6e, bit 0
0x004A	2	HDP OUT HDMI capability	0: HDMI not supported, 1: supported	HDP vendor specific register in adapter. Port#10 Offset 0x6e, bit 2
0x004A	3	HDP OUT DP capability	0: DP not supported, 1: supported	HDP vendor specific register in adapter. Port#10 Offset 0x6e, bit 1
0x004A	4	HDP IN #0 HDMI capability	0: HDMI not supported, 1: supported	HDP vendor specific register in adapter. Port#11 Offset 0x6e, bit 2
0x004A	5	HDP IN #0 DP capability	0: DP not supported, 1: supported	HDP vendor specific register in adapter. Port#11 Offset 0x6e, bit 1
0x004A	6	ee_dont_discard_control_packet	this bit is XOR'ed with dont_discard_control_packet DMA MISC bit (which defaults to 1). This EEPROM bit should be set to 1 if Swless is enabled.	N/A
0x004A	7	Reserved	Reserved	N/A
0x004B	0	HDP IN #1 type select	0: DP, 1: HDMI	HDP vendor specific register in adapter. Port#12 Offset 0x6e, bit 0
0x004B	1	HDP IN #1 HDMI capability	0: HDMI not supported, 1: supported	HDP vendor specific register in adapter. Port#12 Offset 0x6e, bit 2

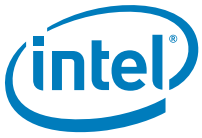


Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x004B	2	HDP IN #1 DP capability	0: DP not supported, 1: supported	HDP vendor specific register in adapter. Port#12 Offset 0x6e, bit 1
0x004B	3	ee_dp_out_tps4_cap	Advertise capability of test pattern 4 for TR for DP rev 1.4	EE_CAP_3
0x004B	4	ee_dp_in_tps4_cap	Advertise capability of test pattern 4 for TR for DP rev 1.4	EE_CAP_3
0x004B	[7:5]		Reserved	N/A
0x004C	to 0x004F	GPIO Ownership configuration	2 bits per GPIO pin 00 : Control Port 01 : HardwareControlled (custom) 10 : Link Controller Port A 11 : Link Controller Port B	DEV.SEC6.GPIO_OWN_CTRL_LOW[7:0]
0x004D	to 0x004F	GPIO Ownership configuration	2 bits per GPIO pin 00 : Control Port 01 : HardwareControlled (custom) 10 : Link Controller Port A 11 : Link Controller Port B	DEV.SEC6.GPIO_OWN_CTRL_LOW[15:8]
0x004E	to 0x004F	GPIO Ownership configuration	2 bits per GPIO pin 00 : Control Port 01 : HardwareControlled (custom) 10 : Link Controller Port A 11 : Link Controller Port B	DEV.SEC6.GPIO_OWN_CTRL_HIGH[7:0]
0x004F	to 0x004F	GPIO Ownership configuration	2 bits per GPIO pin 00 : Control Port 01 : HardwareControlled (custom) 10 : Link Controller Port A 11 : Link Controller Port B	DEV.SEC6.GPIO_OWN_CTRL_HIGH[15:8]
0x0050	[5:0]	MAX CIO Link Width	carry the max link width of cio link	N/A
0x0050	6	EE Read Arbiter Mode	Controls arbitration mode of ee_read_arbiter 0:round-robin (default), 1:strict;	
0x0050	7	Target Bus Arbiter Mode	Controls arbitration mode of target_bus_arbiter 0:round-robin (default), 1:strict;	
0x0051	[7:0]	reserved for pa/pb use. Default 0	Reserved	DEV.SEC6.CHICKEN_BITS
0x0052	[7:0]	reserved for pa/pb use. Default 0	Reserved	DEV.SEC6.CHICKEN_BITS
0x0053	[1:0]	Reserved	Reserved	N/A
0x0053	2	Connector type optical / electrical	When 1 indicates that the connector type of port A is optical, when 0 indicate that the connector type is electrical	DEV.SEC6.GENERAL[1]
0x0053	3	Connector type optical / electrical	When 1 indicates that the connector type of port B is optical, when 0 indicate that the connector type is electrical	DEV.SEC6.GENERAL[1]

Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x0053	[5:4]	board power source	1=BPD (bus powered device) 2=SPD (self powered device) 3=DPD (dual powered device)	DEV.SEC6.GENERAL[9:8]
0x0053	6	Reserved	Reserved	N/A
0x0053	7	Force TAP legacy mode	Forces TAP to work in legacy mode, mTAP and TAP network are disabled.	N/A
0x0054	0	Reserved	Reserved	N/A
0x0054	1	ee_pa_hdp_pwdn	1: HDP logic at portA is disabled 0: HDP logic at portA is enabled	N/A
0x0054	2	ee_pb_hdp_pwdn	1: HDP logic at portB is disabled 0: HDP logic at portB is enabled	N/A
0x0054	3	ee_cio_null_use_single_seed	Cause all lanes of multi-lane link to use the same scrambler initial seed	N/A
0x0054	4	indicate that the device is in tethered cable	When 1 disable controller FW driving the external MUXes GPIO	DEV.SEC6.GENERAL[5]
0x0054	5	Enable port A	When 1 enable port A	DEV.SEC6.GENERAL[4]
0x0054	6	Indicate that the device is in tethered cable	When 1 disable controller FW driving the external MUXes GPIO	DEV.SEC6.GENERAL[5]
0x0054	7	Enable port B	When 1 enable port A	DEV.SEC6.GENERAL[4]
0x0055	[7:0]	snk1_dp_swap	Lanes swap for snk1 in dp mode No swapping means, swap = {3,2,1,0} = 0b11_10_01_00 = 0xe4	N/A
0x0056	[7:0]	Reserved	Reserved	N/A
0x0057	[7:0]	snk2_dp_swap	Lanes swap for snk2 in dp mode No swapping means, swap = {3,2,1,0} = 0b11_10_01_00 = 0xe4	N/A
0x0058	[7:0]	Reserved	Reserved	N/A
0x0059	[7:0]	pa_dp_swap	Lanes swap for pa in dp mode No swapping means, swap = {3,2,1,0} = 0b11_10_01_00 = 0xe4	N/A
0x005A	[7:0]	Reserved	Reserved	N/A
0x005B	[7:0]	pb_dp_swap	Lanes swap for pb in dp mode No swapping means, swap = {3,2,1,0} = 0b11_10_01_00 = 0xe4	N/A
0x005C	[7:0]	Reserved	Reserved	N/A
0x005D	[7:0]	src_dp_swap	Lanes swap for src in dp mode No swapping means, swap = {3,2,1,0} = 0b11_10_01_00 = 0xe4	N/A
0x005E	0	snk1_ee_dp_aux_np_swap	causes the inversion of N and P pins of the DP AUX	N/A
0x005E	1	snk2_ee_dp_aux_np_swap	causes the inversion of N and P pins of the DP AUX	N/A
0x005E	2	pc_ee_dp_aux_np_swap	causes the inversion of N and P pins of the DP AUX	N/A

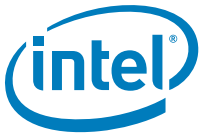


Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x005E	3	src_pa_ee_dp_aux_np_swap	causes the inversion of N and P pins of the DP AUX	N/A
0x005E	4	src_pb_ee_dp_aux_np_swap	causes the inversion of N and P pins of the DP AUX	N/A
0x005E	5	HDP OUT type select	0: DP, 1: HDMI	HDP vendor specific register in adapter. Port#10 Offset 0x6e, bit 0
0x005E	6	HDP OUT HDMI capability	0: HDMI not supported, 1: supported	HDP vendor specific register in adapter. Port#10 Offset 0x6e, bit 2
0x005E	7	HDP OUT DP capability	0: DP not supported, 1: supported	HDP vendor specific register in adapter. Port#10 Offset 0x6e, bit 1
0x005F	[1:0]	snk1_hdp_clk_select	1..0 – clock select for snk1 (debug)	Reg in DP IN 8051 subsystem space. Address 0xcc06[1:0]
0x005F	[3:2]	snk2_hdp_clk_select	3..2 – clock select for snk2 (debug)	Reg in DP IN 8051 subsystem space. Address 0xcc06[1:0]
0x005F	[5:4]	cio null LS duration	When 00 - normal speed (long duration) When 01 - set LS speed level 1 - for simulating mDP mode When 10 - set LS speed level 2 - for simulating legacy mode with optic device When 11 - set LS speed level 3 - for simulating legacy mode w/o optic device	N/A
0x005F	6	Reserved	Reserved	N/A
0x005F	7	force waking cio domain on first power on	When 1 force waking cio domain on first power on	DEV.SEC6.GENERAL[12]
0x00060	[4:0]	ee_scratch_gen_poll_timer[4:0]	this timer used to configure the polling time need when using generic_fsm for status bit (BUSY) of flash. The resolution is 100us multplay by this setting.	N/A
0x0060	5	forc cio power on force power wake	Controls whether LC will power on the cio domain upon assertion of gpio3_force_pwr. 0 – will not power on 1 – will power on	DEV.SEC6.GENERAL[13]
0x0060	6	ee_cio_null_1x10_cb	cancel physical layer 2x10 changes	
0x0060	7	ee_tmu_pll_calibration_disable	option to disable tmu_pll calibration - "1" - disable, "0" enable	NA
0x0061	to 0x0063	ee_clc_vendor_id	This 24-bit IEEE OUI for the vendor. For Apple reg0.	DEV.SEC6.VENDOR_ID[7:0]
0x0062	to 0x0063	ee_clc_vendor_id	This 24-bit IEEE OUI for the vendor. For Apple reg0.	DEV.SEC6.VENDOR_ID[15:8]

Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x0063	to 0x0063	ee_clc_vendor_id	This 24-bit IEEE OUI for the vendor. For Apple reg0.	DEV.SEC6.VENDOR_ID[23:16]
0x0064	to 0x0067	ee_clc_device_id	Vendor specific but it is recommended that it be unique between different classes of devices (ie 1m cable vs 2m cable). For Apple reg1.	DEV.SEC6.DEVICE_ID[7:0]
0x0065	to 0x0067	ee_clc_device_id	Vendor specific but it is recommended that it be unique between different classes of devices (ie 1m cable vs 2m cable). For Apple reg1.	DEV.SEC6.DEVICE_ID[15:8]
0x0066	to 0x0067	ee_clc_device_id	Vendor specific but it is recommended that it be unique between different classes of devices (ie 1m cable vs 2m cable). For Apple reg1.	DEV.SEC6.DEVICE_ID[23:16]
0x0067	to 0x0067	ee_clc_device_id	Vendor specific but it is recommended that it be unique between different classes of devices (ie 1m cable vs 2m cable). For Apple reg1.	DEV.SEC6.DEVICE_ID[31:24]
0x0068	to 0x006B	ee_clc_protocol_version	IECS Protocol Version. Required to be 1. For Apple reg2.	DEV.SEC6.PROTOCOL_VERSION[7:0]
0x0069	to 0x006B	ee_clc_protocol_version	IECS Protocol Version. Required to be 1. For Apple reg2.	DEV.SEC6.PROTOCOL_VERSION[15:8]
0x006A	to 0x006B	ee_clc_protocol_version	IECS Protocol Version. Required to be 1. For Apple reg2.	DEV.SEC6.PROTOCOL_VERSION[23:16]
0x006B	to 0x006B	ee_clc_protocol_version	IECS Protocol Version. Required to be 1. For Apple reg2.	DEV.SEC6.PROTOCOL_VERSION[31:24]
0x006C	to 0x006F	ee_clc_mode	This field is a 4CC and used to indicate if the device is operating properly. 'APP ' – Indicates the device is fully functioning and will implement all the features advertised by the type field. Any other value indicates the device is functioning in a limited capacity and any action required is vendor specific. For Apple reg3.	DEV.SEC6.MODE[7:0]
0x006D	to 0x006F	ee_clc_mode	This field is a 4CC and used to indicate if the device is operating properly. 'APP ' – Indicates the device is fully functioning and will implement all the features advertised by the type field. Any other value indicates the device is functioning in a limited capacity and any action required is vendor specific. For Apple reg3.	DEV.SEC6.MODE[15:8]
0x006E	to 0x006F	ee_clc_mode	This field is a 4CC and used to indicate if the device is operating properly. 'APP ' – Indicates the device is fully functioning and will implement all the features advertised by the type field. Any other value indicates the device is functioning in a limited capacity and any action required is vendor specific. For Apple reg3.	DEV.SEC6.MODE[23:16]

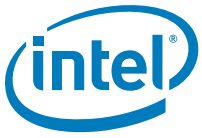


Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x006F	to 0x006F	ee_clc_mode	This field is a 4CC and used to indicate if the device is operating properly. 'APP ' – Indicates the device is fully functioning and will implement all the features advertised by the type field. Any other value indicates the device is functioning in a limited capacity and any action required is vendor specific. For Apple reg3.	DEV.SEC6.MODE[31:24]
0x0070	to 0x0073	ee_clc_type	A 4CC either 'EM ', 'CM ', or 'ECM '. For Apple reg4.	DEV.SEC6.TYPE[7:0]
0x0071	to 0x0073	ee_clc_type	A 4CC either 'EM ', 'CM ', or 'ECM '. For Apple reg4.	DEV.SEC6.TYPE[15:8]
0x0072	to 0x0073	ee_clc_type	A 4CC either 'EM ', 'CM ', or 'ECM '. For Apple reg4.	DEV.SEC6.TYPE[23:16]
0x0073	to 0x0073	ee_clc_type	A 4CC either 'EM ', 'CM ', or 'ECM '. For Apple reg4.	DEV.SEC6.TYPE[31:24]
0x0074	[7:0]	Reserved	Reserved	N/A
0x0075	to 0x00078	ee_arc_ee_base	ARC: Loaded into EEBASE - ARC EE Region base	ARC Memory mapped register (EEBASE[7:0])
0x0076	to 0x00078	ee_arc_ee_base	ARC: Loaded into EEBASE - ARC EE Region base	ARC Memory mapped register (EEBASE[15:8])
0x0077	to 0x00078	ee_arc_ee_base	ARC: Loaded into EEBASE - ARC EE Region base	ARC Memory mapped register (EEBASE[23:16])
0x00078	to 0x00078	ee_arc_ee_base	ARC: Loaded into EEBASE - ARC EE Region base	ARC Memory mapped register (EEBASE[31:24])
0x00079	to 0x0007C	ee_arc_ee_straps	Loaded into EESTRAPS – Config bits from EEPROM	ARC Memory mapped register (EESTAPS[7:0])
0x0007A	to 0x0007C	ee_arc_ee_straps	Loaded into EESTRAPS – Config bits from EEPROM	ARC Memory mapped register (EESTAPS[15:8])
0x0007B	to 0x0007C	ee_arc_ee_straps	Loaded into EESTRAPS – Config bits from EEPROM	ARC Memory mapped register (EESTAPS[23:16])
0x0007C	to 0x0007C	ee_arc_ee_straps	Loaded into EESTRAPS – Config bits from EEPROM	ARC Memory mapped register (EESTAPS[31:24])
0x0007D	to 0x00080	ee_arc_dpin_ssc	Loaded into DPIN0CFG – DPIN0 parameters	N/A
0x0007E	to 0x00080	ee_arc_dpin_ssc	Loaded into DPIN0CFG – DPIN0 parameters	N/A
0x0007F	to 0x00080	ee_arc_dpin_ssc	Loaded into DPIN0CFG – DPIN0 parameters	N/A
0x00080	to 0x00080	ee_arc_dpin_ssc	Loaded into DPIN0CFG – DPIN0 parameters	N/A
0x00081	[3:0]	ee_arc_plugevent_gpio	Loaded into PLUGEVENTCFG – plug event configuration (default GPIO_5__CIO_PLUG_EVENT)	ARC Memory mapped register (PLUGEVENTCFG[3:0])

Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x00081	4	ee_arc_plugevent_on_cio	Loaded into PLUGEVENTCFG – plug event configuration	ARC Memory mapped register (PLUGEVENTCFG[30])
0x00081	5	ee_arc_plugevent_on_pcie	Loaded into PLUGEVENTCFG – plug event configuration	ARC Memory mapped register (PLUGEVENTCFG[31])
0x00081	6	ask Michael	Controls whether DMA (embedded endpoint) will be enabled or disabled. 0 – dma is enabled 1 – dma is disabled	DEV.SEC6.EE_COMMON[8]
0x00081	7	ee_arc_enable	1: ARC is enabled; 0: ARC is kept in reset	ARC Memory mapped register (ARC_DEBUG[0])
0x00082	to 0x00083	ee_arc_plugevent_delay	Loaded into PLUGEVENTCFG – plug event configuration	ARC Memory mapped register (PLUGEVENTCFG[11:4])
0x00083	[3:0]	ee_arc_plugevent_delay	Loaded into PLUGEVENTCFG – plug event configuration	ARC Memory mapped register (PLUGEVENTCFG[15:12])
0x00083	[4:7]	Reserved	Reserved	N/A
0x00084	[5:0]	Reserved	Reserved	N/A
0x00084	6	disable SNK1 aux_n	When 1 disable internal controller controlling the SNK2 aux_n input	DEV.SEC6.AUX_N_CTRL[0]
0x00084	7	disable SNK2 aux_n	When 1 disable internal controller controlling the SNK1 aux_n input	DEV.SEC6.AUX_N_CTRL[2]
0x00085	0	disable UART messages on LS pins	When 1 the LS pins will carry the original LSEO/OE signals (for port A - CIO[1], for port B - CIO[3])	DEV.SEC6.GENERAL[6]
0x00085	[7:1]	Reserved	Reserved	N/A
0x00086	[7:0]	Reserved	Reserved	N/A
0x00087	[7:0]	Reserved	Reserved	N/A
0x00088	[7:0]	ee_gtc_cfg	Chicken bits for GTC	N/A
0x00089	0	ee_ex_flsh_write_protection_enable1_disable0_cb	this signal is used to enable/disable wr_protection feature of external flash - once "1" feature enabled, "0" disable (A0 mode)	N/A
0x00089	1	Reserved	Reserved	
0x00089	2	ee_i2c_master_disable	this bit is used to enable or disable i2c_master module, if "0" i2c master will be enable, if"1" it will disable i2c master functionality	N/A
0x00089	3	XHC EMEP clock dynamic in Host	0 – XHC EMEP clocks are active in Host 1 – XHC EMEP clocks depends on XHC connect in Host	N/A
0x00089	4	ee_scracth_security_en	if "1" - scratch erase/prog is done by HW, if "0" - erase/prog is done by FW.	N/A
0x00089	5	ee_scratch_section_load_enable	decide if to enable scratch section load on power_on "1" - enable, "0"disable	N/A

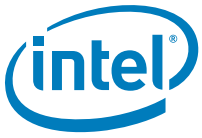


Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x00089	6	Reserved	Reserved	N/A
0x00089	7	ee_i2c_slave_disable	this bit is used to enable or disable i2c_slave module, if "0" i2c slave will be enable, if"1" it will disable i2c slave functionality	N/A
0x008a	to 0x008d	port micro version register	value is read in port micro register 7	DEV.SEC6.VERSION[7:0]
0x008b	to 0x008d	port micro version register	value is read in port micro register 7	DEV.SEC6.VERSION[15:8]
0x008c	to 0x008d	port micro version register	value is read in port micro register 7	DEV.SEC6.VERSION[23:16]
0x008d	to 0x008d	port micro version register	value is read in port micro register 7	DEV.SEC6.VERSION[31:24]
0x008e	[7:0]	General purpose configuration	HPD_Unplug on start. For DFT mode in which an HPD is generated when HPD_PLUG is detected. In DP mode: when set to value X[7:0], other than zero, will force the HPD signal to low for 64*40*X nsec. When 0xc850 is set (both in DP and HDMI mode) will force HPD low for a period of 16*40*X nsec. Not valid in HDMI mode when 0xc850 is zero	Reg in DP IN 8051 subsystem space. Address 0xc848
0x008f	[7:0]	hdp_in_chicken0	When set, FW will disregard hdmi unstable indication from Analog.	Reg in DP IN 8051 subsystem space. Address 0xc849
0x0090	[7:0]	hdp_in_chicken1	Bit 0: when set, prevents requesting a new ADJUST_REQUEST from the GPU if already achieved alignment.	Reg in DP IN 8051 subsystem space. Address 0xc84a
0x0091	[7:0]	General purpose configuration	ee_hdp_in_gp_cfg3[0] (bit zero of EEPROM reg 0x91) should now be: forces DP_IN FW to an eternal loop before waiting for HPD. Can be released by writing register 0xCC92 to value > 3 ([3:1] cause eternal loop in other places)	Reg in DP IN 8051 subsystem space. Address 0xc84b
0x0092	[7:0]	General purpose configuration	For future usage	Reg in DP OUT (P10)8051 subsystem space. Address 0xc848
0x0093	[7:0]	General purpose configuration	For future usage	Reg in DP OUT (P10) 8051 subsystem space. Address 0xc849
0x0094	[7:0]	General purpose configuration	For future usage	Reg in DP OUT (P10) 8051 subsystem space. Address 0xc84a
0x0095	[7:0]	General purpose configuration	ee_hdp_out_gp_cfg3[0] (bit zero of EEPROM reg 0x95) should now be: forces DP_OUT FW to an eternal loop before waiting for HPD. Can be released by writing register 0xCC93 to value > 2 ([2:1] cause eternal loop in other places	Reg in DP OUT (P10) 8051 subsystem space. Address 0xc84b

Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x0096	[7:0]	Low 8b of HDP_IN region	HDP_IN region accessed by HDP_IN (as a master)	Reg in DP IN 8051 subsystem space. Address 0xc84c
0x0097	[7:0]	High 8b of HDP_IN region	HDP_IN region accessed by HDP_IN (as a master)	Reg in DP IN 8051 subsystem space. Address 0xc84d
0x0098	[7:0]	Size of HDP_IN region	HDP_IN region accessed by HDP_IN (as a master)	Reg in DP IN 8051 subsystem space. Address 0xc84e
0x0099	[7:0]	Low 8b of HDP_OUT region	HDP_OUT region accessed by HDP_OUT (as a master)	Reg in DP OUT (P10) 8051 subsystem space. Address 0xc84c
0x009a	[7:0]	High 8b of HDP_OUT region	HDP_OUT region accessed by HDP_OUT (as a master)	Reg in DP OUT (P10) 8051 subsystem space. Address 0xc84d
0x009b	[7:0]	Size of HDP_OUT region	HDP_OUT region accessed by HDP_OUT (as a master)	Reg in DP OUT (P10)8051 subsystem space. Address 0xc84e
0x009c	[7:0]	Descriptor Head	Descriptor Head is the first node in a linked list of registers containing descriptors Byte 0: Register number of next descriptor or 0 to terminate the list Byte 1: Descriptor ID or Descriptor ID Continuation code.	DEV.SEC6.DESCR_HEAD[7:0]
0x009d	[7:0]	Descriptor Head	Descriptor Head is the first node in a linked list of registers containing descriptors Byte 0: Register number of next descriptor or 0 to terminate the list Byte 1: Descriptor ID or Descriptor ID Continuation code.	DEV.SEC6.DESCR_HEAD[15:8]
0x009e	[7:0]	ee_cio_mng_sel_timeout	Select different value for different periods to wait before considering timeout	N/A
0x009f	[7:0]	ee_clc_direct_acc_base	Select the DW offset (from start of the RAM) of memory mapped register area for SW	N/A
0x00A0	[4:0]	ee_clc_direct_acc_base	Select the DW offset (from start of the RAM) of memory mapped register area for SW	N/A
0x00A0	[7:5]	ee_cio_null_cb	general chicken bits	N/A

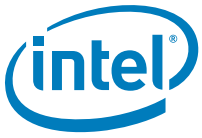


Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x00A1	[7:0]	0-Dn0 Gen1 force 1-Dn1 Gen1 force 2-Dn2 Gen1 force 3-Dn3 Gen1 force 4-EMEP no soft reset 5-PCIE to CIO Target disable 6-CIO to PCIE RO Target disable 7-CIO to PCIE Target disable	0-Force Gen1 in Dn0 Port 1-Force Gen1 in Dn1 Port 2-Force Gen1 in Dn2 Port 3-Force Gen1 in Dn3 Port 4-Disables D3 --> D0 Reset 5-Disables PCIE to CIO Target access 6-Disables CIO to PCIE Target access to Read Only registers 7-Disables CIO to PCIE Target access	N/A
0x00A2	[7:0]	Reserved	Reserved	N/A
0x00A3	[3:0]	DP_IN Capability ID	DP_IN Capability ID	
0x00A3	[7:4]	DP_OUT Capability ID	DP_OUT Capability ID	
0x00A4	[3:0]	DP_IN Maximal DPCD Rev	DP_IN Maximal DPCD Rev 0: 1.1 1: 1.2	
0x00A4	[7:4]	DP_OUT Maximal DPCD Rev	DP_OUT Maximal DPCD Rev 0: 1.1 1: 1.2	
0x00A5	[3:0]	DP_IN Maximal link rate	DP_IN Maximal link rate 0: 1.62 1: 2.7 2: 5.4	
0x00A5	[7:4]	DP_OUT Maximal link rate	DP_OUT Maximal link rate 0: 1.62 1: 2.7 2: 5.4	
0x00A6	[2:0]	DP_IN Maximal lane count	DP_IN Maximal lane count 0: 1 1: 2 2: 4	
0x00A6	[5:3]	DP_OUT Maximal lane count	DP_OUT Maximal lane count 0: 1 1: 2 2: 4	
0x00A6	6	DP_IN MST capability	DP_IN MST capability 0: not supported 1: supported	
0x00A6	7	DP_OUT MST capability	DP_OUT MST capability 0: not supported 1: supported	
0x00A7	0	DP_IN Legacy Adapters Only	DP_IN Legacy Adapters Only 0: Enable new/dp1.2 adapters 1: Enable legacy DP adapters only	

Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x00A7	1	DP_OUT Legacy Adapters Only	DP_OUT Legacy Adapters Only 0: Enable new/dp1.2 adapters 1: Enable legacy DP adapters only	
0x00A7	2	DP_IN AUX adapter for MIN_DP_CAP_ID(0)	DP_IN AUX adapter for MIN_DP_CAP_ID(0) 0: legacy 1: dp1.2	
0x00A7	3	DP_OUT AUX adapter for MIN_DP_CAP_ID(0)	DP_OUT AUX adapter for MIN_DP_CAP_ID(0) 0: legacy 1: dp1.2	
0x00A7	4	DP_IN SST adapter for MIN_DP_CAP_ID(0)	DP_IN SST adapter for MIN_DP_CAP_ID(0) 0: legacy 1: dp1.2	
0x00A7	5	DP_OUT SST adapter for MIN_DP_CAP_ID(0)	DP_OUT SST adapter for MIN_DP_CAP_ID(0) 0: legacy 1: dp1.2	
0x00A7	6	DP_IN AUX adapter for MIN_DP_CAP_ID(1)	DP_IN AUX adapter for MIN_DP_CAP_ID(1) 0: legacy 1: dp1.2	
0x00A7	7	DP_OUT AUX adapter for MIN_DP_CAP_ID(1)	DP_OUT AUX adapter for MIN_DP_CAP_ID(1) 0: legacy 1: dp1.2	
0x00A8	0	DP_IN SST adapter for MIN_DP_CAP_ID(1)	DP_IN SST adapter for MIN_DP_CAP_ID(1) 0: legacy 1: dp1.2	
0x00A8	1	DP_OUT SST adapter for MIN_DP_CAP_ID(1)	DP_OUT SST adapter for MIN_DP_CAP_ID(1) 0: legacy 1: dp1.2	
0x00A8	2	DP_IN Prefer SST legacy	Whenever possible, use legacy DP_IN SST adapter 0: DP_IN SST adapter is selected only according to MIN_DP_CAP_ID(x)/ ee_sst_in_adp_dx 1: Legacy DP_IN SST adapter should be used whenever the link is SST 1.62G or 2.7G	
0x00A8	3	DP_OUT Prefer SST legacy	Whenever possible, use legacy DP_OUT SST adapter 0: DP_IN SST adapter is selected only according to MIN_DP_CAP_ID(x)/ ee_sst_in_adp_dx 1: Legacy DP_IN SST adapter should be used whenever the link is SST 1.62G or 2.7G	
0x00A8	4	DP_IN Wide Tx TL mode	Work in wide Tx mode in DP_IN from TL to the adapter 0: work in legacy mode 1: work in wide mode	
0x00A8	5	DP_OUT Wide Tx TL mode	Work in wide Tx mode in DP_OUT from TL to the adapter 0: work in legacy mode 1: work in wide mode	

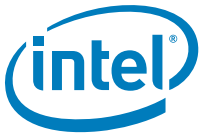


Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x00A8	6	Reserved	Reserved	N/A
0x00A8	7	ee_cdr_mode_en_pre	ee_cdr_mode_en - "0" disable "1" enable CDRmode	N/A
0x00A9	[7:0]	ee_master_lock_timeout	Timeout for target bus master "lock" hold without use, in [ms]; 0 disables locking mechanism	N/A
0x00AA	[7:0]	Disable Downstream Bridges	Bit 7 – activate Bits[4:0] – Disable	
0x00AB	[6:0]	Reserved	Reserved	N/A
0x00AB	7	ee_cio_phy_dis_rs	disable reed salomon mode in cio null phy	
0x00AC	[7:0]	pa_ee_dp_swap2	swap in case the cable was connected upside down	
0x00AD	[7:0]	Reserved	Reserved	N/A
0x00AE	[7:0]	pb_ee_dp_swap2	swap in case the cable was connected upside down	
0x00AF	0	ee_clc_debug_disable_uart_2	disable the second uart	LC_GENERAL[20]
0x00AF	1	ee_plug_event_source	0 - GPIO is set with ee_arc_config 1 - GPIO Only	N/A
0x00AF	2	Enable 64 bit BAR in DMA	1'b0 – DMA 64 bit BAR dis 1'b1 – DMA 64 bit BAR en	N/A
0x00AF	3	Enable 64 bit BAR in USB	1'b0 – USB 64 bit BAR dis 1'b1 – USB 64 bit BAR en	N/A
0x00AF	4	Disable MSIIX in USB EMEPs	0: MSI-X supported 1: MSI-X is disabled	N/A
0x00AF	5	Enable real link between USB and PCIE Switch	1'b0 – no real rate 1'b1 – real rate	N/A
0x00AF	6	ee_usb_swap_dis	CB to enable/disable swap in USB mode -"1" disable swap, "0" swap is supported	N/A
0x00AF	7	Enable DMA in Endpoint mode	1'b0 – no DMA 1'b1 – DMA exists	N/A
0x00B0	[7:0]	PCIE Swithc control (FR)	for future use	N/A
0x00B1	[7:0]	PCIE Swithc control (AR)	for future use	N/A
0x00B2	[7:0]	PCIE PHY control 1	for future use	N/A
0x00B3	[7:0]	PCIE PHY control 2	for future use	N/A
0x00B4	[7:0]	PCIE PHY control 3	for future use	N/A
0x000B5	[7:0]	PCIE PHY control 4	for future use	N/A
0x00B6	[1:0]	Clock Rate of DMA	2'h0 – Gen1 2'h1 – Gen2 2'h2 – Gen3	N/A
0x00B6	[3:2]	Clock Rate of USB	2'h0 – Gen1 2'h1 – Gen2 2'h2 – Gen3	N/A

Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x00B6	4	Enable fast PCIE Switch clock	1'b0 – disable fast 1'b1 – enable fast	N/A
0x00B6	5	ee_usb_aux_xtal_ck_en	select if to move to xtal clk when stable for usb_aux clk in car_poc_usb. "1" move to xtal else stay w/ lc_osc	N/A
0x00B6	6	pa_ee_usb2_polarity	polarity of USB2 D+/D- pins	N/A
0x00B6	7	pb_ee_usb2_polarity	polarity of USB2 D+/D- pins	N/A
0x00B7	[7:0]	USB SBRN Register	USB SBRN Register	N/A
0x00B8	0	ee_pcie_phy_ahb_clk_sel	select between clk freq, legacy 25Mhz -"0", new mode 100Mhz from POC - "1"	N/A
0x00B8	1	ee_pcie_phy_stable_legacy1_new0	new feature to enable pcie clks when no PLL to work on 100Mhz poc clk. "1" - legacy - "0" new mode if stable=1 --> PCIE PLL, if stable =0 -> 100 POC	N/A
0x00B8	2	ee_hub_mode	enable HUB mode - "1"	N/A
0x00B8	3	DMA EMEP Prefetchable BAR	0: MSI-X supported 1: MSI-X is disabled	N/A
0x00B8	4	DMA EMEP No Soft Reset	0: Internal reset upon D3 --> D0 1: No internal reset upon D3 --> D0	N/A
0x00B8	5	DMA source reset control	0: Reset doesn't include D3 --> D0 1: Reset includes D3 --> D0	N/A
0x00B8	6	Immediate DMA init done after reset	1: Init done immediately after Reset	N/A
0x00B8	7	ee_xtal_pcie_sw_clksel_dis	0: sw_clk works w/ both xtal/pcie 1: new feature disabled, sw_clk works only w/ PCIE clks	N/A
0x00B9	[7:0]	Reserved	Reserved	N/A
0x00BA	[7:0]	Control Tx Deempasis	Tx Coefficients	N/A
0x00BB	[7:0]	Control Tx Deempasis	Tx Coefficients	N/A
0x00BC	[7:0]	Control Tx Deempasis	Tx Coefficients	N/A
0x00BD	[7:0]	Reserved	Reserved	N/A
0x00BE	[1:0]	Reserved	Reserved	N/A
0x00BE	2	Clock assign for rate change disable	0: XHC/DMA/adapter clocks are assigned from PCIE Switch Ports 1: Each clock use its own pipe rate control	N/A
0x00BE	3	Immediate PCIE init done after reset	1: Init done immediately after Reset	N/A
0x00BE	4	USB EMEP Prefetchable BAR	0: MSI-X supported 1: MSI-X is disabled	N/A
0x00BE	5	USB EMEP No Soft Reset	0: Internal reset upon D3 --> D0 1: No internal reset upon D3 --> D0	N/A
0x00BE	6	Phy Status value for not connected lanes	0: PhyStatus = 0 for not connected lanes 1: PhyStatus = 1 for not connected lanes	N/A
0x00BE	7	Immediate USB init done after reset	1: Init done immediately after Reset	N/A

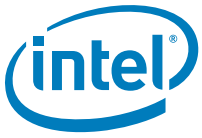


Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x00BF	[7:0]	EE_TO_TAR Base [7:0]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x00C0	[7:0]	EE_TO_TAR Base [15:8]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x00C1	[7:0]	EE_TO_TAR Base [23:16]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x00C2	[7:0]	ee_to_tar_cio_size[7:0]	Size of EE_TO_TAR section, in amount of tuples; 0 = nothing to do.	N/A
0x00C3	[7:0]	EE_TO_TAR Base [7:0]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x00C4	[7:0]	EE_TO_TAR Base [15:8]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x00C5	[7:0]	EE_TO_TAR Base [23:16]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x00C6	[7:0]	ee_to_tar_pcie_size[7:0]	Size of EE_TO_TAR section, in amount of tuples; 0 = nothing to do.	N/A
0x00C7	[7:0]	EE_TO_TAR Base [7:0]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x00C8	[7:0]	EE_TO_TAR Base [15:8]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x00C9	[7:0]	EE_TO_TAR Base [23:16]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x00CA	[7:0]	ee_to_tar_dma_size[7:0]	Size of EE_TO_TAR section, in amount of tuples; 0 = nothing to do.	N/A
0x00CB	[7:0]	EE_TO_TAR Base [7:0]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x00CC	[7:0]	EE_TO_TAR Base [15:8]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x00CD	[7:0]	EE_TO_TAR Base [23:16]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x00CE	[7:0]	ee_to_tar_usb_pa_size[7:0]	Size of EE_TO_TAR section, in amount of tuples; 0 = nothing to do.	N/A
0x00CF	[7:0]	EE_TO_TAR Base [7:0]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x00D0	[7:0]	EE_TO_TAR Base [15:8]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x00D1	[7:0]	EE_TO_TAR Base [23:16]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A

Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x00D2	[7:0]	ee_to_tar_usb_pb_size[7:0]	Size of EE_TO_TAR section, in amount of tuples; 0 = nothing to do.	N/A
0x00D3	[7:0]	EE_TO_TAR Base [7:0]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x00D4	[7:0]	EE_TO_TAR Base [15:8]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x00D5	[7:0]	EE_TO_TAR Base [23:16]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x00D6	[7:0]	ee_to_tar_p2c_pa_size[7:0]	Size of EE_TO_TAR section, in amount of tuples; 0 = nothing to do.	N/A
0x00D7	[7:0]	EE_TO_TAR Base [7:0]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x00D8	[7:0]	EE_TO_TAR Base [15:8]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x00D9	[7:0]	EE_TO_TAR Base [23:16]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x00DA	[7:0]	ee_to_tar_p2c_pb_size[7:0]	Size of EE_TO_TAR section, in amount of tuples; 0 = nothing to do.	N/A
0x00DB	[7:0]	EE_TO_TAR Base [7:0]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x00DC	[7:0]	EE_TO_TAR Base [15:8]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x00DD	[7:0]	EE_TO_TAR Base [23:16]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x00DE	[7:0]	ee_to_tar_pcie_phy_size[7:0]	Size of EE_TO_TAR section, in amount of tuples; 0 = nothing to do.	N/A
0x00DF	[7:0]	EE_TO_TAR Base [7:0]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x00E0	[7:0]	EE_TO_TAR Base [15:8]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x00E1	[7:0]	EE_TO_TAR Base [23:16]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x00E2	[7:0]	ee_to_tar_ana_comm_size[7:0]	Size of EE_TO_TAR section, in amount of tuples; 0 = nothing to do.	N/A
0x00E3	[7:0]	EE_TO_TAR Base [7:0]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x00E4	[7:0]	EE_TO_TAR Base [15:8]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A

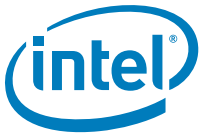


Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x00E5	[7:0]	EE_TO_TAR Base [23:16]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x00E6	[7:0]	ee_to_tar_dp_domain_size[7:0]	Size of EE_TO_TAR section, in amount of tuples; 0 = nothing to do.	N/A
0x00E7	[7:0]	ee_clc_spare_plus_pa		
0x00E8	[7:0]	ee_clc_spare_plus_pa		
0x00E9	[7:0]	ee_clc_spare_plus_pb		
0x00EA	[7:0]	ee_clc_spare_plus_pb		
0x00EB	[7:0]	ee_clc_spare_plus_pa/pb/pc		
0x00EC	[7:0]	ee_clc_spare_plus_pa/pb/pc		
0x00ED	[7:0]	hw_gpio_ownership	hw ownership configuration for gpio_0[4:0] hw ownership configuration for gpio_1[7:5]	
0x00EE	[7:0]	hw_gpio_ownership	hw ownership configuration for gpio_1[1:0] hw ownership configuration for gpio_2[6:2] hw_ownership configuration for gpio_3[7]	
0x00EF	[7:0]	hw_gpio_ownership	hw ownership configuration for gpio_3[3:0] hw ownership configuration for gpio_4[7:4]	
0x00F0	[7:0]	hw_gpio_ownership	hw ownership configuration for gpio_4[0] hw ownership configuration for gpio_5[5:1] hw_ownership configuration for gpio_6[7:6]	
0x00F1	[7:0]	hw_gpio_ownership	hw ownership configuration for gpio_6[2:0] hw ownership configuration for gpio_7[7:3]	
0x00F2	[7:0]	hw_gpio_ownership	hw ownership configuration for gpio_8[4:0] hw ownership configuration for poc_gpio_0[7:5]	
0x00F3	[7:0]	hw_gpio_ownership	hw ownership configuration for poc_gpio_0[1:0] hw ownership configuration for poc_gpio_1[6:2] hw_ownership configuration for poc_gpio_2[7]	
0x00F4	[7:0]	hw_gpio_ownership	hw ownership configuration for poc_gpio_2[3:0] hw ownership configuration for poc_gpio_3[7:4]	
0x00F5	[7:0]	hw_gpio_ownership	hw ownership configuration for poc_gpio_3[0] hw ownership configuration for poc_gpio_4[5:1] hw_ownership configuration for poc_gpio_5[7:6]	
0x00F6	[7:0]	hw_gpio_ownership	hw ownership configuration for poc_gpio_5[2:0] hw ownership configuration for poc_gpio_6[7:3]	
0x00F7	[7:0]	hw_gpio_ownership	hw ownership configuration for snk0_ddc_data[4:0] hw ownership configuration for snk0_ddc_clk[7:5]	

Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x00F8	[7:0]	hw_gpio_ownership	hw ownership configuration for snk0_ddc_clk[1:0] hw ownership configuration for snk1_ddc_data[6:2] hw_ownership configuration for snk1_ddc_clk[7]	
0x00F9	[3:0]	hw_gpio_ownership	hw ownership configuration for snk1_ddc_clk[3:0]	
0x00F9	[7:4]	Reserved	Reserved	N/A
0x00FA	[4:0]	ee_i2c_scl_master_ctrl	i2c_scl_master_ctrl	
0x00FA	[7:5]	Reserved	Reserved	N/A
0x00FB	[4:0]	ee_i2c_sda_master_ctrl	i2c_sda_master_ctrl	
0x00FB	[7:5]	Reserved	Reserved	N/A
0x00FC	[4:0]	ee_i2c_scl_slave_ctrl	i2c_scl_slave_ctrl	
0x00FC	[7:5]	Reserved	Reserved	N/A
0x00FD	[4:0]	ee_i2c_sda_slave_ctrl	i2c_sda_slave_ctrl	
0x00FD	[7:5]	Reserved	Reserved	N/A
0x00FE	[4:0]	ee_tmu_clk_in_ctrl	tmu_clk_in_ctrl	
0x00FE	[7:5]	Reserved	Reserved	N/A
0x00FF	[7:0]	Reserved	Reserved	N/A
0x0100	[7:0]	Reserved	Reserved	N/A
0x0101	[4:0]	ee_pa_overcur_ctrl	pa_overcur_ctrl	
0x0101	[7:5]	Reserved	Reserved	N/A
0x0102	[7:0]	ee_pcie_clk_req_ctrl	TBD	
0x0103	[7:0]	Reserved	Reserved	N/A
0x0104	[7:0]	Reserved	Reserved	N/A
0x0105	[7:0]	Reserved	Reserved	N/A
0x0106	[7:0]	Reserved	Reserved	N/A
0x0107	[7:0]	Configuration bits for CIO Switch	enable	
0x0108	[7:0]	cl1 exit period	value for RO phy reg CL1 exit period	
0x0109	[7:0]	cl2 exit period	value for RO phy reg CL2 exit period	
0x010A	[2:0]	ee_rm_lc_int	RM bits for ram shells in LC	
0x010A	[5:3]	ee_rm_ana_int	RM bits for ram shells in ANA	
0x010A	[7:6]	Reserved	Reserved	N/A
0x010B	[2:0]	ee_rm_usb_int	RM bits for ram shells in USB	
0x010B	[5:3]	ee_rm_pcie_int	RM bits for ram shells in PCIE	
0x010B	[7:6]	Reserved	Reserved	N/A
0x010C	[2:0]	ee_rm_dp_int	RM bits for ram shells in DP	
0x010C	[5:3]	ee_rm_cio_int	RM bits for ram shells in CIO	
0x010C	[7:6]	Reserved	Reserved	N/A
0x010D	[2:0]	ee_rm_rom_lc_int	RM bits for rom shells in LC	

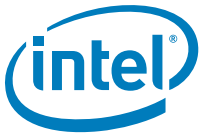


Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x010D	[5:3]	ee_rm_rom_cio_int	RM bits for rom shells in CIO	
0x010D	6	ee_dp_in_fec_cap		
0x010D	7	ee_dp_out_fec_cap		
0x010E	[7:0]	ee_drom_start_addr[7:0]	Base address (in Bytes) from which the DROM is being read (in bytes, points to the size field).	
0x010F	[7:0]	ee_drom_start_addr[15:9]	Base address (in Bytes) from which the DROM is being read (in bytes, points to the size field).	
0x0110	[7:0]	ee_drom_start_addr[23:16]	Base address (in Bytes) from which the DROM is being read (in bytes, points to the size field).	
0x0111	[7:0]	ee_drom_start_addr[31:24]	Base address (in Bytes) from which the DROM is being read (in bytes, points to the size field).	
0x0112	[7:0]	Reserved	Reserved	N/A
0x0113	[7:0]	Reserved	Reserved	N/A
0x0114	[7:0]	Reserved	Reserved	N/A
0x0115	[7:0]	Select Ports to force de-emphasis	bit 0 - Up, bit 1 - Dn0, … , bit 3 - Dn4	N/A
0x0116	[7:0]	Invert Port type (Up/ Dn)	bit 0 - Up, bit 1 - Dn0, … , bit 3 - Dn4	N/A
0x0117	[4:0]	ee_pa_pwr_ctrl	gw_gpio_ownership config	
0x0117	[7:5]	Reserved	Reserved	N/A
0x0118	[4:0]	ee_pb_pwr_ctrl	gw_gpio_ownership config	
0x0118	[7:5]	Reserved	Reserved	N/A
0x0119	[7:0]	ee_cdr_usb_ctrl [7:0]	cdr - TBD	N/A
0x011A	[7:0]	ee_cdr_usb_ctrl [15:8]	cdr - TBD	N/A
0x011B	[7:0]	ee_cdr_usb_ctrl [23:16]	cdr - TBD	N/A
0x011C	[7:0]	ee_cdr_usb_ctrl [31:24]	cdr - TBD	N/A
0x011D	[7:0]	snk1_ee_hdp_phy_cfg 0	DP-phy control bits	N/A
0x011E	[7:0]	snk1_ee_hdp_phy_cfg 1	DP-phy control bits	
0x011F	[7:0]	snk1_ee_hdp_phy_cfg 2	DP-phy control bits	
0x0120	[7:0]	snk1_ee_hdp_phy_cfg 3	DP-phy control bits	
0x0121	[7:0]	snk1_ee_hdp_phy_cfg 4	DP-phy control bits	
0x0122	[7:0]	snk1_ee_hdp_phy_cfg 5	DP-phy control bits	
0x0123	[7:0]	snk1_ee_hdp_phy_cfg 6	DP-phy control bits	
0x0124	[7:0]	snk1_ee_hdp_phy_cfg 7	DP-phy control bits	

Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x0125	[7:0]	snk2_ee_hdp_phy_cfg 0	DP-phy control bits	
0x0126	[7:0]	snk2_ee_hdp_phy_cfg 1	DP-phy control bits	
0x0127	[7:0]	snk2_ee_hdp_phy_cfg 2	DP-phy control bits	
0x0128	[7:0]	snk2_ee_hdp_phy_cfg 3	DP-phy control bits	
0x0129	[7:0]	snk2_ee_hdp_phy_cfg 4	DP-phy control bits	
0x012A	[7:0]	snk2_ee_hdp_phy_cfg 5	DP-phy control bits	
0x012B	[7:0]	snk2_ee_hdp_phy_cfg 6	DP-phy control bits	
0x012C	[7:0]	snk2_ee_hdp_phy_cfg 7	DP-phy control bits	
0x012D	[7:0]	pa_ee_hdp_phy_cfg0	DP-phy control bits	
0x012E	[7:0]	pa_ee_hdp_phy_cfg1	DP-phy control bits	
0x012F	[7:0]	pa_ee_hdp_phy_cfg2	DP-phy control bits	N/A
0x0130	[7:0]	pa_ee_hdp_phy_cfg3	DP-phy control bits	
0x0131	[7:0]	pb_ee_hdp_phy_cfg0	DP-phy control bits	
0x0132	[7:0]	pb_ee_hdp_phy_cfg1	DP-phy control bits	
0x0133	[7:0]	pb_ee_hdp_phy_cfg2	DP-phy control bits	
0x0134	[7:0]	pb_ee_hdp_phy_cfg3	DP-phy control bits	
0x0135	[7:0]	pc_ee_hdp_phy_cfg0	DP-phy control bits	
0x0136	[7:0]	pc_ee_hdp_phy_cfg1	DP-phy control bits	
0x0137	[7:0]	pc_ee_hdp_phy_cfg2	DP-phy control bits	
0x0138	[7:0]	pc_ee_hdp_phy_cfg3	DP-phy control bits	
0x0139	[4:0]	ee_write_protect_gen_ poll_timer[4:0]	this timer used to configure the polling time need when using generic_fsm for status bit (BUSY) of flash. The resolution is 100us multplay by this setting.	N/A
0x0139	5	ee_cio_phy_halt_on_r eset_pa	cause the cio controller wake on halt state allowing control from debugger	
0x0139	6	ee_cio_phy_halt_on_r eset_pa	cause the cio controller wake on halt state allowing control from debugger	
0x0139	7	ee_cio_phy_halt_on_r eset_pa	cause the cio controller wake on halt state allowing control from debugger	
0x013A	0	ee_ignore_secure_stra p	default "0" - Once this bit is set (on the final, secure system), the security strap will be ignored	N/A
0x013A	[7:1]	Reserved	Reserved	N/A
0x013B	[7:0]	ee_tr_pcie_sw_ctrl1	pcie switch general controls	
0x013C	[7:0]	ee_tr_pcie_sw_ctrl2	pcie switch general controls	
0x013D	0	ee_package_mode_ho st	HOST	

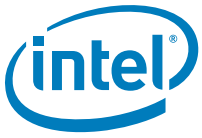


Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x013D	1	ee_package_mode_device	DEVICE	
0x013D	2	ee_package_mode_cdr	CDR	
0x013D	3	ee_package_mode_hub	HUB	
0x013D	[7:4]	Reserved	Reserved	N/A
0x013E	[4:0]	ee_perst_n_ctrl	perst gpio ctrl	
0x013E	[7:5]	Reserved	Reserved	N/A
0x013F	[4:0]	ee_pcie_clk_req_p_ctrl	ee_pcie_clk_req_p_ctrl	
0x013F	[7:5]	Reserved	perst gpio ctrl	
0x0140	[7:0]	PU GPIO Ownership configuration	2 bits per GPIO pin 00 : Link Controller 01 : HardwareControlled (custom)	
0x0141	[7:0]	PU GPIO Ownership configuration	2 bits per GPIO pin 00 : Link Controller 01 : HardwareControlled (custom)	
0x0142	[7:0]	PU GPIO Ownership configuration	2 bits per GPIO pin 00 : Link Controller 01 : HardwareControlled (custom)	
0x0143	[7:0]	PU GPIO Ownership configuration	2 bits per GPIO pin 00 : Link Controller 01 : HardwareControlled (custom)	
0x0144	[7:0]	POC GPIO Ownership configuration	2 bits per GPIO pin 00 : Link Controller 01 : HardwareControlled (custom)	
0x0145	[7:0]	POC GPIO Ownership configuration	2 bits per GPIO pin 00 : Link Controller 01 : HardwareControlled (custom)	
0x0146	[7:0]	POC GPIO Ownership configuration	2 bits per GPIO pin 00 : Link Controller 01 : HardwareControlled (custom)	
0x0147	[7:0]	POC GPIO Ownership configuration	2 bits per GPIO pin 00 : Link Controller 01 : HardwareControlled (custom)	
0x0148	[7:0]	hw_gpio_ownership_1		
0x0149	[7:0]	hw_gpio_ownership_1		
0x014A	[7:0]	hw_gpio_ownership_1		
0x014B	[7:0]	hw_gpio_ownership_1		
0x014C	[7:0]	hw_gpio_ownership_1		
0x014D	[7:0]	hw_gpio_ownership_1		
0x014E	[7:0]	hw_gpio_ownership_1		
0x014F	[7:0]	hw_gpio_ownership_1		
0x0150	[7:0]	hw_gpio_ownership_1		
0x0151	[7:0]	hw_gpio_ownership_1		

Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x0152	[7:0]	hw_gpio_ownership_1		
0x0153	[7:0]	hw_gpio_ownership_1		
0x0154	[4:0]	ee_pa_lsrx_ctrl	gpio ctrl	
0x0154	[7:5]	Reserved	Reserved	N/A
0x0155	[4:0]	ee_pb_lsrx_ctrl	gpio ctrl	
0x0155	[7:5]	Reserved	Reserved	N/A
0x0156	[4:0]	ee_pc_lsrx_ctrl	gpio ctrl	
0x0156	[7:5]	Reserved	Reserved	N/A
0x0157	[4:0]	ee_pa_lstx_ctrl	gpio ctrl	
0x0157	[7:5]	Reserved	Reserved	N/A
0x0158	[4:0]	ee_pb_lstx_ctrl	gpio ctrl	
0x0158	[7:5]	Reserved	Reserved	N/A
0x0159	[4:0]	ee_pc_lstx_ctrl	gpio ctrl	
0x0159	[7:5]	Reserved	Reserved	N/A
0x015A	[4:0]	ee_pa_hpd_ctrl	gpio ctrl	
0x015A	[7:5]	Reserved	Reserved	N/A
0x015B	[4:0]	ee_pb_hpd_ctrl	gpio ctrl	
0x015B	[7:5]	Reserved	Reserved	N/A
0x015C	[4:0]	ee_pc_hpd_ctrl	gpio ctrl	
0x015C	[7:5]	Reserved	Reserved	N/A
0x015D	[5:0]	Disable CIO lanes	When a lane is in CIO mode, value of 1 disable the internal controller communicate the appropriate lane LS messages.	DEV.SEC6.GENERAL[11:10]
0x015D	[7:6]	ee_hdp_car_cb		
0x015E	[7:0]	power indication per domain X - "1" -ON	hdp_cmn_wrap_power_good - 0 pcie_switch_domain_power_good -1 usb_dig_wrap_power_good - 2 cio_domain_power_good -3 svr_domain_power_good – 4 pab_ ana_comm_power_good -5 pc_ ana_comm_power_good -6 usb_ana_comm_power_good -7 cdr_usb_top_power_good -8	
0x015F	[7:0]	power indication per domain X - "1" -ON	hdp_cmn_wrap_power_good - 0 pcie_switch_domain_power_good -1 usb_dig_wrap_power_good - 2 cio_domain_power_good -3 svr_domain_power_good – 4 pab_ ana_comm_power_good -5 pc_ ana_comm_power_good -6 usb_ana_comm_power_good -7 cdr_usb_top_power_good -8	

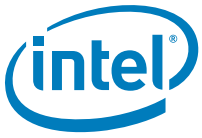


Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x0160	[7:0]	EE_TO_TAR Base [7:0]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x0161	[7:0]	EE_TO_TAR Base [15:8]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x0162	[7:0]	EE_TO_TAR Base [23:16]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x0163	[7:0]	ee_to_tar_p2c_pc_size [7:0]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x0164	[7:0]	EE_TO_TAR Base [7:0]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x0165	[7:0]	EE_TO_TAR Base [15:8]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x0166	[7:0]	EE_TO_TAR Base [23:16]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x0167	[7:0]	ee_to_tar_res_pc_size [7:0]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x0168	[7:0]	EE_TO_TAR Base [7:0]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x0169	[7:0]	EE_TO_TAR Base [15:8]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x016A	[7:0]	EE_TO_TAR Base [23:16]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x016B	[7:0]	ee_to_tar_res_pc_size [7:0]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x016C	[7:0]	EE_TO_TAR Base [7:0]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x016D	[7:0]	EE_TO_TAR Base [15:8]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x016E	[7:0]	EE_TO_TAR Base [23:16]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x016F	[7:0]	ee_to_tar_res_pc_size [7:0]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x0170	[7:0]	EE_TO_TAR Base [7:0]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A

Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x0171	[7:0]	EE_TO_TAR Base [15:8]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x0172	[7:0]	EE_TO_TAR Base [23:16]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x0173	[7:0]	ee_to_tar_res_pc_size [7:0]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x0174	[7:0]	EE_TO_TAR Base [7:0]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x0175	[7:0]	EE_TO_TAR Base [15:8]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x0176	[7:0]	EE_TO_TAR Base [23:16]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x0177	[7:0]	ee_to_tar_res_pc_size [7:0]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x0178	[7:0]	snk2 ee dp swap2	configuration bits for DP lane swap on cable connect	
0x0179	[7:0]	snk1 ee dp swap1	configuration bits for DP lane swap on cable connect	
0x017A	[7:0]	pc ee dp swap2	configuration bits for DP lane swap on cable connect	
0x017B	[7:0]	ee_ee2tar_ctrl[7:0]	enables HW ee2tar, bit per client	N/A
0x017C	[7:0]	ee_ee2tar_ctrl[15:8]	enables HW ee2tar, bit per client	N/A
0x017D	[7:0]	ee_dp_in_rsrvd[7:0]		
0x017E	[7:0]	ee_dp_in_rsrvd[15:8]		
0x017F	[7:0]	ee_dp_out_rsrvd[7:0]		
0x0180	[7:0]	ee_dp_out_rsrvd[15:8]		
0x0181	[7:0]	ee_dp_fec_in_cb		
0x0182	[7:0]	ee_tar_timeout	Target timeout value	N/A
0x0183	[7:0]	ee_clc_spare_pc[7:0]		
0x0184	[7:0]	ee_clc_spare_pc[15:8]		
0x0185	[7:0]	ee_clc_spare_plus_pc[7:0]		
0x0186	[7:0]	ee_clc_spare_plus_pc[15:8]		
0x0187	[7:0]	Reserved	Reserved	N/A
0x0188	[7:0]	Reserved	Reserved	N/A
0x0189	[7:0]	Reserved	Reserved	N/A
0x018A	[7:0]	Reserved	Reserved	N/A
0x018B	[7:0]	Reserved	Reserved	N/A

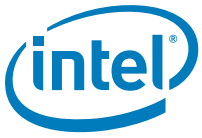


Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x018C	[7:0]	Reserved	Reserved	N/A
0x018D	[7:0]	Reserved	Reserved	N/A
0x018E	[7:0]	Reserved	Reserved	N/A
0x018F	[7:0]	Reserved	Reserved	N/A

4.0 Programming Interface

4.1 Register/Memory Access

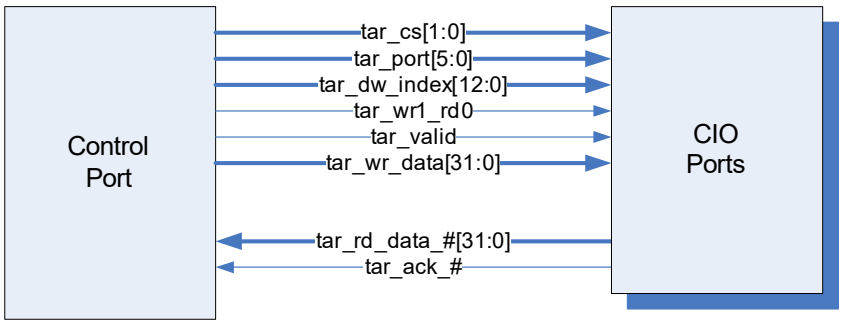
4.1.1 CIO Configuration Space Registers Access

These registers are accessed either through the Control Port µController, which receives the commands either from a CIO Packet or from FLASH Fields, or through the JTAG or I2C Slave mechanisms, which bypass the µController and access the Target Bus directly.

4.1.1.1 Target Bus Access via CIO Packet

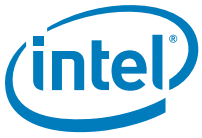
Between the CIO Control Port and all the CIO Ports, there is an internal "target" interface used to access various configuration spaces in the ports. That interface is one-to-many / many-to-one, meaning all ports see all transactions and respond only when the destination port matches their own configuration (Figure 7).

Figure 7. Target Bus (# denotes CIO Port number)



The target bus can be driven by:

- Control Port µController
  - On reception of "CIO Config Layer Read/Write REQUEST" packets. This is the default method used by software.
  - As part of Control Port initialization sequence after CIO Reset, set of registers pre-configured in Flash Memory can be written.
- JTAG (for debug purposes).



4.1.1.2 Target Bus Access via Flash Memory

As part of the initialization sequence, a set of registers preconfigured in Flash Memory can be written. This can be done to fix default values or execute a custom workaround/configuration. See Section 3.3 for more details.

4.1.1.3 JTAG Access

There is an option to access any register mapped to the Target bus through JTAG commands. There are three registers accessed thru JTAG - command, write_data and read_data; all 32 bit wide.

Write flow

- Insert CTRL_PORT_DATA instruction (6'b111001) to IR.
- Insert 32 bits of data to write to JTAG DR. Push to TDI, start from MSB.
- Insert CTRL_PORT_CMD instruction (6'b111000) to IR.
- Insert 32 bits of command to JTAG DR. Push to TDI, start from MSB.
  - Structure: {Reserved[7'h00], Command[4'b0001], Configuration Space[1:0], Port[5:0], DWIndex[12:0]}. See Table 17.

Read flow

- Insert CTRL_PORT_CMD instruction (6'b111000) to IR.
- Insert 32 bits of command to JTAG DR. Push to TDI, start from MSB.
  - Structure: {Reserved [7'h00], Command [4'b0000], Configuration Space [1:0], Port [5:0], DWIndex[12:0]}. See Table 17.
- Insert CTRL_PORT_READ instruction (6'b111010) to IR.
- Wait 1ms.
- Push 32 bits to TDI and collect read data from TDO. MSB is read first.

The Command register parameters are decoded by Control Port according as follows:

Table 17. Command Register Parameters

31 25	24 21	20 19	18 13	12 0
Reserved	CMD	CS	Port#	DW Index

Field	Bit(s)	Description	
DW Index	12:0		Sets DW Index Target bus value
Port#	18:13		Sets Port# Target bus value
CS	20:19	Sets CS Target bus value, as follows:	
		CS Value	**Configuration space**
		00	Path Config. Space
		01	Port Config. Space
		10	Device Config. Space
		11	Counters Config. Space
CMD	21	0: Read command 1: Write command	

Field	Bit(s)	Description
	22	0: Regular Target bus access 1: Access to CIO Switch registers
	23	0: Regular Target bus access 1: Access to PCIe Switch registers
Reserved	31:24	Reserved

4.1.1.3.1 Assumptions / Notes:

- The write data is entered before the command. Otherwise, data in the write_data register will be written.
- There is no "cycle completion" mechanism - it is assumed that the cycle is completed properly.
- Since target bus is much faster than JTAG, no overrides of commands should occur. Yet, waiting ~1ms between accesses will ensure internal cycle completion.
- The cycle may complete with an internal timeout (if the targeted register does not respond with ack). If there is a write there is no indication. If there is a read, 0xDEADBEEF is returned.
- There is a round robin arbitration mechanism between Control Port and JTAG target accesses, thus they should not miss each other. Cycle completion is guaranteed by timeout (1ms).
- Access through JTAG does not involve the micro-controller at all.

4.1.1.4 I^2C Master

4.1.1.4.1 Description

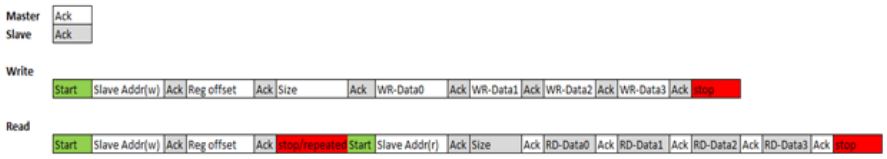
Titan Ridge DD has an internal I^2C master in order to communicate with external controllers. Titan Ridge DD I^2C master supports clock stretching. Titan Ridge DD I^2C master does not support a multi-master environment.

4.1.1.5 I^2C Slave

4.1.1.5.1 Description

I^2C Slave module is used in Titan Ridge DD in order to provide additional access to the chip (similar to JTAG access) through external interface but using reduced pin count (two overall: clock & data). I^2C has a serial Interface which internally transforms into parallel data. I^2C main function is to act as slave and provide read/write access to chip target bus.

Figure 8. I2C Transaction Type



4.1.1.5.2 Transaction legend

- Start bit
- Slave addr - 7'b + 1bit for read/write -> "1" read, "0" write
- Reg offset [7:0] - register obsolete offset in i2c slave target map area.
- Size [7:0] - number of i2c byte to be written or read (see notes below).
- WR/RD_data [7:0] - byte of data
- Stop bit

4.1.1.5.3 Additional Notes

- It is permissible to write 1 or 2 or 3 or 4 bytes in write transaction - any byte above that will be ignored internally in the i2c slave controller and only the first dWord will be used.
- It is permissible to read 1 or 2 or 3 or 4 bytes in read transaction - any master read above the 4th bytes will be answered with zeros. A valid answer is considered first dWord.
- In case of delay in respond in i2c slave size, clk starching will be used.

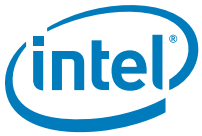
4.2 Register Terminology

Table 18. Register Terminology

Shorthand	Description
R/W	Read/Write. A register with this attribute can be read and written. If written since reset, the value read reflects the value written.
R/W S	Read/Write Status. A register with this attribute can be read and written. This bit represents status of some sort, so the value read may not reflect the value written.
RO	Read Only. If a register is read only, writes to this register have no effect.
WO	Write Only. Reading this register may not return a meaningful value.
R/Clr	Read Clear. A register bit with this attribute is cleared after read. Writes have no effect on the bit value.
W/Clr	Write Clear. A register bit with this attribute is cleared after writing any value.
R/W SC	Read/Write Self Clearing. When written to a 1b the bit causes an action to be initiated. Once the action is complete, the bit returns to 0b. These fields are always read as zero.
R/W1C	Read/Write Clear. A register bit with this attribute can be read and written. However, a Write of a 1b clears (sets to 0b) the corresponding bit and a write of a 0b has no effect.

Table 18. Register Terminology

Shorthand	Description
HwInit	For PCIe registers (from PCI Express Base 2.0 specification). Hardware Initialized – Register bits are initialized by firmware or hardware mechanisms such as pin strapping or serial FLASH. (System firmware hardware initialization is only allowed for system integrated devices). Bits are read only after initialization and can only be reset (for write-once by firmware) with Fundamental Reset. HwInit register bits are not modified by an FLR.
ROS	For PCIe registers (from PCI Express Base 2.0 specification). Sticky - Read-only – Register bits are read-only and cannot be altered by software. Bits are neither initialized nor modified by hot reset or FLR. Where noted, devices that consume AUX power must preserve sticky register values when AUX power consumption (via either AUX power or PME Enable) is enabled. In these cases, registers are neither initialized nor modified by hot, warm, or cold reset.
RsvdP	For PCIe registers (from PCI Express Base 2.0 specification). Reserved and Preserved – Reserved for future R/W implementations. Registers are read-only and must return zero when read. Software must preserve the value read for writes to bits.
RsvdZ	For PCIe registers (from PCI Express Base 2.0 specification). Reserved and Zero – Reserved for future RW1C implementations. Registers are read-only and must return zero when read. Software must use 0b for writes to bits.



4.3 PCI Express Configuration Space

This chapter contains register tables of PCIE Configuration Space of PCIE Bridges/Endpoints in Thunderbolt (PCIE Spec registers and custom registers).

See PCI Express Base 3.0 specification for additional information about PCIE Spec registers.

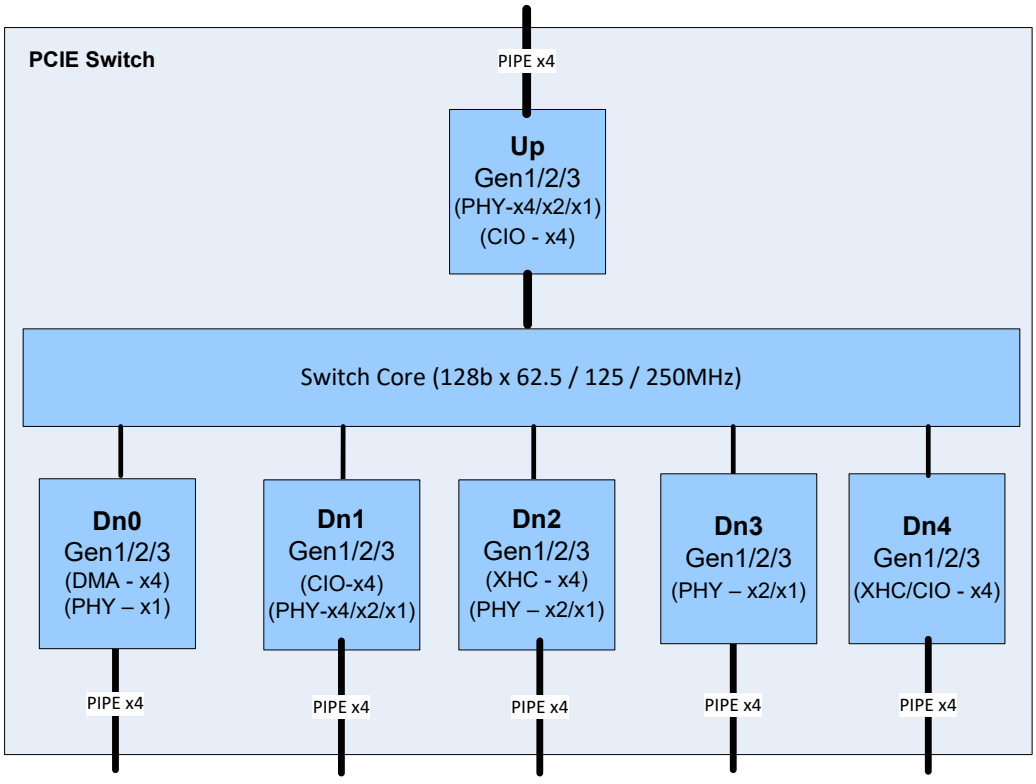
Thunderbolt contains PCIE Switch: Upstream and five Downstream Ports. The PCIe switch structure is shown in Figure 9 .

In addition it contains two PCIE Embedded Endpoints for DMA and XHC.

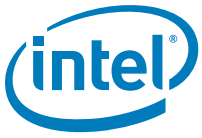
PCIE Switch connects to:

- DMA through Embedded Endpoint.
- XHC through Embedded Endpoint.
- CIO Switch Port through Adapter
- PCIE PHY

Figure 9. PCIe Switch Structure



In each PCIE Port there is PCIE Configuration Space that contains Basic and Extended Capabilities in two separate linked lists.



List of Basic Capabilities

Upstream / Downstream

"Address 0x34 Capability Pointer with value 0x80 (This is still in the Header)

"Address 0x80 PM Capability with next capability pointer - 0x88

"Address 0x88 MSI Capability with next capability pointer - 0xAC

"Address 0xAC SubSysID Capability with next capability pointer - 0xC0

"Address 0xC0 PCIE Capability with next capability pointer - 0x50

"Address 0x50 FPB Capability with next capability pointer - 0x00 (last)

DMA EMEP

"Address 0x34 Capability Pointer with value 0x80 (This is still in the Header)

"Address 0x80 PM Capability with next capability pointer - 0x88

"Address 0x88 MSI Capability with next capability pointer - 0xC0

"Address 0xC0 PCIE Capability with next capability pointer - 0xA0

"Address 0xA0 MSI-X Capability with next capability pointer - 0x00 (last)

XHC EMEP

"Address 0x34 Capability Pointer with value 0x80 (This is still in the Header)

"Address 0x80 PM Capability with next capability pointer - 0x88

"Address 0x88 MSI Capability with next capability pointer - 0xC0

"Address 0xC0 PCIE Capability with next capability pointer - 0x00 (last)

List of Extended Capabilities

Upstream

"Address 0x100 - Device Serial Number Capability with next pointer - 0x200

"Address 0x200 - Advanced Error Reporting Capability with next pointer - 0x300

"Address 0x300 - Virtual Channel Capability with next pointer - 0x400

"Address 0x400 - Power Budgeting Capability with next pointer - 0x500

"Address 0x500 - Vendor Specific Enhanced Capability1 with next pointer - 0x600

"Address 0x600 - Vendor Specific Enhanced Capability2 with next pointer - 0x700

"Address 0x700 - Secondary PCIE Capability with next pointer - 0x800

"Address 0x800 - Latency Tolerance Reporting Capability with next pointer - 0xA00

"Address 0xA00 - L1 PM Substates Capability with next pointer - 0xB00

"Address 0xB00 - Precision Time Management Capability with next pointer - 0xC00

Address 0xC00 - Flattening Portal Bridge Capability with next pointer - 0 (last)

Downstream

"Address 0x100 - Device Serial Number Capability with next pointer - 0x200

"Address 0x200 - Advanced Error Reporting Capability with next pointer - 0x300

"Address 0x300 - Virtual Channel Capability with next pointer - 0x400

"Address 0x400 - Power Budgeting Capability with next pointer - 0x500

"Address 0x500 - Vendor Specific Enhanced Capability1 with next pointer - 0x600

"Address 0x600 - Vendor Specific Enhanced Capability2 with next pointer - 0x700

"Address 0x700 - Secondary PCIE Extended Capability with next pointer - 0x900

"Address 0x900 - Access Control Services Capability with next pointer - 0xC00

Address 0xC00 - Flattening Portal Bridge Capability with next pointer - 0 (last)

DMA EMEP

"Address 0x100 - Device Serial Number Capability with next pointer - 0x200

"Address 0x200 - Advanced Error Reporting Capability with next pointer - 0x300

"Address 0x300 - Virtual Channel Capability with next pointer - 0x400

"Address 0x400 - Power Budgeting Capability with next pointer - 0x500

"Address 0x500 - Vendor Specific Enhanced Capability with next pointer - 0x600

"Address 0x600 - Latency Tolerance Reporting Capability with next pointer - 0x0

XHC EMEP

"Address 0x100 - Device Serial Number Capability with next pointer - 0x200

"Address 0x200 - Advanced Error Reporting Capability with next pointer - 0x300

"Address 0x300 - Virtual Channel Capability with next pointer - 0x400

"Address 0x400 - Power Budgeting Capability with next pointer - 0x500

"Address 0x500 - Vendor Specific Enhanced Capability with next pointer - 0x600

"Address 0x600 - Latency Tolerance Reporting Capability with next pointer - 0x700

"Address 0x700 - Secondary PCIE Extended Capability with next pointer - 0x0 (last)

4.3.1 Type 0 Configuration Space Header

Thunderbolt contains two PCIE Embedded Endpoints: for DMA and XHC. Each Endpoint has Type 0 Configuration Space Header.

Figure 10 details allocation for register fields of Type 0 Configuration Space header for PCI Express device Functions. Those fields are described in Table 19.

Figure 10. Type 0 Configuration Space Header

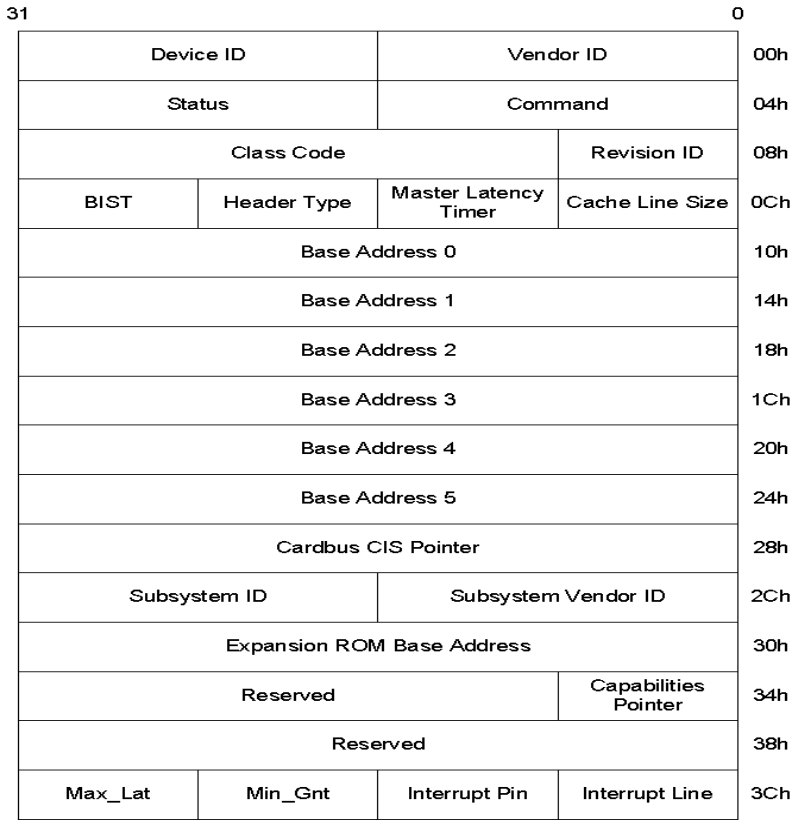


Table 19. Type 0 Configuration Space Header Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x00	PCIE_TYPE0_0	15:0	Vendor ID	RO	0x8086
0x00	PCIE_TYPE0_0	31:16	Device ID	RO	DMA EMEP - 0x15EB XHC EMEP - 0x15EC
0x04	PCIE_TYPE0_1	15:0	Command	See PCIe Spec	0

Table 19. Type 0 Configuration Space Header Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x04	PCIE_TYPE0_1	31:16	Status	See PCIe Spec	0x0010
0x08	PCIE_TYPE0_2	7:0	Revision ID	RO	0
0x08	PCIE_TYPE0_2	31:8	Class Code	RO	DMA EMEP - 0x088000 XHC EMEP - 0x0C0330
0x0C	PCIE_TYPE0_3	7:0	Cache Line Size	R/W	0
0x0C	PCIE_TYPE0_3	15:8	Master Latency Timer	RO	0
0x0C	PCIE_TYPE0_3	23:16	Header Type	RO	0
0x0C	PCIE_TYPE0_3	31:24	BIST	See PCIe Spec	0
0x10	PCIE_TYPE0_4	31:0	Base Address 0	See PCIe Spec	See BAR0 in Table 20
0x14	PCIE_TYPE0_5	31:0	Base Address 1	See PCIe Spec	See BAR1 in Table 20
0x18	PCIE_TYPE0_6	31:0	Base Address 2	See PCIe Spec	See BAR2 in Table 20
0x1C	PCIE_TYPE0_7	31:0	Base Address 3	See PCIe Spec	See BAR3 in Table 20
0x20	PCIE_TYPE0_8	31:0	Base Address 4	See PCIe Spec	See BAR4 in Table 20
0x24	PCIE_TYPE0_9	31:0	Base Address 5	See PCIe Spec	See BAR5 in Table 20
0x28	PCIE_TYPE0_10	31:0	Cardbus CIS Pointer	RO	0
0x2C	PCIE_TYPE0_11	15:0	Subsystem Vendor ID	RO	0x2222
0x2C	PCIE_TYPE0_11	31:16	Subsystem ID	RO	0x1111
0x30	PCIE_TYPE0_12	31:0	Expansion ROM Base Address	See PCIe Spec	0
0x34	PCIE_TYPE0_13	7:0	Capabilities Pointer	RO	0x80
0x34	PCIE_TYPE0_13	31:8	Reserved	RO	0
0x38	PCIE_TYPE0_14	31:0	Reserved	RO	0
0x3C	PCIE_TYPE0_15	7:0	Interrupt Line	R/W	0xFF
0x3C	PCIE_TYPE0_15	15:8	Interrupt Pin	RO	0x01
0x3C	PCIE_TYPE0_15	23:16	Min_Gnt	RO	0
0x3C	PCIE_TYPE0_15	31:24	Max_Lat	RO	0

The Subsystem Vendor ID and Subsystem ID fields can be loaded from FLASH during boot to values other than default.

There are two BARs in DMA EMEP with option to configure 32 or 64 bit from EEPROM

"Memory space of 256K that can be 32 or 64 bit BAR

"MSIX of 4K that can be 32 or 64 bit

Table 20. DMA EMEP BAR Values (32bit)

BAR	Value
BAR0 (MEM)	32'b1111_1111_1111_1100_0000_0000_0000_0000
BAR1 (MSIX)	32'b1111_1111_1111_1111_1111_0000_0000_0000
BAR2	32'b0
BAR3	32'b0
BAR4	32'b0
BAR5	32'b0

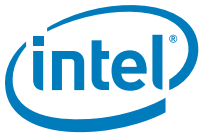


Table 21. DMA EMEP BAR Values (64bit)

BAR	Value
BAR0 (MEM)	32'b1111_1111_1111_1100_0000_0000_0000_0100
BAR1 (MEM)	32'hFFFFFFFF
BAR2 (MSIX)	32'b1111_1111_1111_1111_1111_0000_0000_0100
BAR3 (MSIX)	32'hFFFFFFFF
BAR4	32’b0
BAR5	32’b0

There is a Memory BAR of 64K in XHC EMEP with option to configure 32 or 64 bit from EEPROM.

Table 22. XHC EMEP BAR Values (32bit)

BAR	Value
BAR0 (MEM)	32'b1111_1111_1111_1111_0000_0000_0000_0000
BAR1	32’b0
BAR2	32’b0
BAR3	32’b0
BAR4	32’b0
BAR5	32’b0

Table 23. XHC EMEP BAR Values (32bit)

BAR	Value
BAR0 (MEM)	32'b1111_1111_1111_1111_0000_0000_0000_0100
BAR1 (MEM)	32'hFFFFFFFF
BAR2 (MSIX)	32’b0
BAR3 (MSIX)	32’b0
BAR4	32’b0
BAR5	32’b0

4.3.2 Type 1 Configuration Space Header

Figure 11 details allocation for register fields of Type 1 Configuration Space header for Switch and Root Complex virtual PCI Bridges (US and DS ports). Those fields are described in Table 24.

Figure 11. Type 1 Configuration Space Header

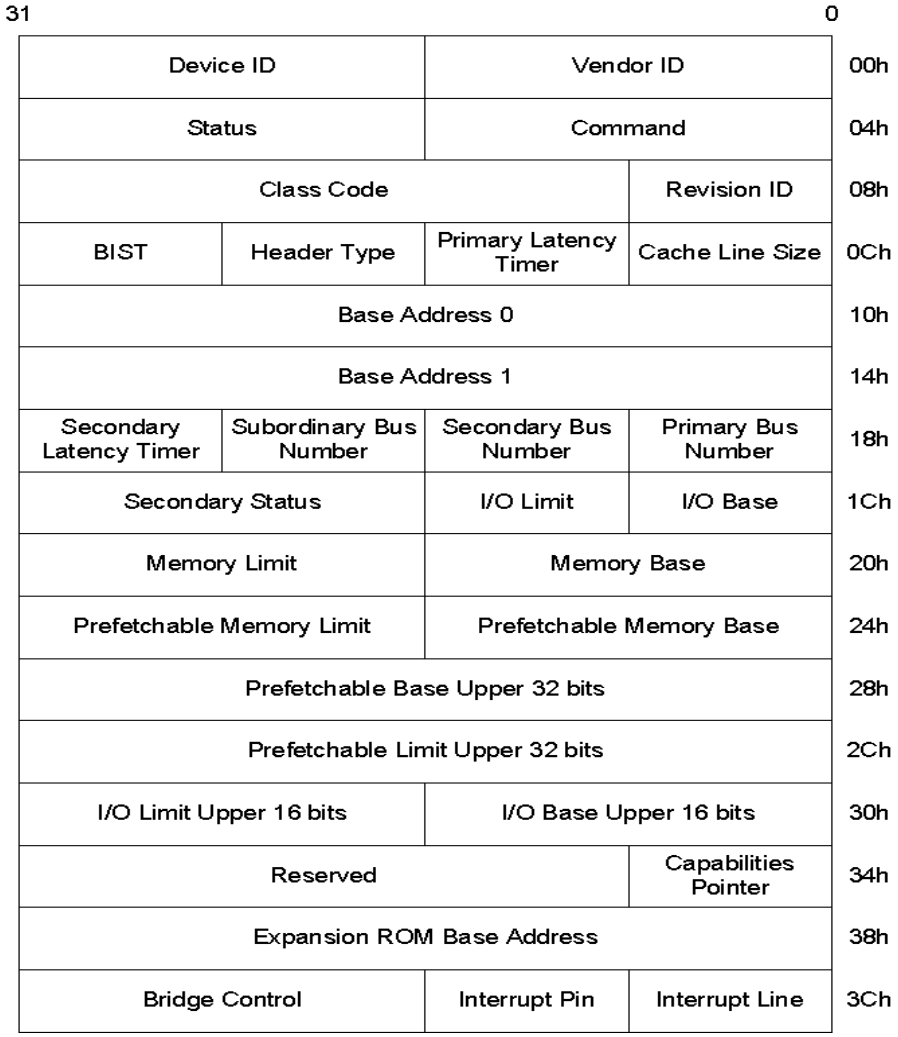


Table 24. Type 1 Configuration Space Header Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x00	PCIE_TYPE0_0	15:0	Vendor ID	RO	0x8086
0x00	PCIE_TYPE0_0	31:16	Device ID	RO	0x15EA
0x04	PCIE_TYPE0_1	15:0	Command	See PCIe Spec	0
0x04	PCIE_TYPE0_1	31:16	Status	See PCIe Spec	0x0010
0x08	PCIE_TYPE0_2	7:0	Revision ID	RO	0
0x08	PCIE_TYPE0_2	31:8	Class Code	RO	0x060400
0x0C	PCIE_TYPE0_3	7:0	Cache Line Size	R/W	0
0x0C	PCIE_TYPE0_3	15:8	Primary Latency Timer	RO	0
0x0C	PCIE_TYPE0_3	23:16	Header Type	RO	0x01
0x0C	PCIE_TYPE0_3	31:24	BIST	See PCIe Spec	0

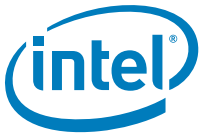


Table 24. Type 1 Configuration Space Header Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x10	PCIE_TYPE0_4	31:0	Base Address 0	See PCIe Spec	0
0x14	PCIE_TYPE0_5	31:0	Base Address 1	See PCIe Spec	0
0x18	PCIE_TYPE0_6	7:0	Primary Bus Number	R/W	0
0x18	PCIE_TYPE0_6	15:8	Secondary Bus Number	R/W	0
0x18	PCIE_TYPE0_6	23:16	Subordinate Bus Number	R/W	0
0x18	PCIE_TYPE0_6	31:24	Secondary Latency Timer	RO	0
0x1C	PCIE_TYPE0_7	7:0	I/O Base	R/W	0x01
0x1C	PCIE_TYPE0_7	15:8	I/O Limit	R/W	0x01
0x1C	PCIE_TYPE0_7	31:16	Secondary Status	See PCIe Spec	0
0x20	PCIE_TYPE0_8	15:0	Memory Base	See PCIe Spec	0
0x20	PCIE_TYPE0_8	31:16	Memory Limit	See PCIe Spec	0
0x24	PCIE_TYPE0_9	15:0	Prefetchable Memory Base	See PCIe Spec	0x0001
0x24	PCIE_TYPE0_9	31:16	Prefetchable Memory Limit	See PCIe Spec	0x0001
0x28	PCIE_TYPE0_10	31:0	Prefetchable Base Upper 32 bits	R/W	0
0x2C	PCIE_TYPE0_11	31:0	Prefetchable Limit Upper 32 bits	R/W	0
0x30	PCIE_TYPE0_12	15:0	I/O Base Upper 16 bits	R/W	0
0x30	PCIE_TYPE0_12	31:16	I/O Limit Upper 16 bits	R/W	0
0x34	PCIE_TYPE0_13	7:0	Capabilities Pointer	RO	0x80
0x34	PCIE_TYPE0_13	31:8	Reserved	RO	0
0x38	PCIE_TYPE0_14	31:0	Expansion ROM Base Address	RO	0
0x3C	PCIE_TYPE0_15	7:0	Interrupt Line	R/W	0xFF
0x3C	PCIE_TYPE0_15	15:8	Interrupt Pin	RO	0x01
0x3C	PCIE_TYPE0_15	31:16	Bridge Control	See PCIe Spec	0

4.3.3 PCI Power Management Capability

Figure 12 details the structure of register fields for Power Management registers and Table 25 describes the register's fields.

Figure 12. Power Management Registers

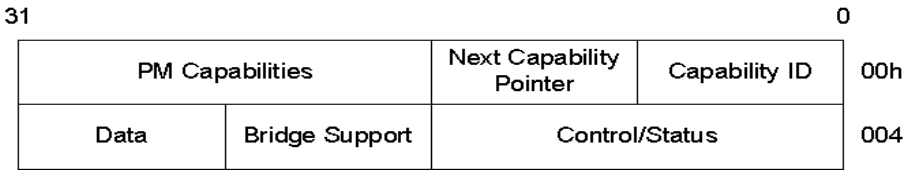


Table 25. Power Management Registers Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x80	PM_CAP_0	7:0	Capability ID	RO	0x01
0x80	PM_CAP_0	15:8	Next Capability Pointer	RO	0x88
0x80	PM_CAP_0	31:16	PM Capabilities	See PCIe Spec	0xFEC3
0x84	PM_CAP_1	15:0	Control and Status	See PCIe Spec	Up/Dn - 0x0008 EMEP - 0x0
0x84	PM_CAP_1	23:16	Bridge Support	See PCIe Spec	0x00
0x84	PM_CAP_1	31:24	Data	See PCIe Spec	0x00

4.3.4 MSI Capability

MSI Capability exists in PCIE Switch Bridges and in Embedded Endpoints

Figure 13 details structure of register fields for MSI registers and Table 26 describes the register's fields.

Figure 13. MSI Registers

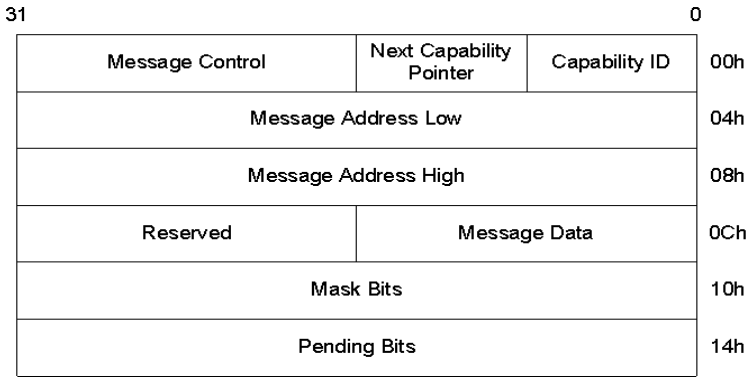


Table 26. MSI Registers Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x88	MSI_CAP_0	7:0	Capability ID	RO	0x05

Table 26. MSI Registers Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x88	MSI_CAP_0	15:8	Next Capability Pointer	RO	Up/Dn - 0xAC EMEP - 0xC0
0x88	MSI_CAP_0	31:16	Message Control	See PCIe Spec	Up/Dn - 0x0080 DMA EP - 0x0080 XHC EP - 0x0086
0x8C	MSI_CAP_1	31:0	Message Address Low	R/W	0
0x90	MSI_CAP_2	31:0	Message Address High	R/W	0
0x94	MSI_CAP_3	15:0	Message Data	R/W	0
0x94	MSI_CAP_3	31:16	Reserved	RO	0
0x98	MSI_CAP_4	31:0	Mask Bits	R/W	0
0x9C	MSI_CAP_5	31:0	Pending Bits	RO	0

4.3.5 Subsystem Vendor ID and Subsystem ID Capability

Standard SubSystem and SubVendor ID Capability that resides in Capability linked list of Upstream and Downstream Bridges. (EMEP contains these fields in Configuration Space Header).

The registers can be loaded from FLASH during boot to values other than default.

Figure 14. Sub System and Sub Vendor ID Registers

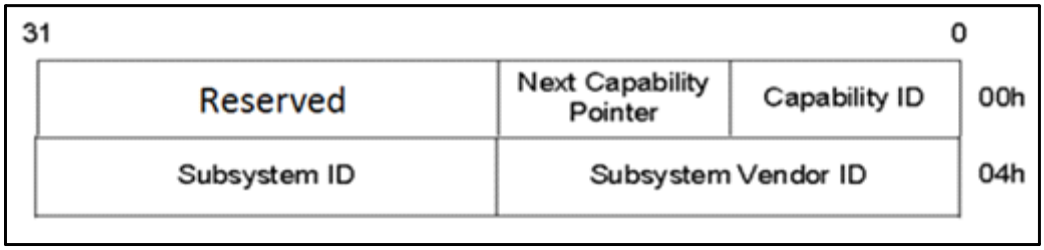


Table 27. Sub System and Sub Vendor ID Registers Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0xAC	SUBSYS_CAP_0	7:0	Capability ID	RO	0x0D
0xAC	SUBSYS _CAP_0	15:8	Next Capability Pointer	RO	0xC0
0xAC	SUBSYS _CAP_0	31:16	Reserved	RO	0x0
0xB0	SUBSYS _CAP_1	15:0	Subsystem Vendor ID	RO	0x2222
0xB0	SUBSYS _CAP_1	31:16	Subsystem ID	RO	0x1111

4.3.6 PCI Express Capability

Figure 15 details the structure of the register fields for PCIe Capabilities registers and Table 28 describes the register's fields (see also Table 29).

Figure 15. PCI Express Registers

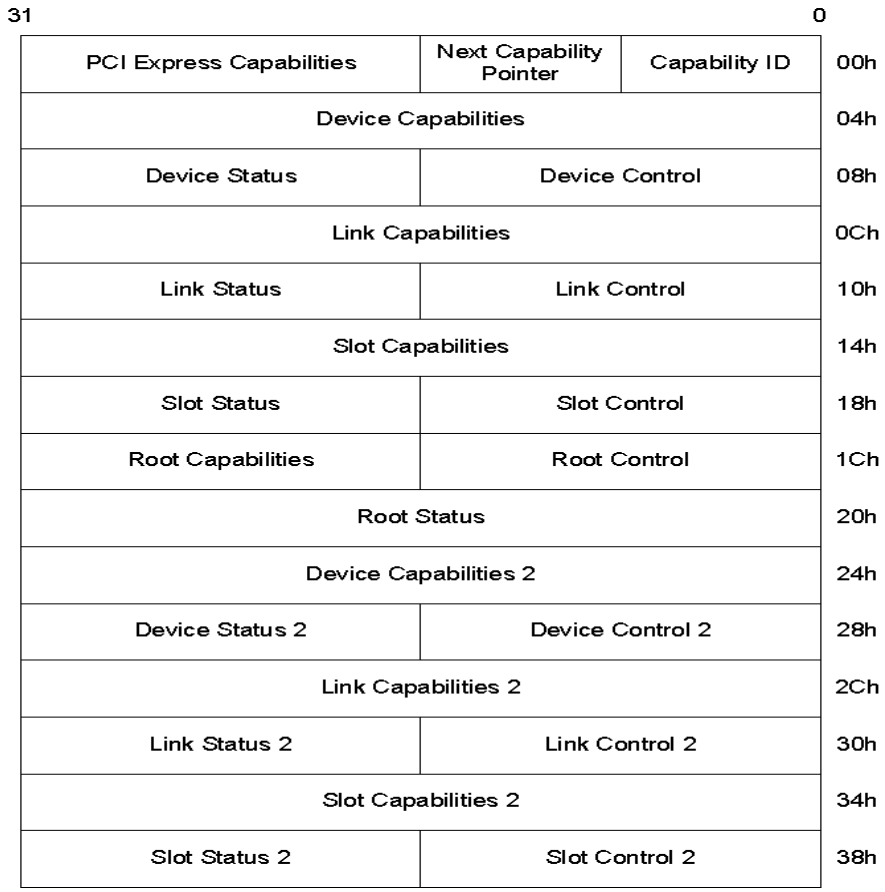


Table 28. PCI Express Registers Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0xC0	PCIE_CAP_0	7:0	Capability ID	RO	0x10
0xC0	PCIE_CAP_0	15:8	Next Capability Pointer	RO	Up/Dn – 0x50 (FPB) XHC EMEP – 0 (last) DMA EMEP – 0xA0 (MSIx)
0xC0	PCIE_CAP_0	31:16	PCI Express Capabilities	See PCIe Spec	Up - 0x0052 Dn - 0x0162 EMEP - 0x0002
0xC4	PCIE_CAP_1	31:0	Device Capability	See PCIe Spec	0x00008020
0xC8	PCIE_CAP_2	15:0	Device Control	See PCIe Spec	0x2810
0xC8	PCIE_CAP_2	31:16	Device Status	See PCIe Spec	Up/Dn – 0 EMEP - 0x0010

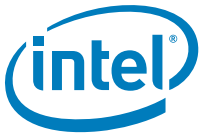


Table 28. PCI Express Registers Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0xCC	PCIE_CAP_3	31:0	Link Capability	See PCIe Spec	0x0027_FC43 Some fields change according to Port number and Speed / Link Width limit See PCIe Spec
0xD0	PCIE_CAP_4	15:0	Link Control	See PCIe Spec	0
0xD0	PCIE_CAP_4	31:16	Link Status	See PCIe Spec	16'h1041
0xD4	PCIE_CAP_5	31:0	Slot Capability	See PCIe Spec	0x0004_0060 Some fields change according to Port number See PCIe Spec
0xD8	PCIE_CAP_6	15:0	Slot Control	See PCIe Spec	0
0xD8	PCIE_CAP_6	31:16	Slot Status	See PCIe Spec	0
0xDC	PCIE_CAP_7	15:0	Root Control	See PCIe Spec	0
0xDC	PCIE_CAP_7	31:16	Root Capability	See PCIe Spec	0
0xE0	PCIE_CAP_8	31:0	Root Status	See PCIe Spec	0
0xE4	PCIE_CAP_9	31:0	Device Capability 2	See PCIe Spec	32'h0000812
0xE8	PCIE_CAP_10	15:0	Device Control 2	See PCIe Spec	0
0xE8	PCIE_CAP_10	31:16	Device Status 2	See PCIe Spec	0
0xEC	PCIE_CAP_11	31:0	Link Capability 2	See PCIe Spec	0
0xF0	PCIE_CAP_12	15:0	Link Control 2	See PCIe Spec	0x0000_0003 See PCIe Spec
0xF0	PCIE_CAP_12	31:16	Link Status 2	See PCIe Spec	0x0000_0040 See PCIe Spec
0xF4	PCIE_CAP_13	31:0	Slot Capability 2	See PCIe Spec	0
0xF8	PCIE_CAP_14	15:0	Slot Control 2	See PCIe Spec	0
0xF8	PCIE_CAP_14	31:16	Slot Status 2	See PCIe Spec	0

4.3.7 MSIx Capability

MSIx Capability exists only in the DMA Embedded Endpoint.

Figure 16 details the structure of the register fields for MSIx registers. Table 29 describes the register's fields.

Figure 16. MSIx Registers

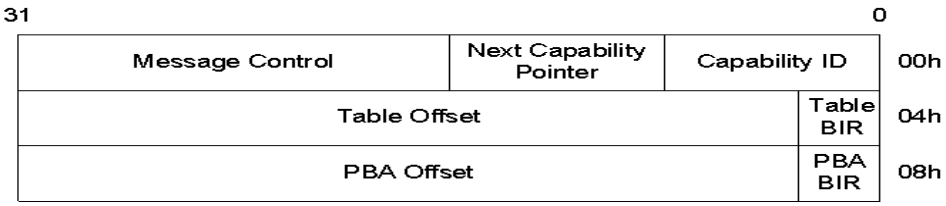


Table 29. MSIx Registers Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0xA0	MSIX_CAP_0	7:0	Capability ID	RO	0x11
0xA0	MSIX_CAP_0	15:8	Next Capability Pointer	RO	0
0xA0	MSIX_CAP_0	31:16	Message Control	See PCIe Spec	0
0xA4	MSIX_CAP_1	2:0	Table BIR	RO	32b - 0x1 64b -0x2
0xA4	MSIX_CAP_1	31:3	Table Offset	RO	0
0xA8	MSIX_CAP_2	2:0	PBA BIR	RO	32b - 0x1 64b -0x2
0xA8	MSIX_CAP_2	31:3	PBA Offset	RO	0x1F4

4.3.8 Flattening Portal Bridge (FPB) Capability

FPB Capability exists only in the PCIe Switch Bridges (Upstream and Downstream). Figure 17 details the structure of the register fields for FPB registers. Table 30 describes the register's fields.

Figure 17. Flattening Portal Bridge (FPB) Registers

Table 30. Flattening Portal Bridge (FPB) Registers

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x50	FPB_CAP_0	7:0	CAP_ID	RO	0x15
0x50	FPB_CAP_0	15:8	NXT_PTR - Pointer to the next item in the capabilities list. Must be NULL for the final item in the list.	RO	0
0x50	FPB_CAP_0	31:16	Reserved	RsvdP	0
0x54	FPB_CAP_1	0	FPB BD Vector Supported - If Set, indicates that the BD Vector mechanism is supported.	RO	1
0x54	FPB_CAP_1	1	FPB MEM Low Vector Supported - If Set, indicates that the MEM Low Vector mechanism is supported.	RO	1

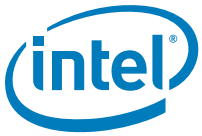


Table 30. Flattening Portal Bridge (FPB) Registers

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x54	FPB_CAP_1	2	FPB MEM High Vector Supported - If Set, indicates that the Mem High mechanism is supported.	RO	1
0x54	FPB_CAP_1	7:3	FPB Num Sec Dev - For Upstream Ports of Switches only, this field indicates the quantity of Device Numbers associated with the Secondary Side of the Upstream Port Bridge. The quantity is determined by adding one to the numerical value of this field. Although it is encouraged that Switch implementations consume Function Numbers efficiently, it is explicitly permitted that Downstream Ports be assigned to Function Numbers that are not contiguous within the indicated range of Device Numbers, and system software is required to scan for Downstream Port Bridges at every Function Number within the indicated quantity of Device Numbers associated with the Secondary Side of the Upstream Port. This field is Reserved for Downstream Ports.	RO/ RsvdP	0x4
0x54	FPB_CAP_1	10:8	FPB BD Vector Size Supported - Indicates the size of the FPB BD Vector implemented in hardware, and constrains the allowed values software is permitted to write to the FPB BD Vector Granularity field. Defined encodings are: ValueSizeAllowed Granularities 000b256 bits8, 16, 32, 64, 128, 256 001b512 bits 8, 16, 32, 64, 128 010b1K bits 8, 16, 32, 64 011b2K bits 8, 16, 32 100b4K bits8, 16 101b8K bits8 All other encodings are Reserved If the FPB BD Vector Supported bit is Clear, then the value in this field is undefined and must be ignored by software.	RO	0x2
0x54	FPB_CAP_1	15:11	Reserved	RsvdP	0

Table 30. Flattening Portal Bridge (FPB) Registers

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x54	FPB_CAP_1	18:16	FPB MEM Low Vector Size Supported - Indicates the size of the Mem Low Vector implemented in hardware, and constrains the allowed values software is permitted to write to the FPB MEM Low Vector Start field. Defined encodings are: ValueSizeAllowed Granularities 000b256 bits1, 2, 4, 8, 16 001b512 bits 1, 2, 4, 8 010b1K bits 1, 2, 4 011b2K bits 1, 2 100b4K bits 1 All other encodings are Reserved If the FPB Mem Low Vector Supported bit is Clear, then the value in this field is undefined and must be ignored by software.	RO	0x1
0x54	FPB_CAP_1	23:19	Reserved	RsvdP	0
0x54	FPB_CAP_1	26:24	FPB MEM High Vector Size Supported - Indicates the size of the Mem Low Vector implemented in hardware. Defined encodings are: 000b256 bits 001b512 bits 010b1K bits 011b2K bits 100b4K bits 101b8K bits All other encodings are Reserved If the FPB Mem High Vector Supported bit is Clear, then the value in this field is undefined and must be ignored by software.	RO	0
0x54	FPB_CAP_1	31:27	Reserved	RsvdP	0
0x58	FPB_CAP_2	0	FPB BD Vector Enable - When Set, enables the FPB BD Vector mechanism If the FPB BD Vector Supported bit is Clear, then it is permitted for hardware to implement this bit as RO, and in this case the value in this field is undefined. Default value of this bit is 0b.	RW/RO	0
0x58	FPB_CAP_2	3:1	Reserved	RsvdP	0

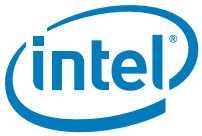


Table 30. Flattening Portal Bridge (FPB) Registers

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x58	FPB_CAP_2	7:4	FPB BD Vector Granularity - The value written by software to this field controls the granularity of the FPB BD Vector and the required alignment of the FPB BD Vector Start field (below). Defined encodings are: ValueGranularityStart Alignment Constraint 0000b8 BDF<no constraint> 0001b16 BDF…0b 0010b32 BDF…00b 0011b64 BDF…000b 0100b128 BDF…0000b 0101b256 BDF…00000b All other encodings are Reserved Based on the implemented FPB BD Vector size, hardware is permitted to implement as RW only those bits of this field that can be programmed to non-zero values, in which case the upper order bits are permitted but not required to be hardwired to 0. If the FPB BD Vector Supported bit is Clear, then it is permitted for hardware to implement this field as RO, and the value in this field is undefined. Default value for this field is 0000b.	RW/RO	0
0x58	FPB_CAP_2	18:8	Reserved	RsvdP	0

Table 30. Flattening Portal Bridge (FPB) Registers

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x58	FPB_CAP_2	31:19	FPB BD Vector Start - The value written by software to this field controls the offset within BD space at which the FPB BD Vector is applied. The value represents a Bus/Device Number (bits [15:3] of an address in BDF Space), such that bit 0 of the FPB BD Vector represents the range starting from the value in this register up to that value plus the granularity minus 1 and bit 1 represents range from this register value plus granularity up to that value plus granularity minus 1, etc. The Function Number offset (bits[2:0]) is fixed by hardware as 000b and cannot be modified. Software must program this field to a value that is naturally aligned according to the value in the FPB BD Vector Granularity Field as indicated in the description for that field (above). If this requirement is violated, the hardware behavior is undefined. If the FPB BD Vector Supported bit is Clear, then it is permitted for hardware to implement this field as RO, and the value in this field is undefined. Default value for this field is 000h.	RW/RO	0
0x5C	FPB_CAP_3	2:0	Reserved	RsvdP	0
0x5C	FPB_CAP_3	15:3	BD Secondary Start - The value written by software to this field controls the offset within BDF space at which Type 1 Configuration Requests passing downstream through the bridge must be converted to Type 0. The value represents a Bus/Device Number (bits [15:3] of an address in BDF Space). The Function Number offset (bits[2:0]) is fixed by hardware as 000b and cannot be modified. When the ARI Forwarding Enable bit in the Device Control 2 register is Set, then software must write bits 7:3 of this field to 00000b. If the FPB BD Vector Supported bit is Clear, then it is permitted for hardware to implement this field as RO, and the value in this field is undefined. Default value for this field is 000h.	RW/RO	0
0x5C	FPB_CAP_3	31:16	Reserved	RsvdP	0

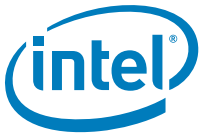


Table 30. Flattening Portal Bridge (FPB) Registers

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x60	FPB_CAP_4	0	FPB MEM Low Vector Enable - When Set, enables the FPB MEM Low Vector mechanism. If the FPB MEM Low Vector Supported bit is Clear, then it is permitted for hardware to implement this field as RO, and in this case the value in this field is undefined. Default value of this bit is 0b.	RW/RO	0
0x60	FPB_CAP_4	3:1	Reserved	RsvdP	0
0x60	FPB_CAP_4	7:4	FPB MEM Low Vector Granularity - The value written by software to this field controls the granularity of the FPB MEM Low Vector, and the required alignment of the FPB MEM Low Vector Start field (below). Defined encodings are: ValueGranularityStart Alignment Constraint 0000b1MB<no constraint> 0001b2MB…0b 0010b4MB…00b 0011b8MB…000b 0100b16MB…0000b All other encodings are Reserved Based on the implemented FPB MEM Low Vector size, hardware is permitted to implement as RW only those bits of this field that can be programmed to non-zero values, in which case the upper order bits are permitted but not required to be hardwired to 0. If the FPB MEM Low Vector Supported bit is Clear, then it is permitted for hardware to implement this field as RO, and the value in this field is undefined. Default value for this field is 0000b.	RW/RO	0
0x60	FPB_CAP_4	19:8	Reserved	RsvdP	0
0x60	FPB_CAP_4	31:20	FPB MEM Low Vector Start - The value written by software to this field sets the base address at which the FPB MEM Low Vector is applied. Software must program this field to a value that is naturally aligned according to the value in the FPB MEM Low Vector Granularity Field as indicated in the description for that field (above). If this requirement is violated, the hardware behavior is undefined. If the FPB MEM Low Vector Supported bit is Clear, then it is permitted for hardware to implement this field as RO, and the value in this field is undefined. Default value for this field is 0000h.	RW/RO	0

Table 30. Flattening Portal Bridge (FPB) Registers

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x64	FPB_CAP_5	0	FPB MEM High Vector Enable - When Set, enables the FPB MEM High Vector mechanism. If the FPB MEM High Vector Supported bit is Clear, then it is permitted for hardware to implement this field as RO, and in this case the value in this field is undefined. Default value of this bit is 0b.	RW/RO	0
0x64	FPB_CAP_5	3:1	Reserved	RsvdP	0
0x64	FPB_CAP_5	7:4	FPB MEM High Vector Granularity - The value written by software to this field controls the granularity of the FPB MEM High Vector, and the required alignment of the FPB MEM High Vector Start Lower field (below). Software is permitted to select any allowed Granularity from the table below regardless of the value in the FPB MEM High Vector Size Supported field. Defined encodings are: ValueGranularityStart Alignment Constraint 0000b256MB<no constraint> 0001b512MB…0b 0010b1GB…00b 0011b2GB…000b 0100b4GB…0000b 0101b8GB…00000b 0110b16GB…000000b 0111b32GB…0000000b Based on the implemented FPB MEM High Vector size, hardware is permitted to implement as RW only those bits of this field that can be programmed to non-zero values, in which case the upper order bits are permitted but not re-quired to be hardwired to 0. If the FPB MEM High Vector Supported bit is Clear, then it is permitted for hardware to implement this field as RO, and the value in this field is undefined. Default value for this field is 0000b.	RW/RO	0
0x64	FPB_CAP_5	23:8	Reserved	RsvdP	0

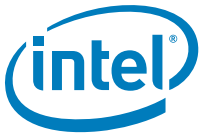


Table 30. Flattening Portal Bridge (FPB) Registers

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x64	FPB_CAP_5	31:24	FPB MEM High Vector Start Lower - The value written by software to this field sets the lower bits of the base address at which the FPB MEM High Vector is applied. Software must program this field to a value that is naturally aligned according to the value in the FPB MEM High Vector Granularity Field as indicated in the description for that field (above). If this requirement is violated, the hardware behavior is undefined. If the FPB MEM High Vector Supported bit is Clear, then it is permitted for hardware to implement this field as RO, and the value in this field is undefined. Default value for this field is 00h.	RW/RO	0
0x68	FPB_CAP_6	31:0	FPB MEM High Vector Start Upper - The value written by software to this field indicates bits 63:32 of the base address at which the FPB MEM High Vector is applied. If the FPB MEM High Vector Supported bit is Clear, then it is permitted for hardware to implement this field as RO, and the value in this field is undefined. Default value for this field is 00000000h.	RW/RO	0
0x6C	FPB_CAP_7	7:0	FPB Vector Access Offset - The value in this field indicates the offset of the 32b portion of the FPB BD, MEM Low or MEM High, Vector that can be read or written by means of the FPB Vector Access Data Register. The selection of BD, MEM Low or MEM High is made by the value written to the FPB Vector Select field of this register. The bits of this field map to the offset according to the value in the corresponding FPB Vector Size Supported field as shown here: Offset BitsThis Field 000b 2:02:0 (7:3 unused) 001b 3:03:0 (7:4 unused) 010b 4:04:0 (7:5 unused) 011b 5:05:0 (7:6 unused) 100b 6:06:0 (7 unused) 101b 7:07:0 All other encodings are Reserved Bits in this field that are unused per the table above must be written by software as 0b, and are permitted but not required to be implemented as RO. Default value for this field is 00h.	RW/RO	0
0x6C	FPB_CAP_7	13:8	Reserved	RsvdP	0

Table 30. Flattening Portal Bridge (FPB) Registers

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x6C	FPB_CAP_7	15:14	FPB Vector Select - The value written to this field selects the Vector to be accessed at the indicated FPB Vector Access Offset, encoded as: 00: BDF 01: MEM Low 10: MEM High 11: Reserved Default value for this field is 00b.	RW	0
0x6C	FPB_CAP_7	31:16	Reserved	RsvdP	0
0x70	FPB_CAP_8	31:0	FPB Vector Access Data - Reads from this register return the DW of data from the FPB Vector at the location determined by the value in the FPB Vector Access Offset Register. Writes to this register replace the DW of data from the FPB Vector at the location determined by the value in the FPB Vector Access Offset Register. Default value for this field is 0000h.	RW	0

4.3.9 Device Serial Number Capability

Figure 18 details the structure of the register fields for Device Serial Number registers and Table 31 describes the register's fields.

Figure 18. Device Serial Number Registers

Table 31. Device Serial Number Registers Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x100	DSN_CAP_0	31:0	PCI Express Enhance Capability Header	RO	0x20010003
0x104	DSN_CAP_1	31:0	Serial Number Register (Lower DW)	RO	0x00C9A000
0x108	DSN_CAP_2	31:0	Serial Number Register (Upper DW)	RO	0x01000000

4.3.10 Advanced Error Reporting Capability

Figure 19 details the structure of the register fields for Advanced Error Reporting registers and Table 32 describes the register's fields.

Figure 19. Advanced Error Reporting Registers

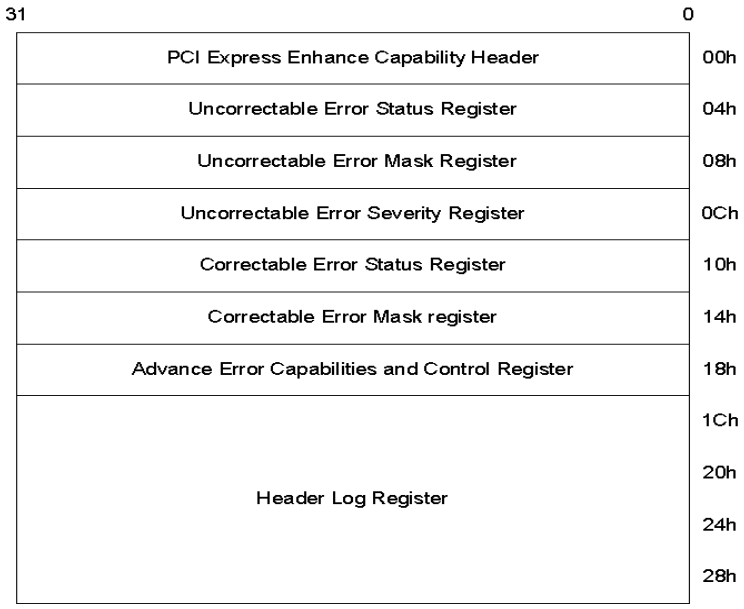


Table 32. Advanced Error Reporting Registers Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x200	AER_CAP_0	31:0	PCI Express Enhanced Capability Header	RO	0x30010001
0x204	AER_CAP_1	31:0	Uncorrectable Error Status Register	See PCIe Spec	0
0x208	AER_CAP_2	31:0	Uncorrectable Error Mask Register	See PCIe Spec	0
0x20C	AER_CAP_3	31:0	Uncorrectable Error Severity Register	See PCIe Spec	Up/Dn0x00462010 DMA EMEP - 0x00062010
0x210	AER_CAP_4	31:0	Correctable Error Status Register	See PCIe Spec	0
0x214	AER_CAP_5	31:0	Correctable Error Mask register	See PCIe Spec	0x00002000
0x218	AER_CAP_6	31:0	Advance Error Capabilities and Control Register	See PCIe Spec	0
0x21C	AER_CAP_7	31:0	Header Log Register 0	ROS	0
0x220	AER_CAP_8	31:0	Header Log Register 1	ROS	0
0x224	AER_CAP_9	31:0	Header Log Register 2	ROS	0
0x228	AER_CAP_10	31:0	Header Log Register 3	ROS	0

4.3.11 Virtual Channel Capability

Figure 20 details the structure of the register fields for Virtual Channel registers and Table 33 describes the register's fields.

Last three registers exist for VC0 and VC1. VC1 part can be configured as part of QoS feature support and also can be hidden in custom QoS support.

Figure 20. Advanced Error Reporting Registers

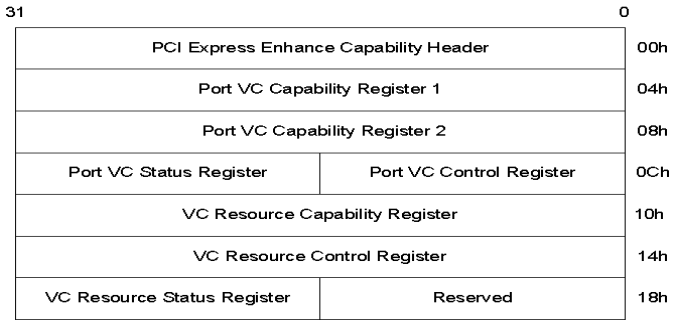


Table 33. Advanced Error Reporting Registers Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x300	VC_CAP_0	31:0	PCI Express Enhance Capability Header	RO	0x40010002
0x304	VC_CAP_1	31:0	Port VC Capability Register 1	RO	0
0x308	VC_CAP_2	31:0	Port VC Capability Register 2	RO	0
0x30C	VC_CAP_3	15:0	Port VC Control Register	3:0 -R/W 15:4 - RsvdP	0
0x30C	VC_CAP_3	31:16	Port VC Status Register	16 - RO 31:17 - RsvdZ	0
0x310	VC_CAP_4	31:0	VC Resource Capability Register	See PCIe Spec	0
0x314	VC_CAP_5	31:0	VC Resource Control Register	R/W *Reserved bits - RsvdP	0x800000FF
0x318	VC_CAP_6	15:0	Reserved	RsvdP	0
0x318	VC_CAP_6	31:16	VC Resource Status Register	17:16 - RO 31:18 - RsvdZ	0x0002
0x31C	VC_CAP_7	31:0	VC1 Resource Capability Register	See PCIe Spec	0
0x320	VC_CAP_8	31:0	VC1 Resource Control Register	R/W *Reserved bits - RsvdP	0
0x324	VC_CAP_9	15:0	Reserved	RsvdP	0
0x324	VC_CAP_9	31:16	VC1 Resource Status Register	17:16 - RO 31:18 - RsvdZ	0

4.3.12 Power Budgeting Capability

Figure 21 details the structure of the register fields for Power Budgeting registers and Table 34 describes the register's fields.

Figure 21. Power Budgeting Registers

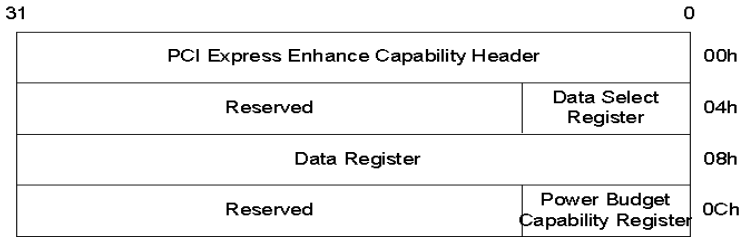


Table 34. Power Budgeting Registers Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x400	PB_CAP_0	31:0	PCI Express Enhance Capability Header	RO	0x50010004
0x404	PB_CAP_1	7:0	Data Select Register	R/W	0
0x404	PB_CAP_1	31:8	Reserved	RsvdP	0
0x408	PB_CAP_2	31:0	Data Register	RO	0x00078200
0x40C	PB_CAP_3	7:0	Power Budget Capability Register	0- HwInit 7:1- RsvdP	0
0x40C	PB_CAP_3	31:8	Reserved	RsvdP	0

4.3.13 Vendor Specific Enhanced Capability

Table 35 describes the Vendor Specific Enhanced register's fields. These registers contain general purpose bits: different modes, dft bits and chicken bits. Vendor Registers might be loaded from FLASH.

Legacy Vendor Registers (Titan Ridge):

"Reg 0 (0x8) - General configuration register

"Reg 1 (0xC) - General configuration register

"Reg 2 (0x10) - General configuration register

"Reg3 (0x14) - Power Budget register

"Reg4 (0x18) - Custom Hot Plug / BIOS register

"Reg5 (0x1C) - General configuration register

"Reg6 (0x20) - General configuration register

"Reg7 (0x24) - Custom NVM register

"Reg8 (0x28) - DFT register 1 (RO)

"Reg9 (0x2C) - DFT register 2 (RW)

"Reg10 (0x30) - Custom Reg access (Command Register)

"Reg11 (0x34) - Custom Reg access (Write Data Register)

"Reg12 (0x38) - Custom Reg access (Read Data Register)

"Reg13 (0x3C) - Custom LTR register 1

"Reg14 (0x40) - Custom LTR register 2

"Reg15 (0x44) - Custom LTR register 3

"Reg16 (0x48) - Custom Vendor Register 1 (RO)

"Reg17 (0x4C) - Custom Vendor Register 2 (RW)

"Reg18 (0x50) - CAB VC0 Register

"Reg19 (0x54) - CAB VC1 Register

"Reg20 (0x58) - QoS configuration register (empty)

"Reg21 (0x5C) - QoS Load priority & Custom mode register

"Reg22 (0x60) - QoS Shadow and VC Control Registers

"Reg23 (0x64) - QoS Tx / Rx TC Remapping Register

"Reg24 (0x68) - QoS Rx Remap Table (Entry0)

"Reg25 (0x6C) - QoS Rx Remapping Table (Entry1)

"Reg26 (0x70) - QoS Rx Remapping Table (Entry2)

"Reg27 (0x74) - QoS Rx Remapping Table (Entry3)

"Reg28 (0x78) - QoS Rx Remapping Table (Entry4)

"Reg29 (0x7C) - QoS Rx Remapping Table (Entry5)

"Reg30 (0x80) - QoS Rx Remapping Table (Entry6)

"Reg31 (0x84) - QoS Rx Remapping Table (Entry7)

"Reg32 (0x88) - Custom Port Arbitration register 1

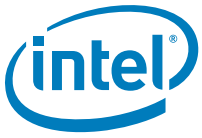
"Reg33 (0x8C) - Custom Port Arbitration register 2

"Reg34 (0x90) - General configuration register

"Reg35 (0x94) - Custom PTM register 1

"Reg36 (0x98) - Custom PTM register 2

"Reg37 (0x9C) - Custom PTM register 3



"Reg38 (0xA0) - Custom L2 feature register

"Reg39 (0xA4) - Custom Compliance Pattern register 1

"Reg40 (0xA8) - Custom Compliance Pattern register 2

"Reg41 (0xAC) - General configuration register

"Reg42 (0xB0) - General configuration register

"Reg43 (0xB4) - General configuration register

"Reg44 (0xB8) - General configuration register

"Reg45 (0xBC) - General configuration register

"Reg46 (0xC0) - General configuration register

"Reg47 (0xC4) - General configuration register

"Reg48 (0xC8) - General configuration register

"Reg49 (0xCC) - General configuration register

"Reg50 (0xD0) - General configuration register

"Reg51 (0xD4) - General configuration register

"Reg52 (0xD8) - General configuration register

"Reg53 (0xDC) - General configuration register

"Reg54 (0xE0) - General configuration register

"Reg55 (0xE4) - General configuration register

"Reg56 (0xE8) - General configuration register

"Reg57 (0xEC) - General configuration register

"Reg58 (0xF0) - General configuration register

"Reg59 (0xF4) - Custom L1 Sub-state register (Upstream Port)

"Reg60 (0xF8) - General configuration register

"Reg61 (0xFC) - General configuration register

Table 35. Vendor Specific Enhanced Registers Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x500	VS_CAP_0	31:0	PCI Express Enhance Capability Header	RO	0x6001000B
0x504	VS_CAP_1	31:0	Vendor Specific Header	RO	0x10018086
0x508	VS_CAP_2	31:0	Vendor Register 0 (VESC_REG0)	R/W	See following tables

Table 35. Vendor Specific Enhanced Registers Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
…	…	31:0	…	R/W	See following tables
0x5FC	VS_CAP_63	31:0	Vendor Register 61 (VESC_REG61)	R/W	See following tables

Table 36. VESC_REG0 (Offset 08h): General configuration register

Offset	Bits	Description	Value
0x508	vesc_reg0[13:0]	**Replay timer value** (in units of clocks) · Gen1 – 16ns · Gen2 – 8ns · Gen3 – 4ns Loaded when bit 31 is written	**14'h450** 14'h550 - CIO
0x508	vesc_reg0[14]	**TXSwing control** 1'b0: PHY is directed to be in Full swing mode (default). 1'b1: PHY is directed to be in Low swing mode.	1'b0
0x508	vesc_reg0[16:15]	**Loopback_control** (DFT) 2'b01: loopback end 2'b10: loopback start	2'b0
0x508	vesc_reg0[17]	**Clkreq_p0top2** 1'b0: MAC moves the PHY to P1 during clkreq# transition. 1'b1: MAC moves the PHY to P2 during clkreq# transition.	1'b0
0x508	vesc_reg0[18]	**enab_urcomp_typ0cfgrd_busnum_mismatch** 1'b0: Bus Num is not checked in Type0 CfgRd. 1'b1: Port sends Cmpl with UR status when the destination bus number in Type0 CfgRd doesn't match the actual bus number of the port (This bit is valid only for Up/EP, and reserved for Dn ports)	(Up/EP) 1'b0
0x508	vesc_reg0[19]	**Virtual Gen2/Gen3 Enable** 1'b0: Enables indication to the port that it in Gen1 running with Gen2/Gen3 clocks rate. 1'b1: Ports counters are according to it's rate	1'b0

Table 36. VESC_REG0 (Offset 08h): General configuration register

Offset	Bits	Description	Value
0x508	vesc_reg0[20]	**enable_expectValidTLP** 1'b0: No Filtering STP 1'b1: Filtering of STP on certain states when no TLP is expected (to prevent error status bits setting)	**1'b1**
0x508	vesc_reg0[21]	**detect_missingEOP_after4K** 1'b0: Missing End of Packet is detected after Max Payload Size value programmed by software. 1'b1: Missing End of Packet is detected after 4K bytes	**1'b1**
0x508	vesc_reg0[22]	**Select_gen1_gen2** 1'b0: No effect 1'b1: Force Port to stay in Gen1 during Link negotiation	(DFT) 1'b0
0x508	vesc_reg0[23]	**enable_eidleinfer_dllp** 1'b0: L0 Electrical Idle inference lack of SKIP received 1'b1: L0 Electrical Idle inference lack of SKIP/DLLP received Related to other chicken bit (vesc_reg6[31]) - If vesc_reg6[31] = 1 this bit must stay 1	**1'b1** (Sim - rand)
0x508	vesc_reg0[24]	**RxInL0s_L1ASPM_enable** 1'b0: L0sRx is not a condition for L1 ASPM entry. 1'b1: Port must be in L0sRx to start L1 ASPM entry (This bit is valid only for Up/EP, and reserved for Dn ports)	(Up/EP) 1'b0 (Sim - rand)
0x508	vesc_reg0[25]	**disab_autospdchng_dncomp** 1'b0: Up/EP initiates Speed Change after Init FC is completed. 1'b1: Disables auto speed change (This bit is valid only for Up/EP, and reserved for Dn ports)	(Up/EP) 1'b0
0x508	vesc_reg0[26]	**L2_Det_Qual** 1'b0: the “Detect” state of Downstream Port won’t be taken in consideration while entering L2 1'b1: the “Detect” state of Downstream Port will be taken in consideration while entering L2 (This bit is valid only for Up, and reserved for Dn ports)	(Up) **1'b1**

Table 36. VESC_REG0 (Offset 08h): General configuration register

Offset	Bits	Description	Value
0x508	vesc_reg0[27]	**L0sL1_Det_Qual** 1'b0: the "Detect" state of Downstream Port won't be taken in consideration while entering L1 1'b1: the "Detect" state of Downstream Port will be taken in consideration while entering L1 (This bit is valid only for Up, and reserved for Dn ports)	(Up) **1'b1**
0x508	vesc_reg0[28]	**Lane negotiation method** 1'b0 – dynamic lane negotiation (according to data) 1'b1 – static lane negotiation (according to xmode input)	1'b0
0x508	vesc_reg0[29]	**cb_clk_req_upon_l1_or_en** 1'b0 – Clock Request looks at Idle state of Port 1'b1 – Clock Request looks at L1 state. (This bit is valid only for Dn, and reserved for Up/EP ports)	1'b0
0x508	vesc_reg0[30]	**Endpoint** Reset 1'b0: No Effect 1'b1: Endpoint device which connected to this Downstream Port will be reset (static bit) (This bit is valid only for Dn, and reserved for Up/EP ports)	(Dn) 1'b0
0x508	vesc_reg0[31]	**Load replay timer value** When software writes 1 to bit 31, the value in bits [13:0] will get loaded into the internal replay timer register.	(Self-Cleared) 1'b0

Table 37. VESC_REG1 (Offset 0Ch): General configuration register

Offset	Bits	Description	Value
0x50C	vesc_reg1[0]	**Switch cut-thru disable** 1'b0: The decision to use cut-thru or store-forward mode on each port depends on the port rate and width 1'b1: The switch port will use store-forward mode always.	**1'b1**
0x50C	vesc_reg1[1]	**Enable_wake** 1'b0: No effect 1'b1: WAKE# is used to wake from L2	1'b0
0x50C	vesc_reg1[2]	**Enable_beacon** 1'b0: No effect 1'b1: Beacon is used to wake from L2	1'b0

Table 37. VESC_REG1 (Offset 0Ch): General configuration register

Offset	Bits	Description	Value
0x50C	vesc_reg1[3]	**L1_ASPM override** 1'b0: No Effect 1'b1: L1 is disabled if configured by SW	1'b0/**1'b1** (Sim – flow)
0x50C	vesc_reg1[4]	**L0STX Override** 1'b0: No Effect 1'b1: L0STX is disabled if configured by SW	**1'b1** (Sim – flow)
0x50C	vesc_reg1[5]	**ClkReq Override** 1'b0: Internal clock request functionality is enabled 1'b1: Disable internal clock request functionality	**1'b1**
0x50C	vesc_reg1[7:6]	**losl1_timer_value** L1 entry timer select (Idle or L0sTx if enabled) 2'b00 - 4us → 8us (in TR) 2'b01 - 8us → 12us (in TR) 2'b10 - 12us → 16us (in TR) 2'b11 - 16us → 20us (in TR) (This bit is valid only for Up/EP, and reserved for Dn ports) Periodic FC is 30us so even if L0sTx is enabled the max value configuration is valid.	(Up/Ep) **2'h10** (Sim – rand)
0x50C	vesc_reg1[8]	**Bypass_RxL0sTimer for_L1_disable** 1'b0: Port doesn't waits in L0sRx, before starting L1. 1'b1: Port waits some configurable time in L0sRx (bits 7:6), before starting L1 ASPM. (This bit is valid only for Up/EP, and reserved for Dn ports)	1'b0 (Sim – rand)
0x50C	vesc_reg1[9]	**L1_RXEleIdle_TO_setting** Timeout value for L1ASPM state machine to wait for Rx Electrical Idle condition. 1'b0: Times out after 5 us. 1'b1: Times out after 10 us.	**1'b1** (Sim – rand)

Table 37. VESC_REG1 (Offset 0Ch): General configuration register

Offset	Bits	Description	Value
0x50C	vesc_reg1[10]	**nonL0_rxelec_mask** 1'b0: No effect 1'b1: Correctable error message generation and setting the correctable error status bit is disabled during the conditions when the link is in a non-L0 state and when Rx EI detected. (to prevent errors near EI transitions)	**1'b1**
0x50C	vesc_reg1[11]	**In L0sTx state** Hardware sets this bit when it enters L0sTx. Software can clear it by writing 1 to it.	1'b0
0x50C	vesc_reg1[12]	**In L0sRx state** Hardware sets this bit when it enters L0sRx. Software can clear it by writing 1 to it.	1'b0
0x50C	vesc_reg1[13]	**In L1 state** Hardware sets this bit when it enters L1. Software can clear it by writing 1 to it.	1'b0
0x50C	vesc_reg1[14]	**In L2 state** Hardware sets this bit when it enters L2. Software can clear it by writing 1 to it.	1'b0
0x50C	vesc_reg1[15]	**Fast Port Cut-Through Fix disable** 1’b0: Fast Port is in Cut-Thru mode to reduce Latency 1’b1: Disable the fix Cut-Thru mode in case of fast port (Fast Port is relatively to other Ports)	1'b0
0x50C	vesc_reg1[16]	**disab_vga_routing** 1'b0: vga_routing is enabled when vga_en bit is set by SW. 1'b0:vga routing is disabled even if vga_en bit is set by SW.	1'b0
0x50C	vesc_reg1[17]	**disab_isa_routing** 1'b0: ISA_routing is enabled when isa_en bit is set by SW. 1'b1: ISA routing is disabled even if isa_en bit is set by SW.	1'b0
0x50C	vesc_reg1[18]	**RXDetect_Bypass** 1'b0: RX Detection logic is NOT bypassed 1'b1: RX Detection logic is bypassed (DFT)	1'b0

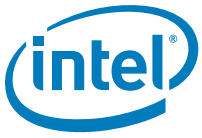


Table 37. VESC_REG1 (Offset 0Ch): General configuration register

Offset	Bits	Description	Value
0x50C	vesc_reg1[19]	**l0srx_ctrbypass_enable** 1'b0: Counter not bypassed 1'b1: In L0SRx state machine counter is bypassed when Rx EI condition is detected.	**1'b1**
0x50C	vesc_reg1[20]	**PresenceDet_enable** 1'b0: No effect 1'b1: Transitions from L0 to Recovery, and from Recovery to Detect state are accelerated when Presence = 0	**1'b1**
0x50C	vesc_reg1[21]	**bypass_inl1** 1'b0: Port condition to be in L1 will NOT be bypassed 1'b1: Port condition to be in L1 will be bypassed	1'b0/**1'b1** (Sim – flow)
0x50C	vesc_reg1[22]	**bypass_inl0srx** 0: Port condition to be in L0SRX will NOT be bypassed. 1: Port condition to be in L0SRX will be bypassed.	1'b0/**1'b1** (Sim – flow)
0x50C	vesc_reg1[23]	**losl1_timer_value_inms** L1 entry timer unit control 1'b0: bits[7:6] unit is in us 1'b1: bits[7:6] unit is in ms (DFT) (This bit is valid only for Up/EP, and reserved for Dn ports)	(Up/Ep) 1'b0
0x50C	vesc_reg1[24]	**WAKE_pinB_qual** 1'b0: WAKE_pinB is not used to exit from L2 1'b1: WAKE_pinB is used to exit from L2. (This bit is valid only for Dn, and reserved for Up/EP ports)	1'b0
0x50C	vesc_reg1[25]	**Vendor_IOSpace_dis** 1'b0: IO space is enabled. 1'b1: IO space is disabled. Following registers will return zero when accessed by software.	1'b0

Table 37. VESC_REG1 (Offset 0Ch): General configuration register

Offset	Bits	Description	Value
0x50C	vesc_reg1[26]	**l2eidlewait_en** 1'b0: During L2 entry Port wait for partner to enter electrical idle before sending EIOS and entering EI. 1'b1: During L2 entry Port doesn't wait for partner and enters electrical idle on its own timing. (This bit is valid only for Dn, and reserved for Up/EP ports)	(Dn) 1'b0
0x50C	vesc_reg1[27]	**hotrstexit_timer_en** 1'b0: Waits for Rx electrical idle to make a transition from Hot Reset to Detect (Bug) 1'b1: exit to DETECT after 2ms timer expired and no Electrical Idle detected within that period (Bug Fix) (This bit is valid only for Dn, and reserved for Up/EP ports)	(Dn) **1'b1**
0x50C	vesc_reg1[28]	**LinkWidthCap_selection** Link Width in Link Capability register selection control 1'b0: Set according to xmode input 1'b1: Set according to EEPORM load	1'b0
0x50C	vesc_reg1[29]	**rcvrcfgtoidle_send32tsx_en** Number of Tx TS2 during Recover.Config to Recovery.Idle transition. 34 TSx instead of 18. 1'b0: 18 TS2 are sent (default – according to Spec (16)) 1'b1: 34 TS2 are sent (DFT)	1'b0
0x50C	vesc_reg1[30]	**rcvrcfgtoidle_rcv4tsx_en** Expected Number of Rx TS2 during Recover.Config to Recovery.Idle transition. 1'b0: 8 TS2 expected (default – according to the Spec) 1'b1: 4 TS2 expected (DFT)	1'b0
0x50C	vesc_reg1[31]	**cb_pme_err_message_dis** 1'b0: PostReqProcVC0 block is blocked from sending extra credit update for PM_PME message (Bug fix) 1'b1: PostReqProcVC0 sends extra credit update for PM_PME message (Bug)	1'b0

Table 38. VESC_REG2 (Offset 10h): General configuration register

Offset	Bits	Description	Value
0x510	vesc_reg2[0]	**Disable constant Clock Request Ack** 1'b0: Clock request Ack is constant high. 1'b1: Clock request Ack is generated from delayed request.	1'b0
0x510	vesc_reg2[1]	**Power Down Delay Enable** Delay of Power Down signal in case of Lane Reversal 1'b0: No effect 1'b1: Internal PIPE PowerDown signal delay of one cycle.	1'b0
0x510	vesc_reg2[3:2]	**L0sTx Timeout select** 2'b00: 12 2'b01:9 2'b10:6 2'b11:4	2'b0
0x510	vesc_reg2[7:4]	**L1 Entry Delay Counter** Delays entry to L1 for configurable time: 4'h0 – No Delay, 4'h1 - ~1ms, 4'h2 - ~2ms, 4'h3 - ~4ms 4'h4 – ~8ms, 4'h5 – ~16ms, 4'h6 – ~64ms, 4'h7 – ~128ms 4'h8 – ~256ms, 4'h9 – ~0.5 sec, 4'hA – ~1 sec, 4'hB – ~2sec 4'hC – ~4 sec, 4'hD – ~8 sec, 4'hE – ~16 sec, 4'hF - ~32 sec	4'h0
0x510	vesc_reg2[8]	**DFT PME generation** 1'b0: No effect 1'b1: Sends PM_PME message till SW clears PME_Status	1'b0
0x510	vesc_reg2[9]	**Disable Bus Capture from Host Interface** 1'b0: Capture Bus and Dev Num only from PHY access 1'b1: Capture Bus and Dev Num from PHY / Host access. (This bit is valid only for Dn and reserved for Up/EP ports)	(Dn) 1'b0
0x510	vesc_reg2[10]	**Host_datataken_datavalid chicken bit** 1'b0: Backdoor register access bug is fixed. 1'b1: Backdoor register access bug fix is disabled.	1'b0

Table 38. VESC_REG2 (Offset 10h): General configuration register

Offset	Bits	Description	Value
0x510	vesc_reg2[11]	**cb_Ltr_value _maxlimit** (LTR) 1'b0: Max LTR register doesn't limit the LTR final value. 1'b1: Max LTR register limits the LTR final value. (This bit is valid only for Up/EP and reserved for Dn ports)	(Up/EP) **1'b1**
0x510	vesc_reg2[12]	**cb_rxexit_duetorecov** 1'b0: Port waits for periodic FC update to exit L0sRx before it can initiate Link Retrain. 1'b1: Port immediately exits from L0Srx and initiate Link Recovery (This bit is valid only for Dn and reserved for Up/EP ports)	(Dn) **1'b1**
0x510	vesc_reg2[13]	**cb_dynltr_sel** (LTR) Selects between static and dynamic LTR value for Switch down ports that are connected with non-LTR capable EPs 1'b0: Dynamic LTR value 1'b1: Static LTR value (This bit is valid for Dn ports)	(Dn) **1'b1**
0x510	vesc_reg2[16:14]	**cb_prog_cons8count_value** (DFT) Number of consecutive TS to be considered as 8. 3'h1 – two TS … 3'h7 – eight TS (Valid if bit 17 is set)	**3'h6**
0x510	vesc_reg2[17]	**cb_prog_cons8count_enable** 1'b0: Eight consecutive TS indication is set upon 8 TS. 1'b1: Enables Eight consecutive TS indication to be programmable (bits 16:14)	**1'b1**
0x510	vesc_reg2[19:18]	**cb_replay_numlimit_sel** (DFT) Selects the number of Replays till Recovery 2'b00: 16 2'b01: 32 2'b10: 64 2'b11: 256 (Valid if bit 21 is set)	2'b0

Table 38. VESC_REG2 (Offset 10h): General configuration register

Offset	Bits	Description	Value
0x510	vesc_reg2[20]	**cb_replay_norecov** (DFT) 1'b0: Port goes to Recovery after 4 Replays (Spec) 1'b1: Port never goes to Recovery as a result of Replays (Valid if bit 21 is set)	1'b0
0x510	vesc_reg2[21]	**cb_master_replay** (DFT) 1'b0: No effect 1'b1: Enable for Replay manipulations (bits 20:18)	1'b0
0x510	vesc_reg2[22]	**cb_extrenal_pme disable** 1'b0: No effect 1'b1: Disables PME generation	1'b0
0x510	vesc_reg2[23]	**cb_false_linkdown** 1'b0: No effect 1'b1: Forces a Port to report link down condition (This bit is valid only for Dn, and reserved for Up/EP ports)	(Dn) 1'b0
0x510	vesc_reg2[24]	**cb_disable_l1soft** 1'b0: L1 Software is active (according to D-state) 1'b1: L1 Software is disabled (DFT) (This bit is valid only for Up/Ep and reserved for EP ports)	(Up/Ep) 1'b0
0x510	vesc_reg2[25]	**cb_regacc_disable** 1'b0: Configuration Space can be accessed through backdoor interface. 1'b1: Disables alternate backdoor register access feature	1'b0
0x510	vesc_reg2[26]	**cb_ltr_disable** (LTR) 1'b0: LTR is controlled by Software. 1'b1: Disables LTR feature (hide Capability).	1'b0
0x510	vesc_reg2[27]	**cb_disab_redunrecov** 1'b0: Redundant recovery fix is enabled. 1'b1: Redundant recovery fix is disabled.	1'b0
0x510	vesc_reg2[28]	**cb_bypass_creditchk** (QoS) 1'b0: default behavior when there is no QoS custom modes 1'b1: Bypass credit check when ingress port has VC1 enabled and egress port is custom VC0 only mode.	1'b0 **(QoS – 1'b1)**

Table 38. VESC_REG2 (Offset 10h): General configuration register

Offset	Bits	Description	Value
0x510	vesc_reg2[29]	**disable_ecrc_fix** 1'b0: ECRC fix of FC loss is enabled 1'b1: ECRC fix is disabled	1'b0
0x510	vesc_reg2[30]	**cb_enable_vc1** (QoS) 1'b0: VC1 is disabled in PCIE Switch. 1'b1: VC1 in enabled in PCIE Switch. (This bit is valid only for Up and reserved for Dn/EP ports)	(Up) **(QoS – 1'b1)**
0x510	vesc_reg2[31]	**Disable Hot Reset fix over Tunnel** 1'b0: Hot Reset bug over tunnel is fixed, Port doesn't assert logic idle wait if directed to Hot Reset. 1'b1: Hot Reset bug over tunnel is not fixed	1'b0

Table 39. VESC_REG 3 (Offset 14h): General configuration register

Offset	Bits	Description	Value
0x510	vesc_reg3[7:0]	**D0_MAX_3P3V_BASE_PWR** Provides the max power consumption in D0 state from 3.3V power supply. Total power consumption is this value times scale (0.01)	8'h0
0x510	vesc_reg3[15:8]	**D0_SUSTAINED_3P3V_BASE_PWR** Provides the sustained power consumption in D0 state from 3.3V power supply. Total power consumption is this value times scale (0.01)	8'h0
0x510	vesc_reg3[23:16]	**D3_MAX_3P3V_BASE_PWR** Provides the max power consumption in D3 state from 3.3V power supply. Total power consumption is this value times scale (0.01)	8'h0
0x510	vesc_reg3[31:24]	**D3_SUSTAINED_3P3V_BASE_PWR** Provides the sustained power consumption in D3 state from 3.3V power supply. Total power consumption is this value times scale (0.01)	8'h0

Table 40. VESC_REG 4: (Offset 18h): Custom Hot Plug / BIOS register

Offset	Bits	Description	Value
0x518	vesc_reg4[31:0]	Custom use	32'h0

Table 41. VESC_REG 5: (Offset 1Ch): General configuration register

Offset	Bits	Description	Value
0x51C	vesc_reg5[0]	**cb_dynamic_sw_rate_change_dis** 1'b0: Cut-through is disabled 20 clks after sw clk speed change 1'b0: The fix to disable Cut-through is disabled (This bit is used only in Upstream and effects the whole switch)	1'b0 (Up)
0x51C	vesc_reg5[1]	**d0u_hot_plug_fix_en** 1'b0: D0U is not considered in Hot Plug PM PME generation 1'b1: D0U is considered during Hot Plug PM PME generation (This bit is valid only for Dn and reserved for Up/EP ports)	(Dn) **1'b1**
0x51C	vesc_reg5[2]	**LTR close msg fix disable** (LTR) 1'b0 – close ltr Message handling enabled 1'b1 – close ltr Message handling disabled	1'b0
0x51C	vesc_reg5[3]	**LTR extra msg fix disable** (LTR) 1'b0 – Does not send duplicate ltr message 1'b1 – sends duplicate ltr message	1'b0
0x51C	vesc_reg5[4]	**cb_l2_rate_fix_en** 1'b0 – In L2 flow, does speed change only at Detect (bug) 1'b1 – Does speed change in before entry L2.Idle	**1'b1**
0x51C	vesc_reg5[5]	**Exit from L2 on PERST#** 1'b0 – Do not exit from L2 when PCIRST is there. 1'b1 – Exit from L2 when PCIRST is there. (This bit is valid only for Up/EP and reserved for Dn ports)	(Up/Ep) **1'b1**
0x51C	vesc_reg5[6]	**L1 entry during L2 fix disable** 1'b0 – Port doesn't enter L1 ASPM if L2L3 is in progress 1'b1 – Port enter L1 ASPM if L2L3 is in progress (bug) (This bit is valid only for Up/EP and reserved for Dn ports)	(Up/Ep) 1'b0

Table 41. VESC_REG 5: (Offset 1Ch): General configuration register

Offset	Bits	Description	Value
0x51C	vesc_reg5[7]	**L0s entry during L1/L2 fix disable** 1'b0 – Port doesn't enter L0sTx if L2L3 or L1 is in progress 1'b1 – Port enter L0sTx ASPM if L2L3 or L1 in progress (bug)	1'b0
0x51C	vesc_reg5[8]	**L1 Soft exit timer fix disable** 1'b0: Dn Port does not wait for 1.5 ms during L1 soft exit 1'b1: Dn Port waits for 1.5 ms during L1 soft exit (bug) (This bit is valid only for Dn and reserved for Up/EP ports)	(Dn) 1'b0
0x51C	vesc_reg5[9]	**LTR dependency on Dn fix** 1'b0: LTR message will be sent only if at least one downstream port received LTR message from Endpoint device 1'b1: Fix that doesn't check if LTR message was received once (This bit is valid only for Up and reserved for Dn/EP ports)	(Up) **1'b1**
0x51C	vesc_reg5[10]	**LTR dependency on Dn fix** 1'b0: if any of downstream ports is locked there is no need to receive at least one LTR message to send one 1'b1: LTR message will be sent only if at least one downstream port received LTR message from Endpoint device (This bit is valid only for Up and reserved for Dn/EP ports)	1'b0
0x51C	vesc_reg5[11]	**Disable TLP Event in Fifo** 1'b0: New TLP event is done through FIFO for rate change. 1'b1: Previous method of transferring the New TLP Event.	1'b0
0x51C	vesc_reg5[12]	**Disable peer to peer ordering fix** 1'b0: Peer to Peer ordering issue is fixed 1'b1: Peer to Peer Ordering issue is not fixed (This bit is valid only for Dn and reserved for Up/EP ports)	(Dn) 1'b0

Table 41. VESC_REG 5: (Offset 1Ch): General configuration register

Offset	Bits	Description	Value
0x51C	vesc_reg5[13]	**cb_l2_emep_phystatus_en** 1'b0: Do not exit from TRANSIT_P1 state of L2SeqWake FSM. 1'b1: Exit from TRANSIT_P1 state of L2SeqWake FSM. (This bit is valid only for Up/Ep and reserved for Dn ports)	Up/Dn – 1'b0 USB Ep – 1'b0 DMA Ep – 1'b0 **(B-Step)**
0x51C	vesc_reg5[14]	**cb_LTR_nonzeroTC_dis** 1'b0: Flags a Malformed TLP upon LTR Msg with non-zero TC. 1'b1: Port does not flag a Malformed TLP upon LTR Msg with non-zero TC.	(Dn) 1'b0
0x51C	vesc_reg5[15]	**cb_LTR_notexpected_dis** 1'b0: Port flags a Malformed TLP upon LTR Msg. 1'b1: Port does not flag a Malformed TLP upon LTR Msg. (This bit is valid only for Up/EP and reserved for Dn ports)	(Up/Ep) 1'b0
0x51C	vesc_reg5[16]	**cb_nonzro_TC_msg_acpt** 1'b0: Do not Accept Msg TLP's with non zero TC.Flag it as Malformed TLP. 1'b1: Accept TLP's with non zero TC.Do not Flag it as Malformed TLP.	1'b0
0x51C	vesc_reg5[17]	**cb_idle_to_rlock_disable_invert** 1'b0: Cfg.Idle to Recovery transition is fixed 1'b1: Bug in transition from Cfg.Idle to recovery	1'b0
0x51C	vesc_reg5[18]	**cb_low_addr_fix_disable** 1'b0: Lower address and byte count of UR CPL is fixed 1'b1: Bad Lower address and byte count of UR CPL is fixed	1'b0
0x51C	vesc_reg5[19]	**cb_disable_swdn_rcvd_beacon** 1'b0: Detection Beacon during L2 is active 1'b1: Disables Beacon Detection (This bit is valid only for Dn and reserved for Up/EP ports)	(Dn) 1'b0

Table 41. VESC_REG 5: (Offset 1Ch): General configuration register

Offset	Bits	Description	Value
0x51C	vesc_reg5[20]	**cb_fts_ext_sync_3k_or_4k** Selects the number of transmitted FTS extended sync bit 1'b0: 4095 1'b1: 3000	**1'b1**
0x51C	vesc_reg5[21]	**cb_update_fc_maltlp_en** 1'b0: Port doesn't update FC credits for malformed TLP's 1'b1: Port updates FC credits for malformed TLP's	1'b0
0x51C	vesc_reg5[22]	**cb_obff_enable_wr_en** 1'b0: OBFF enable is not writable 1'b1: OBFF enable is still writable (feature is not supported)	1'b0
0x51C	vesc_reg5[23]	**cb_aspm_speed_chg_disable** 1'b0: Speed Change fix during ASPM Prep is enabled 1'b1: Speed Change fix during ASPM Prep is disabled	1'b0
0x51C	vesc_reg5[24]	**cb_tcvc_mapping_shadow_disable** (QoS) 1'b0: TC/VC mapping is done with shadow VC1 register 1'b1: TC VC mapping is done with spec VC1 register	1'b0 **(QoS - 1'b1)**
0x51C	vesc_reg5[25]	**cb_eidle_infer_disable** 1'b0: The issue of Idle inference is fixed. 1'b1: The issue of Idle inference is not fixed. (This disables a fix in EI inferring and not the feature)	1'b0
0x51C	vesc_reg5[26]	**cb_eidle_infer_anylane_disable** 1'b0: The issue of Idle inference for any lane is fixed. 1'b1: The issue of Idle inference for any lane is not fixed.	1'b0
0x51C	vesc_reg5[27]	**cb_crdtchk_hdr_arb_fix_disable_chan0** 1'b0: The hdr threshold on channel 0 is 'd1 1'b1: The hdr threshold on channel 0 is 'd2	1'b0
0x51C	vesc_reg5[28]	**cb_crdtchk_hdr_arb_fix_disable_chan1** 1'b0: The hdr threshold on channel 1 is 'd1 1'b1: The hdr threshold on channel 1 is 'd2	1'b0
0x51C	vesc_reg5[29]	**cb_crdtchk_data_arb_fix_disable_chan1** 1'b0: The hdr threshold on channel 1 is 'd8 1'b1: The the hdr threshold on channel 1 is 'd16	1'b0

Table 41. VESC_REG 5: (Offset 1Ch): General configuration register

Offset	Bits	Description	Value
0x51C	vesc_reg5[30]	**cb_crdtchk_hdr_arb_fix_disable_chan2** 1'b0: The hdr threshold on channel 2 is ‘d1 1'b1: The hdr threshold on channel 2 is ‘d2	1'b0
0x51C	vesc_reg5[31]	**cb_crdtchk_data_arb_fix_disable_chan2** 1'b1: The hdr threshold on channel 2 is ‘d16 1'b0: The hdr threshold on channel 2 is ‘d8	1'b0

Table 42. VESC_REG 6: (Offset 20h): General configuration register

Offset	Bits	Description	Value
0x520	vesc_reg6[0]	**cb_eieos_32_rcvrcfglock_enable** – Default 1’b0 1'b0: EIEOE in RCVR.CFG is sent after every 33 TS in (non Gen1) 1'b1: EIEOS in RCVR.CFG is sent after every 32 TS in (non Gen1)	**1'b1**
0x520	vesc_reg6[1]	**cb_eieos_32_rcvrlock_enable** – Default 1’b0 1'b0: EIEOE in RCVR.CFG is sent after every 31 TS in (non Gen1) 1'b1: EIEOS in RCVR.CFG is sent after every 32 TS in (non Gen1)	**1'b1**
0x520	vesc_reg6[2]	**cb_eieos_cfg_first_TS_enable** – Default 1’b0 1'b1: EIEOS in is not sent CFG.LINKWIDTHSTART before first TS. 1'b1: EIEOS in CFG.LINKWIDTHSTART is sent before first TS.	**1'b1**
0x520	vesc_reg6[3]	**cb_eidle_pulse_fix_enable –** Default 1’b0 1'b0: Tx Elec Idle pulse occurs when in Detect state 1'b1: Fix to eliminate Tx Elec Idle pulse when in Detect state.	**1'b1**
0x520	vesc_reg6[4]	**cb_ln0_LinkNum_fix_enable–** Default 1’b0 1'b0: Rcved TS Link Number is checked only on Ln0 1'b1: Rcved TS Link Number is checked on all lanes (The Bug is fixed in Recovery State)	1'b0
0x520	vesc_reg6[5]	**cb_updtltr1_lockmask_unset_enable** (LTR) 1'b0: LTR1 register in Downstream ports is not updated when LTR1 lock or mask bits are unset. 1'b1: LTR1 register in Downstream ports is updated when LTR1 lock or mask bits are unset.	**1'b1**

Table 42. VESC_REG 6: (Offset 20h): General configuration register

Offset	Bits	Description	Value
0x520	vesc_reg6[6]	**cb_max_val_chg_sndltr_enable** (LTR) 1'b0: Doesn't send LTR Message from EndPoint (EMEP) if max ltr register change causes a change in the latency value. (This bit is valid only for Ep and reserved for Up/Dn ports) 1'b1: Send LTR Message from if max ltr register change causes a change in the latency value.	(Ep) **1'b1**
0x520	vesc_reg6[7]	**cb_notlimit_lswitch_enable** (LTR) 1'b0: Lswitch value is limited to 20% (25%) of LTR Dn min (Bug) 1'b1: Lswitch value is not limited to 20% (25%) of LTR Dn min (This bit is valid only for Up and reserved for Dn/Ep ports)	(Up) **1'b1**
0x520	vesc_reg6[8]	**cb_noreq_bit_ltr1_nonD0_enable** (LTR) 1'b0: The LTR requirement stays high upon entry to non-D0 state high if Port in locked (Bug) 1'b0: The LTR requirement get reset upon entry to non-D0 state high if Port in locked (This bit is valid only for Dn and reserved for up/Ep ports)	(Dn) **1'b1**
0x520	vesc_reg6[9]	**cb_allanylane_lpback_fix_enable** 1'b0: In Cfg state port checks on loopback bit set on any lane. 1'b1: In Cfg state port checks on loopback bit set on all lane.	**1'b1**
0x520	vesc_reg6[10]	**cb_DstateSM_reset_noDLDown_enable** –Default 1'b0 1'b0: DstateSM reset is on Link Down (DL Down). 1'b1: DstateSM doesn't reset on Link Down (DL Down).	1'b0 (Sim - rand)
0x520	vesc_reg6[11]	**cb_ur_err_msg_status_enable** 1'b0: Error Msg is not sent and error status bit is not set for non-active SWDN ports. 1'b1: Error Msg are sent and error status bit is set for non-active SWDN ports. (This bit is valid only for Up and reserved for Dn/Ep ports)	(Up) 1'b0 (Sim - rand)

Table 42. VESC_REG 6: (Offset 20h): General configuration register

Offset	Bits	Description	Value
0x520	vesc_reg6[12]	**cb_ur_dnport_id_enable** 1'b0: UR CPL because of non-active downstream port have the Completer ID (B:D:F) of the upstream port. 1'b1: UR CPL because of non-active downstream port have the Completer ID (B:D:F) of the downstream port. (This bit is valid only for Up and reserved for Dn/Ep ports)	(Up) **1'b1**
0x520	vesc_reg6[13]	**cb_sig_sys_err_enable** 1'b1: Signal System Error bit (Status Reg Offset 0x06) is set upon ERR_FATAL/NONFATAL Message and SERR# is 1'b1. 1'b1: Signal System Error bit (Status Reg Offset 0x06) is not set upon ERR_FATAL/NONFATAL Message and SERR# is 1'b1. (This bit is valid only for Dn and reserved for Up/Ep ports)	(Dn) 1'b0 **(?)** (Sim - rand)
0x520	vesc_reg6[14]	**cb_mask_adv_err_cor_enable** 1'b0: Advisory Error Correctable status is set upon FATAL error 1'b1: Advisory Error Correctable status is not set upon FATAL error	**1'b1**
0x520	vesc_reg6[15]	**cb_custom_clkreq_disable** 1'b0: Custom CLKREQ is enabled (needed for UP only) 1'b1: Custom CLKREQ is disabled (for Dn/EMEP) (Used only in Host Router Mode)	Up - 1'b0 Dn / EP - **1'b1**
0x520	vesc_reg6[16]	**cb_disable_MsgdestVC_byrouteID** 1'b0: destVC for ID routed Messages is correctly computed (using the ID (B:D:F) information) 1'b1: destVC for ID routed Messages are incorrectly computed in (without using the ID (B:D:F) information)	1'b0
0x520	vesc_reg6[17]	**cb_devnum_fix_disable** 1'b0: Dev Num in the UR CPL's sent by Dn ports is 'correctly set to the Dn ports device number. 1'b1: Dev Num in the UR CPL's sent by Dn ports is 'd0. (This bit is valid only for Dn and reserved for Up/Ep ports)	1'b0

Table 42. VESC_REG 6: (Offset 20h): General configuration register

Offset	Bits	Description	Value
0x520	vesc_reg6[18]	**cb_MRD_Lk_fix_disable** 1'b0: UR CPL's Lock for MrdLk 32/64 are returned 1'b1: UR CPL's for MrdLk 32/64 are not returned	1'b0
0x520	vesc_reg6[20:19]	**cb_room_avail_margin_select** 2'b00 – Margin is 5'd8 2'b 01 – Margin is 5'd12 2'b 10 – Margin is 5'd16 2'b 11 – Not applicable but if programmed Margin is 5'd8	2'b00
0x520	vesc_reg6[22:21]	**cb_min_idle_transmit_count** While in Configuration: 2'b00 – Margin is 4'd2 2'b01 – Margin is 4'd3 2'b10 – Margin is 4'd6 2'b11 – Margin is 4'd7 While in Recovery: 2'b00 – Margin is 4'd4 2'b01 – Margin is 4'd5 2'b10 – Margin is 4'd8 2'b11 – Margin is 4'd9	2'b00 (Sim - rand)
0x520	vesc_reg6[23]	**cb_lane_reversal_disable** 1'b0: Lane reversal exists according to define 1'b1: Lane reversal is disabled (even if defined)	1'b0
0x520	vesc_reg6[24]	**cb_lane_reversal_x2_mode_disable:** Default 1'b0 1'b0: Lane 0 is compared with 1 and Lane 1 with 0. 1'b1: Lane 0 is compared with 3 and Lane 1 with 2.	1'b0
0x520	vesc_reg6[26:25]	**cb_update_fcq_wait_count:** Default 1'b0 1'b0: At gen1 speed wait for 5 cycles. 1'b1: At gen1 speed wait for 4 cycles.	1'b0 (Sim - rand)
0x520	vesc_reg6[27]	**cb_sw_mode_err_cfgwr0_msgd_disab** 1'b0: For poisoned TLP advisory error, CfgWr0 and MsgD are taken into account. 1'b1: For poisoned TLP advisory error, CfgWr0 and MsgD are not taken into account.	1'b0

Table 42. VESC_REG 6: (Offset 20h): General configuration register

Offset	Bits	Description	Value
0x520	vesc_reg6[28]	**EI inferring disable** 1’b0: EI Inferring is enabled 1’b1: EI Inferring is disabled	1’b0
0x520	vesc_reg6[29]	**cb_prog_cons2_sel:** Default 1’b0 1'b0: Counter value in TSXDet is set to 1 1'b1: Counter value in TSXDet is set to 2 (DFT)	1'b0
0x520	vesc_reg6[30]	**cb_goto_quiet_rcvr_notdet:** Default 1’b0 1'b0: Wait 12 ms before going to DETECT.QUIET when Rcvr is not detected on all lanes. 1'b1: Do not wait 12 ms and immediately go to DETECT.QUIET when Rcvr is not detected on all lanes.	**1'b1**
0x520	vesc_reg6[31]	**cb_disable_eidleinfer_skip:** Default 1’b0 1'b0: Inferring EI by skip absence is enabled 1'b1: Inferring EI by skip absence is disabled Can be set only if EI disabled (vesc_reg6[28]) or DLLP inferring is enabled instead (vesc_reg0[23]))	1'b0 (Sim - rand)

Table 43. VESC_REG 7: (Offset 24h): Custom NVM register

Offset	Bits	Description	Value
0x524	vesc_reg7[31:0]	Custom use	32'h0

Table 44. VESC_REG 8: (Offset 28h): DFT register 1 (RO)

Offset	Bits	Description	Value
0x528	vesc_reg8[31:0]	Read Only register that collects several internal Hardware indication for Debug Bit 31 – Data Link is Active Bit 30 – Link Up Other bits changes according to configuration. 4 options controlled by vesc_reg9[31:30]	32'h0

Table 45. VESC_REG 9: (Offset 2Ch): DFT register 2

Offset	Bits	Description	Value
0x52C	vesc_reg9[9:0]	**Recovery cause** Entry to Recovery sticky Bit9 – Received TS Bit8 – Presence change (Unplug) Bit7 – TLP Replay (several times) Bit6 – DLLP Absence Bit5 – Retrain Link (only Dn) Bit4 – Hot Reset (only Dn) Bit3 – Disabled (only Dn) Bit2 – Loopback Bit1 – Rx EI without EIOS Bit0 – Speed Change Note: Bits that can be reset by writing 1	10'h0
0x52C	vesc_reg9[10]	**Recovery to Detect** Indicates transition from Recovery to Detect happened Note: Bits that can be reset by writing 1	1'b0
0x52C	vesc_reg9[11]	**Configuration to Detect** Indicates transition from Configuration to Detect happened Note: Bits that can be reset by writing 1	1'b0
0x52C	vesc_reg9[12]	**Polling to Detect** Indicates transition from Polling to Detect happened Note: Bits that can be reset by writing 1	1'b0
0x52C	vesc_reg9[15:13]	Reserved	1'b0
0x52C	vesc_reg9[19:16]	**LTSSM Sub-State Read Only** Hardware status of Sub-state of LTSSM state (bits 24:21)	

Table 45. VESC_REG 9: (Offset 2Ch): DFT register 2

Offset	Bits	Description	Value
0x52C	vesc_reg9[23:20]	**LTSSM State Read Only** LTSSM state status 4'h0 – Detect 4'h1 – Polling 4'h2 – Configuration 4'h3 – L0 4'h4 – Recovery 4'h5 – Disable 4'h6 – Loopback 4'h7 – Hot Reset 4'h8 – L0sTx 4'h9 – L0sRx 4'hA – L1 4'hB - L2 4'hC – L0sTxRx 4'hD – Transition state in L0s (wait Tx exit) 4'hE – Transition State in L0s (wit Rx exit) 4'hF – Transition state to Recovery	
0x52C	vesc_reg9[27:24]	**cb_select_ln_eq_probe** Control of Equalization signals select for debug	4’h0
0x52C	vesc_reg9[31:28]	**Read Only vesc_reg8 control** Select of different signals for debug to be routed to vesc_reg8	2'b00

Table 46. VESC_REG 10: (Offset 30h): Custom Reg access (Command Register)

Offset	Bits	Description	Value
0x530	vesc_reg10[31:0]	Custom use	32'h0

Table 47. VESC_REG 11: (Offset 34h): Custom Reg access (Write Data Register)

Offset	Bits	Description	Value
0x534	vesc_reg11[31:0]	Custom use	32'h0

Table 48. VESC_REG 12: (Offset 38h): Custom Reg access (Read Data Register)

Offset	Bits	Description	Value
0x538	vesc_reg12[31:0]	Custom use	32'h0

Table 49. VESC_REG 13 (Offset 3Ch): Custom LTR register 1

Offset	Bits	Description	Value
0x53C	vesc_reg13[31:0]	Custom use	32'h0

Table 50. VESC_REG 14 (Offset 40h): Custom LTR register 2

Offset	Bits	Description	Value
0x540	vesc_reg14[31:0]	Custom use	32'h0

Table 51. VESC_REG 15 (Offset 44h): Custom LTR register 3

Offset	Bits	Description	Value
0x544	vesc_reg15[31:0]	Custom use	32'h0

Table 52. VESC_REG 16 (Offset 48h): Custom Vendor Register 1

Offset	Bits	Description	Value
0x548	vesc_reg16[31:0]	Custom use	32'h0

Table 53. VESC_REG 17 (Offset 4Ch): Custom Vendor register 2

Offset	Bits	Description	Value
0x54C	vesc_reg17[31:0]	Custom use	32'h0

Table 54. VESC_REG 18 (Offset 50h): CAB VC0 register

Offset	Bits	Description	Value
0x550	vesc_reg18[0]	**VC0 CAB enable** 1'b0: VC0 CAB is disabled 1'b1: VC0 CAB is enabled (This bits is valid only for Dn port)	(Dn) 1'b0 (CAB – **1'b1**)
0x550	vesc_reg18[1]	**VC0 MemRd Admission Enable** 1'b0: VC0 MemRd Admission is disabled 1'b1: VC0 MemRd Admission is enabled	1'b0 (CAB – **1'b1**)
0x550	vesc_reg18[2]	**Load Threshold value** 1'b0: No effect 1'b1: Load MemRd admission threshold for VC0	1'b0
0x550	vesc_reg18[3]	**VC0 CAB capable** Read Only bit to indicate Downstream Port supports VC0 CAB (This bits is valid only for Dn port)	Up/Ep – 1'b0 Dn – **1'b1**
0x550	vesc_reg18[4]	**rd_cmpl_same_cycle_fix_dis** 1'b0: Port handles the case of Rd and Cmpl at the same cycle. 1'b1: Bug is not fixed	1'b0
0x550	vesc_reg18[5]	**check_cab_calculation_en** 1'b0: Port doesn't check over/underflow of counters 1'b1: Port checks over/underflow of counters	**1'b1**
0x550	vesc_reg18[6]	cb_dont_wr_cab_if_disabled_fix_dis 1'b0: CAB is not written at all if not enabled 1'b1:CAB is written, even if not enabled (Bug)	1'b0
0x550	vesc_reg18[7]	Reserved	1'b0

Table 54. VESC_REG 18 (Offset 50h): CAB VC0 register

Offset	Bits	Description	Value
0x550	vesc_reg18[11:8]	**VC0 CAB Size** Read only field to indicate CAB size in units of 512 Bytes	Up/Ep – 4'h0 Dn - 4'h8
0x550	vesc_reg18[13:12]	Reserved	4'h0
0x550	vesc_reg18[14]	**cb_stop_tx_high_stop_wr_retry** 1'b0: When StopTx is high stop write to Retry Buffer only if available space is high than threshold (vesc_reg34[4:3]) 1'b1: When StopTx is high stop write to Retry Buffer	1'b0
0x550	vesc_reg18[15]	**cb_stop_tx_low_count_sel** Select time StopTx considered still high after de-assertion 1'h0: Wait 32 cycles after TxStop is low 1'h1: Wait 16 cycles after TxStop is low	1'b0
0x550	vesc_reg18[31:16]	**VC0 Threshold** Threshold value in dwords (32 bits) for VC0	16'h0

Table 55. VESC_REG 19 (Offset 54h): CAB VC1 register

Offset	Bits	Description	Value
0x554	vesc_reg19[0]	**VC1 CAB enable** 1'b0: VC1 CAB is disabled 1'b1: VC1 CAB is enabled (This bits is valid only for Dn port)	(Dn) 1'b0/**1'b1**
0x554	vesc_reg19[1]	**VC1 MemRd Admission Enable** 1'b0: VC1 MemRd Admission is disabled 1'b1: VC1 MemRd Admission is enabled	1'b0/**1'b1**
0x554	vesc_reg19[2]	**Load Threshold value** 1'b0: No effect 1'b1: Load MemRd admission threshold for VC1	1'b0/**1'b1**
0x554	vesc_reg19[3]	**VC1 CAB capable** Read Only bit to indicate Downstream Port supports VC1 CAB (This bits is valid only for Dn port)	Up/Ep – 1'b0 Dn – **1'b1**
0x554	vesc_reg19[4]	**rd_cmpl_same_cycle_fix_dis** 1'b0: Port handles the case of Rd and Cmpl at the same cycle. 1'b1: Bug is not fixed	1'b0

Table 55. VESC_REG 19 (Offset 54h): CAB VC1 register

Offset	Bits	Description	Value
0x554	vesc_reg19[5]	**check_cab_calculation_en** 1'b0: Port doesn't check over/underflow of counters 1'b1: Port checks over/underflow of counters	**1'b1**
0x554	vesc_reg19[6]	cb_dont_wr_cab_if_disabled_fix_dis 1'b0: CAB is not written at all if not enabled 1'b1:CAB is written, even if not enabled (Bug)	1'b0
0x554	vesc_reg19[7]	Reserved	2'b0
0x554	vesc_reg19[12:8]	**VC1 CAB Size** Read only field to indicate CAB size in units of 512 Bytes	Up/Ep – 4'h0 Dn - 4'h8
0x554	vesc_reg19[15:12]	Reserved	4'h0
0x554	vesc_reg19[31:16]	**VC1 Threshold** Threshold value in dwords (32 bits) for VC1	16'h0

Table 56. VESC_REG 20 (Offset 'h58): CAB reserved register

Offset	Bits	Description	Value
0x558	vesc_reg20[0]	Reserved	32'h0

Table 57. VESC_REG 21 (Offset 'h5C) -- QoS - Load priority & Custom mode register

Offset	Bits	Description	Value
0x55C	vesc_reg21[7:0]	**Priority value VC arbiter** (per transaction type) Used in per transaction type (Post / Non-Post / Cmpl) VC arbiter (Loaded when bit 16 is set)	8’d0
0x55C	vesc_reg21[15:8]	**Priority value VC arbitration** (over all transaction types) Used in in VC arbiter over all transaction types (Loaded when bit 17 is set)	8’d0
0x55C	vesc_reg21[16]	**Load priority value VC arbiter** (per transaction type) 1'b0: No effect 1'b1: Loads Priority value VC arbiter per transaction type.	1’b0
0x55C	vesc_reg21[17]	**Strict priority VC arbiter** (per transaction type) 1'b0: No effect 1'b1: Strict Priority in VC arbiter per transaction type (DFT)	1’b0
0x55C	vesc_reg21[18]	**Load priority value VC arbiter** (over all type of transactions) 1'b0: No effect 1'b1: Loads Priority value VC arbiter over all transaction type.	1’b0

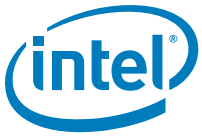


Table 57. VESC_REG 21 (Offset 'h5C) -- QoS - Load priority & Custom mode register

Offset	Bits	Description	Value
0x55C	vesc_reg21[19]	**Strict priority VC arbiter** (over all type of transactions) 1'b0: No effect 1'b1: Strict Priority in VC arbiter over all transaction type (DFT)	1’b0
0x55C	vesc_reg21[20]	**cb_disable_priority_arb** 1'b0: Arbitration is active over transaction types 1'b1: Disable priority arbitration over transaction types	1’b0
0x55C	vesc_reg21[21]	**cb_disable_lookahead_buffer** 1'b0: Look ahead to Rx buffers to keep the VC request channel for VC Arbiter. 1'b1: Disable looking ahead to buffer (Bug)	1’b0
0x55C	vesc_reg21[22]	**cb_tx_tc_remap_on_all_links_en** 1'b0: Tx TC remapping is allowed on custom VC0 link 1'b1: Tx TC remapping is allowed on any link	1'h0
0x55C	vesc_reg21[23]	**cb_rx_tc_remap_on_all_links_en** 1'b0: Rx TC remapping is allowed on custom VC0 link 1'b1: Rx TC remapping is allowed on any link	1'h0
0x55C	vesc_reg21[24]	**Custom VC mode enable** 1'b0: No Effect 1'b1: Custom VC mode	1’b0
0x55C	vesc_reg21[25]	**VC0 link only enable** 1'b0: No Effect 1'b1: VC0 only link (set together with bit 24)	1’b0
0x55C	vesc_reg21[26]	**Map according to Source TC/VC map** 1'b0: Send packet according to TC/VC map of destination. 1'b1: Send packet according to TC/VC map of source.	1’b0
0x55C	vesc_reg21[27]	Enable VC0 CPL push VC0 and VC1 Posted. 1'b0: No Effect 1'b1: Completion on VC0 push Posted on VC0 and VC1	1’b0
0x55C	vesc_reg21[28]	Enable VC1 CPL push VC0 and VC1 Posted 1'b0: No Effect 1'b1: Completion on VC1 push Posted on VC0 and VC1	1’b0
0x55C	vesc_reg21[29]	**cb_qos_custom_spec_rx_sel**	
0x55C	vesc_reg21[30]	**cb_qos_custom_spec_tx_sel**	
0x55C	vesc_reg21[31]	**cb_txvc_mapping_shadow_disable**	0

Table 58. VESC_REG 22 (Offset 'h60) -- Shadow port VC Capability and VC Resource Control register

Offset	Bits	Description	Value
0x560	vesc_reg22[2:0]	**Extended VC Count** Extended VC count to be loaded with value 1	3'h0
0x560	vesc_reg22[3]	Reserved	1'b0
0x560	vesc_reg22[6:4]	**Low Priority Extended VC Count** Low Priority Extended VC count to be loaded with value 1	3'h0
0x560	vesc_reg22[15:7]	Reserved	9'h0
0x560	vesc_reg22[23:16]	**TC/VC1 Map** Field to be lowed with TC mapping for VC1	8'h0
0x560	vesc_reg22[26:24]	**VC1 ID** VC ID to be loaded with value 1	3'h0
0x560	vesc_reg22[30:27]	Reserved	4'h0
0x560	vesc_reg22[31]	**VC1 enable** 1'b0: No 1'b1: Custom VC1 is enabled	1'b0

Table 59. VESC_REG 23 (Offset 'h64) -- TX and Rx TC remapping register

Offset	Bits	Description	Value
0x564	vesc_reg23[0]	**Remap TC Tx Post** Map all Tx Posted traffic to TC0	1'b0
0x564	vesc_reg23[1]	**Remap TC Tx Non-Post** Map all Tx NonPosted traffic to TC0	1'b0
0x564	vesc_reg23[2]	**Remap TC Tx Cmpl** Map all Tx CPL traffic to TC0	1'b0
0x564	vesc_reg23[3]	**Remap TC Tx Msg** Map all Tx Msg traffic to TC0	1'b0
0x564	vesc_reg23[4]	**Remap one TC Tx Post** Map Tx Posted with TC == vesc_reg23 [10:8] to TC0	1'b0
0x564	vesc_reg23[5]	**Remap one TC Tx Non-Post** Map Tx NonPosted with TC == vesc_reg23 [10:8] to TC0	1'b0
0x564	vesc_reg23[6]	**Remap one TC Tx Cmpl** Map Tx CPL with TC == vesc_reg23 [10:8] to TC0	1'b0
0x564	vesc_reg23[7]	**Remap one TC Tx Msg** Map Tx Msg with TC == vesc_reg23 [10:8] to TC0	1'b0
0x564	vesc_reg23[10:8]	**TC for Tx Remap** TC value with which the TLP TC is to be matched for remapping.	3'h0
0x564	vesc_reg23[14:11]	Reserved	0
0x564	vesc_reg23[15]	TBD	1'b0
0x564	vesc_reg23[16]	**Remap TC Rx Post** Map Rx Posted to TC 22:20	1'b0

Table 59. VESC_REG 23 (Offset 'h64) -- TX and Rx TC remapping register

Offset	Bits	Description	Value
0x564	vesc_reg23[17]	**Remap TC Rx Non-Post** Map Rx NonPosted to TC 22:20	1'b0
0x564	vesc_reg23[18]	**Remap TC Rx Cmpl** Map Rx CPL to TC 22:20	1'b0
0x564	vesc_reg23[19]	**Remap TC Rx Msg** Map Rx Msg to TC 22:20	1'b0
0x564	vesc_reg23[22:20]	**TC RX Remap** Remap to this TC incoming traffic	3'h0
0x564	vesc_reg23[23]	**Remap TC Rx Non-Match Post** Map Rx Posted when it does not have a match in the bdf table entry to TC 29:27	1'b0
0x564	vesc_reg23[24]	**Remap TC Rx Non-Match Non-Post** Map Rx NonPosted when it does not have a match in the bdf table entry to TC 29:27	1'b0
0x564	vesc_reg23[25]	**Remap TC Rx Non-Match Cmpl** Map Rx CPL when it does not have a match in the bdf table entry to TC 29:27	1'b0
0x564	vesc_reg23[26]	**Remap TC Rx Non-Match Msg** Map Rx Msg when it does not have a match in the bdf table entry to TC 29:27	1'b0
0x564	vesc_reg23[29:27]	**Non-Match TC Rx Remap** Remap is to this TC when Non Match to bdf entry.	3'h0
0x564	vesc_reg23[30]	Reserved	1'b0
0x564	vesc_reg23[31]	**Upstream Traffic RX TC remapping** 1'b0: RX TC remapping is done for all RX traffic 1'b1: RX TC remapping is done only for Traffic whose destination is Upstream (This bit valid for Dn and reserved forUp/Dn)	1'b0

Table 60. VESC_REG 24-31 (Offset 'h68 - 'h84) -- Rx remapping BDF (Bus:Device: Function) tables (vesc_reg24 to vesc_reg31 have the same structure)

Offset	Bits	Description	Value
0x5*	vesc_reg*[0]	**Post Rx TC Map** Map Rx Posted (MemWr) to TC 6:4 if bdf [31:16] matches	1'b0
0x5*	vesc_reg*[1]	**NonPost Rx TC Map** Map Rx NonPosted to TC 6:4 if bdf [31:16] matches	1'b0
0x5*	vesc_reg*[2]	**Cmpl Rx TC Map** Map Rx CPL to TC 6:4 if bdf [31:16] matches	1'b0
0x5*	vesc_reg*[3]	**Msg Rx TC Map** Map Rx Msg to TC 6:4 if bdf [31:16] matches	1'b0

Table 60. VESC_REG 24-31 (Offset 'h68 - 'h84) -- Rx remapping BDF (Bus:Device: Function) tables (vesc_reg24 to vesc_reg31 have the same structure)

Offset	Bits	Description	Value
0x5*	vesc_reg*[6:4]	**Remap to this TC** Remapping will be done to TC specified in this field (0 to 7)	3'h0
0x5*	vesc_reg*[7]	**Ignore Function Number** Wild Card option to include all functions under same line	1'b0
0x5*	vesc_reg*[15:8]	Reserved	8'h0
0x5*	vesc_reg*[31:16]	**BDF** Bus : 8 bits [31:24] Device : 5 bits [23:19] Function : 3 bits [18:16]	16'h0

Table 61. VESC_REG 32 (Offset 'h88): Custom Port Arbitration registers 1

Offset	Bits	Description	Value
0x588	vesc_reg32[31:0]	TBD	32'h0

Table 62. VESC_REG 33 (Offset 'h8C): Custom Port Arbitration registers 2

Offset	Bits	Description	Value
0x58C	vesc_reg33[31:0]	TBD	32'h0

Table 63. VESC_REG 34: (Offset 90h): General configuration register

Offset	Bits	Description	Value
0x590	vesc_reg34[1:0]	**cb_eidle_to_eidleset_upbnd_sel** Time to wait from Rx EI to EIOS 2'b00: Upper bound for idle to idleset == 7'd40 2'b01: Upper bound for idle to idleset == 7'd20 2'b10: Upper bound for idle to idleset == 7'd60 2'b11: Upper bound for idle to idleset == 7'd80	2'b0
0x590	vesc_reg34[2]	**cb_mask_txdata_vld_disable**– Default 1'b0 1'b0: Mask TxDataValid and TxStartBlock during Tx EI 1'b1: Do not mask TxDataValid and TxStartBlock during Tx EI	1'b0
0x590	vesc_reg34[4:3]	**cb_ctrl_retry_buf_thrshold** (QoS) Considering Retry Buffer available room at Tx channel 2'b00: Current behavior No blocking of VC0 packets. 2'b01: Block if Retry Buffer is 3/4 full 2'b10: Block if Retry Buffer half full 2'b11: Block if Retry Buffer is 1/4 full	(Dn Port) 2b00 2'h01 (Sim - direct)

Table 63. VESC_REG 34: (Offset 90h): General configuration register

Offset	Bits	Description	Value
0x590	vesc_reg34[5]	**cb_pipedemux_strobe_reset_dis** 1'b0: Reset of PipeDemux address count strobe at De-Skew. 1'b1: Disable reset of PipeDemux address count strobe. (This count strobe is used in Gen1/2)	1'b0 (Sim - rand)
0x590	vesc_reg34[6]	**cb_gen3_block_dllp** 1'b0: For Dn port doesn't block Init FC DLLP till Equalization completes. For Up/Ep port block Init FC DLLP till good DLLP Pkt is received 1: For Dn ports (when Upcomp = 1) block Init FC DLLP till Equalization completes. For Up/Ep port doesn't block Init FC DLLP till good DLLP Pkt is received	1'b0
0x590	vesc_reg34[7]	**cb_recov_speed_to_detect** 1'b0: Recovery.Speed to Detect timeout after 48 ms. 1'b1: No Timeout from Recovery.Speed to Detect (Bug)	1'b0
0x590	vesc_reg34[12:8]	**cb_down_port_DevNum** (for custom use) Device number that will be used for DownStream Ports (instead of default) if bit 13 is set. (This field is valid for Dn port and reserved for Up/Ep ports)	(Dn) 5'b0 (Sim - direct)
0x590	vesc_reg34[13]	**cb_use_down_port_DevNum** 1'b0: No effect 1'b1: Use the **cb_down_port_DevNum** as the device number for Downstream Port. (This bit is valid for Dn port and reserved for Up/Ep ports)	(Dn) 1'b0 (Sim - direct)
0x590	vesc_reg34[14]	**cb_disable_tlp_formater** 1'b0: Use new TLP formatter (TLP's are always written to retry buffer in gen3 format and read according to data rate). 1'b1: Do not use TLP formatter. TLP's are always written to retry buffer in format of the current data rate.	1'b0

Table 63. VESC_REG 34: (Offset 90h): General configuration register

Offset	Bits	Description	Value
0x590	vesc_reg34[15]	**cb_disable_anylane_eios** 1'b0: Detected EIOS on any lane 1'b1: Detected EIOS on all lanes	1'b0 (Sim - rand)
0x590	vesc_reg34[16]	**cb_disable_extra_skip** 1'b0: Fix issue of sending Skip from SkipReq during L0 (PHY) 1'b1: SkipReq in PhyLayer tries to sends Skip during L0 (bug)	1'b0
0x590	vesc_reg34[18:17]	**cb_en_wteios_config_L1[1:0]** X0: Do not wait for eios before entering L1 01: Wait for eios before entering L1 11: Wait for eios for configurable time before entering L1 (These bits are inverted for Up/EP)	2'b00
0x590	vesc_reg34[19]	**cb_en_wteios_config_L1[2]** 1'b0: Wait 2xTTX-IDLE-MIN for eios before entering L1 1'b1: Wait 4xTTX-IDLE-MIN for eios before entering L1	**1'b1**
0x590	vesc_reg34[20]	**cb_en_wteios_config_L2[0]** 1'b0: Do not wait for eios before entering L2 1'b1: Wait for eios before entering L2 (These bit is inverted for Up/EP)	1'b0
0x590	vesc_reg34[21]	**cb_en_wteios_config_L2[1]** 0: Default timer to wait for EIOS on the receive side. 1: Enlarge the wait EIOS timer.	**1'b1**
0x590	vesc_reg34[22]	**cb_ bypass_equalization** 1'b0: Do not bypass gen3 equalization 1'b1: Completely Bypass gen3 equalization (DFT - Simulation)	1'b0
0x590	vesc_reg34[23]	**cb_lane_nonpad_check_dis** 1'b0: Port checks the lane number 1'b1: port just check the lane is non PAD	**1'b1**
0x590	vesc_reg34[24]	**cb_link_nonpad_check_dis** 1'b0: Port checks the link number 1'b1: port just check the link is non PAD	**1'b1**

Table 63. VESC_REG 34: (Offset 90h): General configuration register

Offset	Bits	Description	Value
0x590	vesc_reg34[25]	**cb_bypass_rx_detect** 1'b0: Do not Bypass Rx Detection in DETECT.QUIET_PRE state 1'b1: Bypass Rx Detection in DETECT.QUIET_PRE state (DFT)	1'b0
0x590	vesc_reg34[26]	**cb_bypass_scram_descram** 1'b0: Do not Bypass Scrambler/DeScrambler. 1'b1: Bypass Scrambler/DeScrambler (DFT**)**	1'b0
0x590	vesc_reg34[27]	**cb_TXStoreForward_enable** 1'b0: Core operates in cut-thru mode (Retry Buffer) 1'b1: Core operates in Store forward mode	1'b0 (Sim - rand)
0x590	vesc_reg34[28]	**cb_ByPassCreditChk** 1'b0: Do not by pass credit check 1'b1: Bypass credit check (DFT)	1'b0
0x590	vesc_reg34[29]	**cb_CoreHasInfCredits** 1'b0: Core has finite credits 1'b1: Core has infinite credits (DFT)	1'b0
0x590	vesc_reg34[30]	**cb_LBMode_one** 1'b0: No loopback 1'b1: Tx looped back to Rx within the port (DFT)	1'b0
0x590	vesc_reg34[31]	**cb_ForceToCompliance** 1'b0: Port is not forced to compliance 1'b1: Port is forced to compliance (DFT)	1'b0

Table 64. VESC_REG 35 (Offset 'h94): General configuration register

Offset	Bits	Description	Value
0x594	vesc_reg35[0]	**cb_exit_l1_trigger_soft_sel** 1'b0: Exit L1 from Mux is used for L1 Soft 1'b1: Exit L1 from Mux is not used for L1 Soft	1’b0
0x594	vesc_reg35[1]	**cb_exit_l1_trigger_aspm_sel** 1'b0: Exit L1 from Mux is used for L1 ASPM 1'b1: Exit L1 from Mux is not used for L1 ASPM	1’b0
0x594	vesc_reg35[31:0]	Custom use	32'h0

Table 65. VESC_REG 36 (Offset 'h98): DFT Read Only registers (Gen3, Port, L1Sub)

Offset	Bits	Description	Value
0x598	vesc_reg36[27:0]	Read Only indications	28'h0
0x598	vesc_reg36[31:28]	Debug Mux selector	4'h0

Table 66. VESC_REG 37 (Offset 'h9C): DFT Sticky registers to capture different events

Offset	Bits	Description	Value
0x59C	vesc_reg37[31:0]	TBD	32'h0

Table 67. VESC_REG 38 (Offset 'hA0): Custom L2 feature register

Offset	Bits	Description	Value
0x5A0	vesc_reg38[31:0]	TBD	32'h0

Table 68. VESC_REG 39 (Offset 'hA4): Custom Compliance Pattern register 1

Offset	Bits	Description	Value
0x5A4	vesc_reg39[3:0]	**K-char value** Used to force K-Char in Gen1/2 Pattern along with register 40	4'h0
0x5A4	vesc_reg39[9:4]	**FSM state** Used with bit 30 or bit 29 to force required state Values are from 6'd0 to 6'd34	6'b0
0x5A4	vesc_reg39[10]	**Disable Load Board Compliance Entry** 1'b0: No effect 1'b1: Prevents from Port to enter Polling.Compliance due to Rx Electrical Idle signal being high	1'b0
0x5A4	vesc_reg39[11]	Reserved	1'b0
0x5A4	vesc_reg39[12]	**LFSR advance disable output** Don’t Advance LFSR output value (valid if bit 26 is set)	1'b0
0x5A4	vesc_reg39[13]	**Scrambler reset output** Reset Scrambler output value (valid if bit 26 is set)	
0x5A4	vesc_reg39[14]	**Drive Compliance output** Drive Compliance output value (valid if bit 26 is set)	1'b0
0x5A4	vesc_reg39[15]	**Exit Compliance output** Exit Compliance output value (valid if bit 26 is set)	1'b0
0x5A4	vesc_reg39[16]	**Rx EI input** Rx Electrical Idle input value (valid if bit 27)	1'b0
0x5A4	vesc_reg39[17]	**Compliance entry method input** Compliance entry method (valid if bit 27 and 25 are set)	1'b0
0x5A4	vesc_reg39[18]	**Send Compliance input** Send Compliance input value (valid if bit 27 is set)	1'b0
0x5A4	vesc_reg39[19]	**Modified Compliance input** Modified Compliance input value (valid if bit 27 is set)	1'b0
0x5A4	vesc_reg39[20]	**Custom value lane 0 enable** 1'b0: No effect 1'b1: Enable to force the custom pattern on lane 0	1'b0

Table 68. VESC_REG 39 (Offset 'hA4): Custom Compliance Pattern register 1

Offset	Bits	Description	Value
0x5A4	vesc_reg39[21]	**Custom value lane 1 enable** 1'b0: No effect 1'b1: Enable to force the custom pattern on lane 1	1'b0
0x5A4	vesc_reg39[22]	**Custom value lane 2 enable** 1'b0: No effect 1'b1: Enable to force the custom pattern on lane 2	1'b0
0x5A4	vesc_reg39[23]	**Custom value lane 3 enable** 1'b0: No effect 1'b1: Enable to force the custom pattern on lane 3	1'b0
0x5A4	vesc_reg39[24]	**Compliance Entry Method enable** 1'b0: No effect 1'b1: Enables to force Compliance Entry Method	1'b0
0x5A4	vesc_reg39[25]	**Overwrite FSM outputs from FSM** 1'b0: No effect 1'b1: Enables to force several control outputs of FSM	1'b0
0x5A4	vesc_reg39[26]	**Overwrite FSM Inputs to FSM** 1'b0: No effect 1'b1: Enables to force several control inputs of FSM	1'b0
0x5A4	vesc_reg39[27]	**Jump to Gen3 specific sate enable** 1'b0: No effect 1'b1: Enables to jump states in order to repeat 4 consecutive states for full Gen3 block (bits 9:4)	1'b0
0x5A4	vesc_reg39[28]	**Stop Compliance FSM at specific sate enable** 1'b0: No effect 1'b1: Indicates to stop at specific state of FSM (bits 9:4)	1'b0
0x5A4	vesc_reg39[29]	**Force Compliance FSM specific state enable** 1'b0: No effect 1'b1: Forces specific state of FSM (bits 9:4)	1'b0
0x5A4	vesc_reg39[30]	**Custom Pattern from Register Enable** 1'b0: No effect 1'b1: Enables to force custom pattern from register instead of regular compliance pattern.	1'b0

Table 68. VESC_REG 39 (Offset 'hA4): Custom Compliance Pattern register 1

Offset	Bits	Description	Value
0x5A4	vesc_reg39[31]	**Custom Compliance Enable** 1'b0: No effect 1'b1: Master Bit that enables to use other bits and register 40 to force custom pattern or perform several manipulation to Compliance FSM.	1'b0

Table 69. VESC_REG 40 (Offset 'hA8): Custom Compliance Pattern register 2

Offset	Bits	Description	Value
0x5A8	vesc_reg40[31:0]	**Data from Register** Constant 4 symbols that will be forced on PIPE for custom Compliance Pattern (when bits 31 and 30 are set)	32'h0

Table 70. VESC_REG 41: (Offset ACh): General configuration register

Offset	Bits	Description	Value
0x5AC	vesc_reg41[0]	**cb_gen3_valid_flag_sel** 1'b0: RxDataValid de-assertion is per lane 1'b1: RxDataValid de-assertion is common	1'b0
0x5AC	vesc_reg41[1]	**cb_detetect_rxei_exit_by_eieos_gen2_dis** 1'b0: Rx EI exit in Gen2 by EIEOS 1'b1: Rx EI exit in Gen2 by Rx EI signal	1'b0 (Sim - rand)
0x5AC	vesc_reg41[2]	**cb_detetect_rxei_exit_by_eieos_gen3_dis** 1'b0: Rx EI exit in Gen3 by EIEOS 1'b1: Rx EI exit in Gen3 by Rx EI signal	1'b0 (Sim - rand)
0x5AC	vesc_reg41[3]	**cb_any_lane_rx_ei_exit_det_sel** 1'b0: no effect 1'b1: Any Lane RxEI is done by EIEOS and by Rx EI signal	**1'b1**
0x5AC	vesc_reg41[4]	**cb_all_lane_rx_ei_exit_det_sel** 1'b0: no effect 1'b1: All Lane RxEI is done by EIEOS and by Rx EI signal	**1'b1**
0x5AC	vesc_reg41[5]	**cb_disable_frmerr_data_sds** 1'b0: When recovering from framing error receiver stops processing data until SDS is received 1'b1: When recovering from framing error receiver does not stop processing data until SDS is received	**1'b1** **(TBD)**
0x5AC	vesc_reg41[6]	**cb_rxvalid_deassert_disable** 1'b0: No effect 1'b1: RxValid de-assertion of PIPDemux is delayed for 1 cycle	1'b0

Table 70. VESC_REG 41: (Offset ACh): General configuration register

Offset	Bits	Description	Value
0x5AC	vesc_reg41[7]	**cb_gen2_eieos_detect_cut_dis** 1'b0: Detects Gen2 EIEOS even without first two Bytes 1'b1: Detects Gen2 EIEOS only if first two Bytes exist	1'b0
0x5AC	vesc_reg41[8]	**cb_gen2_eieos_detect_shift_dis** 1'b0: Detects Gen2 EIEOS even if shifted by 2 Bytes. 1'b1: Detects Gen2 EIEOS only if it is aligned correctly.	1'b0
0x5AC	vesc_reg41[9]	**cb_easy_gen2_eieos_detection** 1'b0: no effect 1'b1: Enables to Detects Gen2 EIEOS without last 8 bytes.	**1'b1**
0x5AC	vesc_reg41[10]	**cb_easy_gen3_eieos_detection** 1'b0: no effect 1'b1: Enables to Detects Gen3 EIEOS without last 4 bytes.	1'b0
0x5AC	vesc_reg41[11]	**cb_rst_eieos_flag_in_recov_speed_dis** 1'b0: EIEOS flag is reset during entry to Recovery.Speed 1'b1 :Fix of EIEOS flag reset is disabled	1'b0
0x5AC	vesc_reg41[12]	**cb_no_first_chanbond_dis** 1'b0: First Channel Bonding pulse is disabled (pulse is masked in order not to ruin first EIEOS) 1'b1: First Channel Bonding pulse is enabled	1'b0 (Sim - rand)
0x5AC	vesc_reg41[13]	**cb_gen2_eios_detect_2nd_byte_dis** 1'b0: Gen2 EIOS is detected by only first 3 bytes (Spec) 1'b1: Gen2 EIOS is detected by only first 2 bytes	**1'b1** (Sim - rand)
0x5AC	vesc_reg41[14]	**cb_gen2_eios_detect_3rd_byte_en** 1'b0: Gen2 EIOS is detected without last byte (Spec) 1'b1: Gen2 EIOS is detected by all 4 bytes	1'b0 (Sim - rand)
0x5AC	vesc_reg41[15]	**cb_ignore_rx_data_in_ei_en** (not used)	1'b0
0x5AC	vesc_reg41[16]	**cb_clr_dat_strm_valid_with_rx_ei** 1'b0: no effect 1'b1: Enable to clear Data Stream Valid in Rx EI	**1'b1**
0x5AC	vesc_reg41[17]	**cb_lnrev_rx_ei_early** 1'b0: no effect 1'b1: Selects Rx EI one cycle earlier	1'b0
0x5AC	vesc_reg41[18]	**cb_blk_align_deassertion_dis** 1'b0: Block Align is 1 when Data Stream is no valid 1'b1: Force Block Align control signal high	1'b0

Table 70. VESC_REG 41: (Offset ACh): General configuration register

Offset	Bits	Description	Value
0x5AC	vesc_reg41[19]	**cb_adv_less_nph_credits** 1’b0 : No Action 1’b1 : Advertise less Non-Post Header credits	1'b0
0x5AC	vesc_reg41[22:20]	**cb_adv_less_nph_value** 1’b0 : No effect 1’b1 : Less credits in steps of 4 (0 - 4, 1- 8, … 7 - 28)	3'b0
0x5AC	vesc_reg41[23]	**cb_adv_less_ph_credits** 1’b0 : No Action 1’b1 : Advertise one credit less for Post Header	1'b0
0x5AC	vesc_reg41[24]	**cb_adv_less_pd_credits** 1’b0 : No Action 1’b1 : Advertise 1 credits less for Post Data	1'b0
0x5AC	vesc_reg41[25]	**cb_adv_less_cplh_credits** 1’b0 : No Action 1’b1 : Advertise one credit less for Cmpl Header	1'b0
0x5AC	vesc_reg41[26]	**cb_adv_less_cpld_credits** 1’b0 : No Action 1’b1 : Advertise 1 credit less for Cmpl Data	1'b0
0x5AC	vesc_reg41[27]	**cb_dllp_seq_burst_dis** 1’b0 : Back to Back DLLP can be sent 1’b1 : Disables the option to send back to back DLLP	1'b0
0x5AC	vesc_reg41[28]	**cb_dlssm_arb_fast_ack_grant_dis** 1’b0 : Early Grant ACK for BW improvement 1’b1 : Early Grant ACK is disabled	1'b0
0x5AC	vesc_reg41[29]	**cb_dlssm_arb_fast_fc_grant_dis** 1’b0 : Early Grant FC for BW improvement 1’b1 : Early Grant FC is disabled	1'b0
0x5AC	vesc_reg41[30]	**cb_dlssm_arb_fast_tlp_grant_dis** 1’b0 : Early Grant TLP for BW improvement 1’b1 : Early Grant TLP is disabled	1'b0
0x5AC	vesc_reg41[31]	**cb_reduce_tlp_ipg_fix** 1’b0 : Fix to reduce TLP IPG and improve performance 1’b1 : Fix is disabled	1'b0

Table 71. VESC_REG 42: (Offset B0h): General configuration register

Offset	Bits	Description	Value
0x5B0	vesc_reg42[0]	**cb_det_pwr_down_delay_en** 1'b0 : no effect 1'b1 : delay Power Down in Detect, relatively to Tx EI	1'b0 (Sim - rand)
0x5B0	vesc_reg42[1]	**cb_dis_pwr_down_delay_en** 1'b0: no effect 1'b1: Delay Power Down in Disabled, relatively to Tx EI	1'b0 (Sim - rand)
0x5B0	vesc_reg42[2]	**cb_combine_phy_status_static** 1'b0: no effect 1'b1: PhyStatus de-assertion combined according to xmode	1'b0
0x5B0	vesc_reg42[4:3]	**cb_sel_time_from_rst_to_rx_detect** Select timer value after Reset till Rx Detection 2'b00 : 1ms 2'b01 : 5ms 2'b10 : 13ms 2'b11 : 15ms	**2'b01**
0x5B0	vesc_reg42[6:5]	**cb_sel_time_in_detect_quite** Select timer value in Detect Quite 2'b00 : 13ms 2'b01 : 11ms 2'b10 : 12ms 2'b11 : 14ms	2'b00
0x5B0	vesc_reg42[7]	**cb_disable_snd_eios** 1'b0 : Port sends EIOS before asserting Tx EI while reducing xmode to x1 in Configuration.LaneNumAccept 1'b1 : Port doesn't send EIOS before asserting Tx EI while reducing xmode to x1 in Configuration.LaneNumAccept	1'b0 (Sim - rand)
0x5B0	vesc_reg42[8]	**cb_eidle_inferred_recov_disable** 1'b0 **:** Infer EI is checked in Recovery.Speed entry 1'b1 : Infer EI isn't checked in Recovery.Speed entry	1'b0
0x5B0	vesc_reg42[9]	**cb_idle_before_sds_fix_dis** 1'b0 – Fix to prolong last TS to prevent Logical Idle before Transmission of SDS 1'b1 – Disable the fix of Logical Idle before SDS	1'b0

Table 71. VESC_REG 42: (Offset B0h): General configuration register

Offset	Bits	Description	Value
0x5B0	vesc_reg42[10]	**cb_l0stx_fsm_rst_in_recov_dis** 1'b0 – Entry to Recovery Reset L0sTx FSM 1'b1 – Disable the L0sTx FSM reset	1'b0
0x5B0	vesc_reg42[11]	**cb_l1aspm_fsm_rst_in_recov_dis** 1'b0 – Entry to Recovery Reset L1 ASPM FSM 1'b1 – Disable the L1 ASPM FSM reset	1'b0
0x5B0	vesc_reg42[12]	**cb_l1soft_fsm_rst_in_recov_dis** 1'b0 – Entry to Recovery Reset L1 Soft FSM 1'b1 – Disable the L1 Soft FSM reset	1'b0
0x5B0	vesc_reg42[13]	**cb_backdoor_d0_l1_exit_dis** 1'b0 – Exit L1Soft when Port exits non D0 state (Host i/f) 1'b1 – Exit from non D0 state (Host i/f) doesn't effect L1	1'b0
0x5B0	vesc_reg42[14]	**cb_ei_time_during_rate_change_sel** Selects the time to be in Tx EI 1'b0 – 8us 1'b1 – 60us	**1'b1** (Sim – rand)
0x5B0	vesc_reg42[15]	**cb_exit_elec_idle_for_l0s_idle_sel** 1'b0 – L0sRx exit upon any lane exit from Rx EI 1'b1 – L0sRx exit upon all lane exit from Rx EI	1'b0 (Sim - rand)
0x5B0	vesc_reg42[16]	**cb_exit_elec_idle_for_l1_idle_sel** 1'b0 – L1 exit upon any lane exit from Rx EI 1'b1 – L1 exit upon all lane exit from Rx EI	1'b0 (Sim - rand)
0x5B0	vesc_reg42[17]	**cb_send_one_eios_in_poll_comp** 1'b0: No Effect 1'b1: In cases of 2 EIOS disables the second EIOS	1'b0
0x5B0	vesc_reg42[18]	**cb_bond_rx_valid_fix_dis** 1'b0 – RxDataValid is delayed with same delay of Rx Data. 1'b1 – RxDataValid delay is not fixed.	1'b0
0x5B0	vesc_reg42[20:19]	**cb_l0s_entry_time_sel** Select the time to wait during L0s entry (in PCLK div2) 2'b00 – 120 cycles 2'b01 – 90 cycles 2'b10 – 60 cycles 2'b11 – 30 cycles	2'b00 (Sim - rand)

Table 71. VESC_REG 42: (Offset B0h): General configuration register

Offset	Bits	Description	Value
0x5B0	vesc_reg42[21]	**cb_lcrc_gap_fix_dis** 1'b0**:** Fix the issue of LCRC calculation when TxDataValid is throttled. 1'b1: Issue of LCRC calculation when TxDataValid is throttled is not fixed.	1'b0
0x5B0	vesc_reg42[22]	**cb_fast_grant_ext_dis** 1'b0 : Grant for external channels is returned immediately 1'b1 : Grant for external channels is delayed for one cycle	1'b0
0x5B0	vesc_reg42[23]	**cb_fast_grant_int_en** 1'b0 : Grant for internal channels is delayed for one cycle 1'b1 : Grant for internal channels is returned immediately	1'b0
0x5B0	vesc_reg42[24]	**cb_early_vc_sel_forreq_ext_dis** 1'b0 : VC select for external channels comes earlier 1'b1 : VC select for external channels comes later	1'b0
0x5B0	vesc_reg42[25]	**cb_early_vc_sel_forreq_int_dis** 1'b0 : VC select for internal channels comes earlier 1'b1 : VC select for internal channels comes later	1'b0
0x5B0	vesc_reg42[26]	**cb_return_ur_in_non_d0_state_en** 1'b0 : no effect 1'b1 : When Port in non D0 UR is returned upon MemRd	**1'b1**
0x5B0	vesc_reg42[27]	**cb_vdm_type1_fc_sel** 1'b0 : Port doesn't returns FC on VDM type 1 (from User) 1'b1 : Port returns FC on VDM type 1	Up/Dn – 1'b0 EMEP - **1'b1**
0x5B0	vesc_reg42[28]	**cb_vdm_type0_fc_sel** -(in EMEP) 1'b0 : Port doesn't returns FC on VDM type 0 (from User) 1'b1 : Port returns FC on VDM type 0	Up/Dn – 1'b0 EMEP - **1'b1**
0x5B0	vesc_reg42[29]	**cb_dis_invld_tlp_lenchk** 1'b0: Port checks TLP length and Parity. Assert a framing error if check does not pass. 1'b1 : Port doesn't check TLP length and Parity.	1'b0
0x5B0	vesc_reg42[30]	**cb_gen2_early_rx_valid_dis** 1'b0 : RxValid is asserted one cycle earlier in PIPEDemux in order not to miss first Gen2 EIEOS 1'b1 : Issue is not fixed (first EIEOS is missed)	1'b0

Table 71. VESC_REG 42: (Offset B0h): General configuration register

Offset	Bits	Description	Value
0x5B0	vesc_reg42[31]	**cb_gen3_early_rx_valid_dis** 1’b0 : RxValid is asserted one cycle earlier in PIPEDemux in order not to miss first Gen3 EIEOS 1’b1 : Issue is not fixed (first EIEOS is missed)	**1'b1**

Table 72. VESC_REG 43: (Offset B4h): General configuration register

Offset	Bits	Description	Value
0x5B4	vesc_reg43[3:0]	**cb_preset_to_use_ln0** Value of the preset to use during the master phase on lane0 (Valid values are 0 to A)	4'h0
0x5B4	vesc_reg43[7:4]	**cb_preset_to_use_ln1:** Value of the preset to use during the master phase on lane1 (Valid values are 0 to A)	4'h0
0x5B4	vesc_reg43[11:8]	**cb_preset_to_use_ln2** Value of the preset to use during the master phase on lane2 (Valid values are 0 to A)	4'h0
0x5B4	vesc_reg43[15:12]	**cb_preset_to_use_ln3** Value of the preset to use during the master phase on lane3 (Valid values are 0 to A)	4'h0
0x5B4	vesc_reg43[19:16]	**cb_preset_to_request** Value of the preset to request during the master phase (Valid values are 0 to A)	4'h0 (Sim - Eq)
0x5B4	vesc_reg43[20]	**cb_dn_ph3_later_entry_en** 1’b0 : no effect 1’b1 : Delay entry of Dn Port to Phase 3	1'b0 (Sim - Eq)
0x5B4	vesc_reg43[21]	**cb_force_constant_preset** 1’b0 : no effect 1’b1 : Option to force on PIPE preset values from register (Value is taken from bits [19:16])	1'b0
0x5B4	vesc_reg43[22]	**cb_eq_use_rx_preset_dis** 1’b0 : Port reacts on “Use Preset” from Partner 1’b1 : Port ignores “Use Preset” from Partner	1'b0 (Sim - Eq)

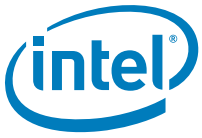


Table 72. VESC_REG 43: (Offset B4h): General configuration register

Offset	Bits	Description	Value
0x5B4	vesc_reg43[23]	**cb_check_valid_rx_preset_dis** 1'b0 : Port checks if Rx Preset is valid 1'b1 : Port doesn't check if Rx Preset is valid	1'b0
0x5B4	vesc_reg43[24]	**cb_only_one_good_eq** 1'b0 : no effect 1'b1 : Only one good Equalization Evaluation needed	1'b0
0x5B4	vesc_reg43[25]	**cb_adjusted_coeff_value** 1'b0 : Coefficient values adjusted for B step (during A-Step) 1'b1 : Coefficient values are the same as in A step	1'b0
0x5B4	vesc_reg43[26]	**cb_optimal_setting_reached_sel** 1'b0 : "optimal" condition based on "coff tmp" parameters 1'b1 : "optimal" condition based on "coff" parameters	1'b0
0x5B4	vesc_reg43[27]	**cb_force_optimal_setiing_reached** 1'b0 : no effect 1'b1 : DFT option to force "optimal" condition	1'b0
0x5B4	vesc_reg43[28]	**cb_force_all_checks_satisfied** 1'b0 : no effect 1'b1 : DFT option to force "coeff check" condition	1'b0
0x5B4	vesc_reg43[29]	**cb_toggle_invalid_request_dis** 1'b0 : no effect 1'b1 : DFT option to disabled toggle of invalid request	1'b0
0x5B4	vesc_reg43[30]	**cb_bypass_master_phase** 1'b0 : Do not Bypass the master phase of Equalization 1'b1 : Bypass the master phase of Equalization.	1'b0
0x5B4	vesc_reg43[31]	**cb_usepreset_on_rjct_coeff** 1'b0: Do not assert Use preset when coefficients are rejected. 1'b1: Assert Use preset when coefficients are rejected.	1'b0 (Sim - Eq)

Table 73. VESC_REG 44: (Offset B8h): General configuration register

Offset	Bits	Description	Value
0x5B8	vesc_reg44[0]	**cb_slave_capture_value_sel** (Equalization) 1'b0 : During Slave phase checking Stored parameters 1'b1 : During Slave phase checking Rx parameters	1'b0 (Sim - Eq)
0x5B8	vesc_reg44[1]	**cb_another_try_after_reject** (Equalization) 1'b0 : Port finish Master Phase in case of reject. 1'b1 : Port tries different Preset/Coeff in case of reject.	**1'b1**

Table 73. VESC_REG 44: (Offset B8h): General configuration register

Offset	Bits	Description	Value
0x5B8	vesc_reg44[2]	**cb_finish_after_reject_sel** 1’b0 : In case of reject Equalization fails 1’b1 : In case of reject Port goes to next step	**1'b1**
0x5B8	vesc_reg44[3]	**cb_slave_capture_value_fix_dis** 1’b0 : In Slave mode returns the values from FSM parameters (sync with FSM updates) 1’b1 : In Slave mode returns the values directly from previously capture values from TS (Need to set this bit in case of Equalization Bypass – Sim/ DFT)	1'b0
0x5B8	vesc_reg44[5:4]	**cb_eq_counter_value_sel** Select counter value during Equalization Master Phase 2'b00 600ns 2'b01 700ns 2'b10 800ns 2'b11 1us	2'b00 (Sim - Eq)
0x5B8	vesc_reg44[7:6]	**cb_num_of_good_rx_eval_sel** Selects number good Rx Evaluation 2'b00 : 2 2'b01 : 4 2'b10 : 6 2'b11 : 8	2'b00 (Sim - Eq)
0x5B8	vesc_reg44[9:8]	**cb_num_of_bad_rx_eval_sel** 2’d0 : 64 2’d1 : 128 2’d2 : 196 2’d3 : 255	2'b00
0x5B8	vesc_reg44[10]	**cb_optimal_setting_force** 1’b0 : No effect 1’b1 : Force optimal setting to 1 (DFT)	1'b0
0x5B8	vesc_reg44[11]	**cb_checks_satisfied_force** 1’b0 : No effect 1’b1 : Force check satisfied to 1 (DFT)	1'b0
0x5B8	vesc_reg44[12]	**cb_3rd_coeff_rule_check_fix_dis** Reserved extra bits for ECO	1'b0

Table 73. VESC_REG 44: (Offset B8h): General configuration register

Offset	Bits	Description	Value
0x5B8	vesc_reg44[13]	**cb_upcomp0_pase3_entry_fix_dis** Reserved extra bits for ECO	
0x5B8	vesc_reg44[14]	**cb_gen1_tx_ei_later_rise** 1’b0 : no effect 1’b1 : Tx EI assertion happens one cycle later (in Gen1)	1'b0 (Sim - rand)
0x5B8	vesc_reg44[15]	**cb_gen2_tx_ei_later_rise** 1’b0 : no effect 1’b1 : Tx EI assertion happens one cycle later (in Gen2)	1'b0 (Sim - rand)
0x5B8	vesc_reg44[16]	**cb_gen3_tx_ei_later_rise** 1’b0 : no effect 1’b1 : Tx EI assertion happens one cycle later (in Gen3)	1'b0
0x5B8	vesc_reg44[17]	**cb_gen1_tx_ei_later_fall** 1’b0 : no effect 1’b1 : Tx EI de-assertion happens one cycle later (in Gen1)	1'b0 (Sim - rand)
0x5B8	vesc_reg44[18]	**cb_gen2_tx_ei_later_fall** 1’b0 : no effect 1’b1 : Tx EI de-assertion happens one cycle later (in Gen2)	1'b0 (Sim - rand)
0x5B8	vesc_reg44[19]	**cb_gen3_tx_ei_later_fall** 1’b0 : no effect 1’b1 : Tx EI de-assertion happens one cycle later (in Gen3)	1'b0
0x5B8	vesc_reg44[20]	**cb_tx_elec_idle_delay_sel** Fix to prevent SyncHdr of during TxEI entry or exit Selects the Tx EI that wil be used to force SynHdr to 2’b01 1’b0 : Tx EI in PHYTX uses early version 1’b1 : Tx EI in PHYTX uses late version	1'b0
0x5B8	vesc_reg44[21]	**cb_sync_hdr_tx_ei_sel** Selects the Tx EI that wil be used to force SynHdr to 2’b01 1’b0 : Uses long version (early assertion / later de-assertion) 1’b1 : one version is used (controlled by previous bit)	1'b0
0x5B8	vesc_reg44[22]	**cb_gen3_tx_data_valid_gap_fix_dis** 1’b0 : Fix to hold Tx Data Valid after Tx EI de-assertion. 1’b1 : Tx Data Valid is de-asserted after Tx EI de-assertion.	1'b0

Table 73. VESC_REG 44: (Offset B8h): General configuration register

Offset	Bits	Description	Value
0x5B8	vesc_reg44[23]	**cb_eidleset_rec_disable** 1’b0 : Recovery Speed condition includes EIOS indication 1’b1 : Disable EIOS indication in the condition	1'b0 (Sim - rand)
0x5B8	vesc_reg44[24]	**cb_later_eios_done_en** 1’b0 : no effect 1’b1 : Enables one cycle delay on EIOS sent indication	1'b0
0x5B8	vesc_reg44[25]	**cb_poll_eios_send_fix_dis** 1’b0 : Fix to change speed only after EIOS was sent 1’b1 : Disable the fix (This bit should be set for Compliance testing)	1'b0
0x5B8	vesc_reg44[26]	**cb_capture_gen3_value_fix_dis** 1’b0 : Capture Gen3 value if ConsecTS >= 2 1’b1 : Capture Gen3 value if ConsecTS = 2	1'b0
0x5B8	vesc_reg44[27]	**cb_exit_elec_idle_for_infer_idle_sel** 1’b0 – Exit from Rx EI for EI infer FSM based on all lanes 1’b1 – Exit from Rx EI for EI infer FSM based on any lanes	1'b0 (Sim - rand)
0x5B8	vesc_reg44[28]	**cb_poll_active_continue_to_detect_ts** 1’b0 : no effect 1’b1 : Continue to detect TS during Polling Active	**1'b1** (Sim - rand)
0x5B8	vesc_reg44[29]	**cb_cfg_start_continue_to_detect_ts** 1’b0 : no effect 1’b1 : Continue to detect TS during Configuration Start	**1'b1** (Sim - rand)
0x5B8	vesc_reg44[30]	**cb_cfg_complete_continue_to_detect_ts** 1’b0 : no effect 1’b1 : Continue to detect TS during Configuration Complete	**1'b1** (Sim - rand)
0x5B8	vesc_reg44[31]	**cb_eidle_recov_enable** 1’b0 : no effect 1’b1 : Enable Rx EI indication according to PIPE signal for Recovery FSM	**1'b1** (Sim - rand)

Table 74. VESC_REG 45: (Offset BCh): General configuration register

Offset	Bits	Description	Value
0x5BC	vesc_reg45[0]	**cb_xmode_delay_dis** 1’b0: Internal xmode indication is delayed for one cycle 1’b1: Fix of delaying internal xmode indication is disabled	1'b0

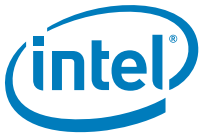


Table 74. VESC_REG 45: (Offset BCh): General configuration register

Offset	Bits	Description	Value
0x5BC	vesc_reg45[1]	**cb_mask_frame_err_detected** 1'b0: No effect 1'b1: Option to mask Frame Error detection (DFT)	1'b0
0x5BC	vesc_reg45[2]	**cb_mask_frame_err_tlp** 1'b0: No effect 1'b1: Option to mask Frame Error TLP detection (DFT)	1'b0
0x5BC	vesc_reg45[3]	**cb_disable_tlp_len_err_x1mode** 1'b0: No effect 1'b1: Option to mask TLP length error detection in x1 (DFT)	1'b0
0x5BC	vesc_reg45[4]	**cb_disable_tlp_len_err_x2mode** 1'b0: No effect 1'b1: Option to mask TLP length error detection in x2 (DFT)	1'b0
0x5BC	vesc_reg45[5]	**cb_disable_tlp_len_err_x4mode** 1'b0: No effect 1'b1: Option to mask TLP length error detection in x4 (DFT)	1'b0
0x5BC	vesc_reg45[6]	**cb_disable_frame_err_x1mode** 1'b0: No effect 1'b1: Option to mask Frame Error detection in x1 (DFT)	1'b0
0x5BC	vesc_reg45[7]	**cb_disable_frame_err_x2mode** 1'b0: No effect 1'b1: Option to mask Frame Error detection in x2 (DFT)	1'b0
0x5BC	vesc_reg45[8]	**cb_disable_frame_err_x4mode** 1'b0: No effect 1'b1: Option to mask Frame Error detection in x4 (DFT)	1'b0
0x5BC	vesc_reg45[9]	**cb_stp_align_dllp_detect_x1_dis** 1'b0: Fix to ignore DLLP it STP Alignment block in order not to indicate false Framing Errors in x1 mode 1'b1: Fix is disabled	1'b0
0x5BC	vesc_reg45[10]	**cb_stp_align_dllp_detect_x2_dis** 1'b0: Fix to ignore DLLP it STP Alignment block in order not to indicate false Framing Errors in x2 mode 1'b1: Fix is disabled	1'b0
0x5BC	vesc_reg45[11]	**cb_stp_align_dllp_detect_x4_dis** 1'b0: Fix to ignore DLLP it STP Alignment block in order not to indicate false Framing Errors in x4 mode 1'b1: Fix is disabled	1'b0

Table 74. VESC_REG 45: (Offset BCh): General configuration register

Offset	Bits	Description	Value
0x5BC	vesc_reg45[12]	**cb_cfg_frame_err_dis** 1'b0: No Effect 1'b1: Disable Frame Error detection in Configuration (DFT)	1'b0
0x5BC	vesc_reg45[13]	**cb_recov_frame_err_dis** 1'b0: No Effect 1'b1: Disable Frame Error detection in Recovery (DFT)	1'b0
0x5BC	vesc_reg45[14]	**cb_gen3_count_sync_fix_en** 1'b0: No Effect 1'b1: Part of bad fix trial of sync TxDataValid and TxEI (vesc_reg46[22] is the correct fix)	1'b0
0x5BC	vesc_reg45[15]	**cb_gen3_count_sync_early_en** 1'b0: No Effect 1'b1: Part of bad fix trial of sync TxDataValid and TxEI (vesc_reg46[22] is the correct fix)	1'b0
0x5BC	vesc_reg45[16]	**cb_move_to_rcvr_cfg_fix_dis** 1'b0: Fix to move from Recovery.Lock to Recovery.Cfg only when detected exit from Rx EI 1'b1: Transition from Recovery.Lock to Recovery.Cfg ignores exit from Rx EI	1'b0
0x5BC	vesc_reg45[17]	**cb_late_eios_fix_dis** 1'b0: Fix to send EIOS one cycle earlier in Configuration state 1'b1: EIOS is sent one cycle later in Configuration state	1'b0
0x5BC	vesc_reg45[18]	**cb_delay_upcomp0_ph2_dis** (Equalization) 1'b0: Fix to delay Phase 2 to meet correct transition 1'b1: Transition happens earlier and some TS data is wrong (This bit is valid in Up/Ep ports and reserved in Dn port)	(Up/Ep) 1'b0
0x5BC	vesc_reg45[19]	**cb_delay_upcomp1_ph3_dis** (Equalization) 1'b0: Fix to delay Phase 3 to meet correct transition 1'b1: Transition happens earlier and some TS data is wrong (This bit is valid in Dn ports and reserved in Up/Ep port)	(Dn) 1'b0
0x5BC	vesc_reg45[20]	**cb_sync_hdr_mux_del_delay_en** (Equalization) 1'b0: No effect 1'b1: Fix to delay one cycle the value of 2'b01 of SyncHdr	1'b0

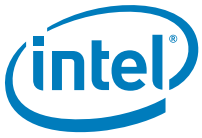


Table 74. VESC_REG 45: (Offset BCh): General configuration register

Offset	Bits	Description	Value
0x5BC	vesc_reg45[21]	**cb_sync_hdr_early_tx_ei_fix_en** 1'b0: No effect 1'b1: Internal synchdr signal changes one cycle earlier (Bad fix)	1'b0
0x5BC	vesc_reg45[22]	**cb_dynamic_coeff_calc_en** (Equalization) 1'b0: Coefficient are taken according to Preset form LUT 1'b1: Option to calculate the coefficient dynamically	1'b0 (Sim - Eq)
0x5BC	vesc_reg45[23]	**cb_upcomp0_ec11_delay_fix_dis** (Equalization) 1'b0: Fix to delay EC = 2'b11 to meet correct transition timing 1'b1: Issue where EC turns to value 2'b11 to early	1'b0
0x5BC	vesc_reg45[24]	**cb_last_rd_ptr_during_replay_fix_dis** 1'b0: Fix to load correct pointer for Replay 1'b1: Issue with loading bad pointer during Replay	1'b0
0x5BC	vesc_reg45[25]	**cb_check_fcrc_min_len_fix_dis** (Equalization) 1'b0: Ignore not valid length for FCRC calculation (below min) 1'b1: FCRC Calculation checks any length TLP	1'b0
0x5BC	vesc_reg45[26]	**cb_check_fcrc_max_len_fix_dis** (Equalization) 1'b0: Ignore not valid length for FCRC calculation (above max) 1'b1: FCRC Calculation checks any length TLP	1'b0
0x5BC	vesc_reg45[27]	**cb_ignore_phy_errors_en** 1'b0: No Effect 1'b1: Option to ignore PHY related errors for Advanced Error Reporting status bits (DFT)	1'b0
0x5BC	vesc_reg45[28]	**cb_ignore_tlp_errors** 1'b0: No Effect 1'b1: Option to ignore TLP related errors for Advanced Error Reporting status bits (DFT)	1'b0
0x5BC	vesc_reg45[29]	**cb_ignore_dllp_errors** 1'b0: No Effect 1'b1: Option to ignore DLLP related errors for Advanced Error Reporting status bits (DFT)	1'b0

Table 74. VESC_REG 45: (Offset BCh): General configuration register

Offset	Bits	Description	Value
0x5BC	vesc_reg45[30]	**cb_ignore_replay_errors** 1’b0: No Effect 1’b1: Option to ignore Replay related errors for Advanced Error Reporting status bits (DFT)	1'b0
0x5BC	vesc_reg45[31]	**cb_ignore_ur_errors** 1’b0: No Effect 1’b1: Option to ignore UR related errors for Advanced Error Reporting status bits (DFT)	1'b0

Table 75. VESC_REG 46: (Offset C0h): General configuration register

Offset	Bits	Description	Value
0x5C0	vesc_reg46[0]	**cb_force_fs_from_reg** (Gen3) 1’b0: Local FS value is taken from PHY 1’b1: Local FS value is taken from bits 7:2 (DFT)	1’b0
0x5C0	vesc_reg46[1]	**cb_force_lf_from_reg** (Gen3) 1’b0: Local LF value is taken from PHY 1’b1: Local LF value is taken from bits 13:8 (DFT)	1’b0
0x5C0	vesc_reg46[7:2]	**cb_local_fs_from_reg** (Gen3) Local FS value to take instead of PHY value This value is used if bit 0 is set	5’h0
0x5C0	vesc_reg46[13:8]	**cb_local_lf_from_reg** (Gen3) Local LF value to take instead of PHY value This value is used if bit 1 is set	5’h0
0x5C0	vesc_reg46[14]	**cb_mask_start_block_after_ei_en** (Gen3) 1’b0: No effect 1’b1: Internally mask start block signals during Tx EI	1’b0
0x5C0	vesc_reg46[15]	**cb_mask_data_sync_hdr_after_ei_dis** (Gen3) 1’b0: Internally force sync header signals during Tx EI to 2'b01 1’b1: Sync Header is driven to 2'b10 during Tx EI (bug)	1’b0
0x5C0	vesc_reg46[16]	**cb_l0s_rx_entry_upon_rx_ei** 1’b0: EI detection for entry to L0sRx upon Rx EI or EIOS. 1’b1: EI detection for entry to L0sRx upon EIOS on any lane.	1’b0 (Sim - rand)
0x5C0	vesc_reg46[17]	**cb_early_skip_det_fix_dis** 1’b0: Fix of issue in L0sRx where SKIP detection is too early. 1’b1: Disable the fix of too early SKIP detection in L0sRx.	1’b0

Table 75. VESC_REG 46: (Offset C0h): General configuration register

Offset	Bits	Description	Value
0x5C0	vesc_reg46[18]	**cb_l0s_skip_detect_fix_dis** 1'b0: Fix to save the indication of received Skip in L0sRx 1'b1: Disable the fix of Skip detection flag.	1'b0
0x5C0	vesc_reg46[19]	**cb_early_sds_det_fix_dis** 1'b0: Fix of issue in L0sRx where SDS detection is too early (Bad fix) 1'b1: Disable the fix of too early SDS detection in L0sRx.	**1'b1**
0x5C0	vesc_reg46[20]	**cb_l0s_sds_detect_fix_dis** 1'b0: Fix to save the indication of received SDS in L0sRx 1'b1: Disable the fix of SDS detection flag.	1'b0
0x5C0	vesc_reg46[21]	**cb_sel_time_of_invalid_request** (Equalization) Selects the time invalid request will be asserted 1'b0: 2 cycles 1'b1: 8 cycles	1'b0 (Sim - Eq)
0x5C0	vesc_reg46[22]	**cb_sync_tx_valid_and_ei_fix_dis** (Gen3) 1'b0: Fix to sync TxDataValid assertion to de-assertion of Rx Electrical Idle to meet PIPE Spec timing 1'b1: The issue is not fixed	1'b0
0x5C0	vesc_reg46[23]	**cb_xmode_phy_tx_delay_dis** 1'b0: Fix to delay xmode indication for Rx block 1'b1: Fix to delay xmode indication for Rx block is disabled	1'b0
0x5C0	vesc_reg46[24]	**cb_xmode_phy_rx_delay_dis** 1'b0: Fix to delay xmode indication for Tx block 1'b1: Fix to delay xmode indication for Tx block is disabled	1'b0
0x5C0	vesc_reg46[25]	**cb_dn_retrain_link_upon_up_rate_change_en** 1'b0: No effect 1'b1: Retrain Link of Dn Port while Up Port changes speed (This bit is valid for Dn port and reserved for Up/Ep)	(Dn) 1'b0
0x5C0	vesc_reg46[26]	**cb_disable_retrain_link_dllp_absence** 1'b0: No Effect 1'b1: Disable Link Recovery due to absence of DLLP (DFT)	1'b0

Table 75. VESC_REG 46: (Offset C0h): General configuration register

Offset	Bits	Description	Value
0x5C0	vesc_reg46[28:27]	**cb_retrain_link_value_sel** Selects timeout value of DLLP absence for Link Recovery 2'b00: 256 us 2'b01: 512 us 2'b10: 1 ms 2'b11: 4 ms	2'b00
0x5C0	vesc_reg46[29]	**cb_send_less_periodic_fc_dllp** 1'b0: No effect 1'b1: Send less periodic DLLP FC Update	1'b0 (Sim - rand)
0x5C0	vesc_reg46[30]	**cb_slow_clk_faster_dllp_update_en** 1'b0: No effect 1'b1: During L1/L2 without Clock and using slow internal clock periodic DLLP timer acceleration	**1'b1**
0x5C0	vesc_reg46[31]	**cb_mask_frame_err_duringdl_rise_dis** 1'b0: Fix to mask frame error during DL rise 1'b1: Fix is disabled	1'b0

Table 76. VESC_REG 47: (Offset C4h): General configuration register

Offset	Bits	Description	Value
0x5C4	vesc_reg47[0]	**cb_skip_det_shift_en** 1'b0: No effect 1'b1: Option to detect SKIP if internally it was shifted	1'b0
0x5C4	vesc_reg47[1]	**cb_sds_detect_by_12_bytes** 1'b0: No effect 1'b1: Option to detect SDS by less bytes (12 instead of 16)	**1'b1**
0x5C4	vesc_reg47[2]	**cb_main_lane_not_active_fix_en** 1'b0: No effect 1'b1: Fix to reset Rx Data Path is main lane is not active	**1'b1** (Sim - rand)
0x5C4	vesc_reg47[3]	**cb_false_dllp_chk_dis** 1'b0: Fix for not to miss TLP because of DLLP before it 1'b1: Fix is disabled	1'b0
0x5C4	vesc_reg47[4]	**cb_false_dllp_chk_dis_short** 1'b0: Fix for not to miss TLP because of back to back DLLP before it (treats slightly different case them bit 3) 1'b1: Fix is disabled	1'b0

Table 76. VESC_REG 47: (Offset C4h): General configuration register

Offset	Bits	Description	Value
0x5C4	vesc_reg47[5]	**cb_plmux_tx_ei_gap_fix_dis** 1'b0: Fix to leave Tx EI asserted till TxDataValid is asserted 1'b1: Fix is disabled	1'b0
0x5C4	vesc_reg47[6]	**cb_early_tx_ei_fall_2mux** 1'b0 : No effect 1'b1 : Option to de-assert internal Tx EI earlier (DFT)	1'b0
0x5C4	vesc_reg47[7]	**cb_slave_delay_byte6_fix_dis** (Equalization) 1'b0: Fix to align TS byte 6 with EC during Eq slave phase 1'b1: Fix is disabled	1'b0
0x5C4	vesc_reg47[8]	**cb_custom_clr_equalization_done** (Equalization 1'b0 : No effect 1'b1 : Custom DFT bit to clear Equalization done indication	1'b0
0x5C4	vesc_reg47[9]	**cb_perform_equal_every_rate_change** (Equalization) 1'b0: No effect 1'b1: Equalization will be performed at every entry to Gen3	1'b0
0x5C4	vesc_reg47[10]	**cb_upcomp0_end_of_phase3_fix_dis** (Equalization) 1'b0: Align TS EC/coeff fields at the end of Eq Phase 3 1'b1: The delay is disabled	1'b0
0x5C4	vesc_reg47[11]	**cb_upcomp1_end_of_phase2_fix_dis** (Equalization) 1'b0: Align TS EC/coeff fields at the end of Eq Phase 2 1'b1: The delay is disabled	1'b0
0x5C4	vesc_reg47[12]	**cb_delay_frame_error_dis** 1'b0 : Frame Error indication is delayed in LTSSM 1'b1 : The delay is disabled	1'b0
0x5C4	vesc_reg47[13]	**cb_mask_frame_err_with_ei** 1'b0: Frame Error indication is valid only if there is no Rx EI 1'b1: Rx EI doesn't mask Framing Error	1'b0
0x5C4	vesc_reg47[14]	**cb_tx_data_valid_fall_sync_fix_en** 1'b0: Fix to align TxDataValid cycle shortly after end of Tx EI 1'b1: Fix is disabled	1'b0
0x5C4	vesc_reg47[15]	**cb_gen3_delay_tx_ei_fix_dis** 1'b0: Fix to delay Tx EI de-assertion till TxDataValid cycle 1'b1: Fix is disabled	1'b0

Table 76. VESC_REG 47: (Offset C4h): General configuration register

Offset	Bits	Description	Value
0x5C4	vesc_reg47[16]	**cb_reset_fsm_in_tx_ei_fix_dis** 1'b0: Reset PIPEMux FSM during Tx EI in Gen3 fix 1'b1: Fix is disabled	1'b0
0x5C4	vesc_reg47[17]	**cb_gen3_mult_eieos_fix_dis** (Recovery) 1'b0: Send several EIEOS during exit from Tx EI (in Gen3) 1'b1: Send only one EIEOS during exit from TxEI (One EIEOS can be missed due to TxEI /TDataValid fixes)	1'b0
0x5C4	vesc_reg47[18]	**cb_gen3_num_of_eieos_sel** (Recovery) 1'b0: Launch 3 EIEOS (should insure at least one EIEOS in PIPE) 1'b1: Launch 4 EIEOS	1'b0
0x5C4	vesc_reg47[19]	**cb_gen3_l0stx_mult_eieos_fix_dis** (L0s) 1'b0: Send several EIEOS during exit from Tx EI (in Gen3) 1'b1: Send only one EIEOS during exit from TxEI (One EIEOS can be missed due to TxEI /TDataValid fixes)	1'b0
0x5C4	vesc_reg47[20]	**cb_gen3_l0stx_num_of_eieos_sel** (L0s) 1'b0: Launch 3 EIEOS (should insure at least one EIEOS in PIPE) 1'b1: Launch 4 EIEOS	1'b0
0x5C4	vesc_reg47[21]	**cfg_lane_num_wait_timer_fix_dis** 1'b0: Extra time wait enable in Config.LaneNumAccept state 1'b1: Extra time wait disabled in Config.LaneNumAccept state (1'b1 might be problematic in Lane Reversal)	1'b0 (Sim - rand)
0x5C4	vesc_reg47[22]	**cfg_lane_num_wait_sel** 1'b0: Extra time wait is till next us tick 1'b1: Extra time wait is till end of state timeout	1'b0
0x5C4	vesc_reg47[23]	**cb_gen3_comp_pattern_align_fix_dis** 1'b0: Fix of delaying start of Compliance Pattern till de-assertion of Tx Electrical Idle 1'b1: Fix is disabled	1'b0
0x5C4	vesc_reg47[24]	**cb_gen3_eieos_pipe_demux_align_en** 1'b0: No effect 1'b1: Re-align PIPEDemux at EIEOS	1'b0

Table 76. VESC_REG 47: (Offset C4h): General configuration register

Offset	Bits	Description	Value
0x5C4	vesc_reg47[25]	**cb_pipe_demux_rst_after_de_skew_en** 1'b0: No effect 1'b1: Reset PIPEDemux after each change of De-Skew	**1'b1**
0x5C4	vesc_reg47[26]	Reserved	1'b0
0x5C4	vesc_reg47[27]	Reserved	1'b0
0x5C4	vesc_reg47[28]	Reserved	1'b0
0x5C4	vesc_reg47[29]	**cb_fine_adjust_shorter_dis** While comes to this state from Credit Update state 1'b0: Arbiter wait 2 cycles in Fine Adjust state 1'b1: Arbiter wait 3 cycles in Fine Adjust state	1'b0
0x5C4	vesc_reg47[30]	Reserved	1'b0
0x5C4	vesc_reg47[31]	Reserved	1'b0

Table 77. VESC_REG 48: (Offset C8h): General configuration register

Offset	Bits	Description	Value
0x5C8	vesc_reg48[0]	**cb_pmtop_ei_alllanes_sel** (all lanes for PMTop block) 1'b0: Rx EI detection according to PIPE signals 1'b1: Rx EI detection according internal indication (in non Gen1 mode generated from EIOS / EIEOS packets)	1'b0
0x5C8	vesc_reg48[1]	**cb_after_invalid_request_change_coeff** (Equalization) 1'b0: Try same coeffs after invalid request 1'b1: Try different coeffs after invalid request	1'b0
0x5C8	vesc_reg48[2]	**cb_upcomp0_end_of_ph3_delay_sel** 1'b0: Fix of delaying Phase 3 in Dn Port 1'b1: Fix is disabled	1'b0
0x5C8	vesc_reg48[3]	**cb_upcomp1_end_of_ph2_delay_sel** 1'b0 : Fix of delaying Phase 2 in Up/Rp Port 1'b1 : Fix is disabled	1'b0
0x5C8	vesc_reg48[4]	**cb_wait_for_preset_change** 1'b0: Fix is not enabled 1'b1: During Equalization Slave phase wait for Preset change before each new validation of coeffs	**1'b1**
0x5C8	vesc_reg48[5]	**cb_detect_rx_ei_any_sel_det** (any lane for Detect) 1'b0: Rx EI is detected according to PIPE signal 1'b1: Rx EI is detected according PIPE signal in Gen1 and according EIOS/PIPE signal in Gen2/Gen3 (vesc_reg41[3:1])	1'b0

Table 77. VESC_REG 48: (Offset C8h): General configuration register

Offset	Bits	Description	Value
0x5C8	vesc_reg48[6]	**cb_detect_rx_ei_any_sel_poll** (any lane for Polling) 1'b0: Rx EI is detected according to PIPE signal 1'b1: Rx EI is detected according PIPE signal in Gen1 and according EIOS/PIPE signal in Gen2/Gen3 (vesc_reg41[3:1])	1'b0
0x5C8	vesc_reg48[7]	**cb_detect_rx_ei_any_sel_recov** (any lane for Recovery) 1'b0: Rx EI is detected according to PIPE signal 1'b1: Rx EI is detected according PIPE signal in Gen1 and according EIOS/PIPE signal in Gen2/Gen3 (vesc_reg41[3:1])	**1'b1** (Sim - rand)
0x5C8	vesc_reg48[8]	**cb_detect_rx_ei_all_sel_ltssm** (all lanes for LTSSM) 1'b0: Rx EI is detected according PIPE signal in Gen1 and according EIOS/PIPE signal in Gen2/Gen3 (vesc_reg41[3:1]) 1'b1: Rx EI is detected according to PIPE signal	1'b0 (Sim - rand)
0x5C8	vesc_reg48[9]	**cb_detect_rx_ei_all_sel_hot** (all lanes for Hot Reset) 1'b0: Rx EI is detected according PIPE signal in Gen1 and according EIOS/PIPE signal in Gen2/Gen3 (vesc_reg41[3:1]) 1'b1: Rx EI is detected according to PIPE signal	1'b0
0x5C8	vesc_reg48[10]	**cb_detect_rx_ei_all_sel_l0s** (all lanes for L0s) 1'b0: Rx EI is detected according PIPE signal in Gen1 and according EIOS/PIPE signal in Gen2/Gen3 (vesc_reg41[3:1]) 1'b1: Rx EI is detected according to PIPE signal	1'b0 (Sim - rand)
0x5C8	vesc_reg48[11]	**cb_detect_rx_ei_all_sel_l1prep** (all lanes for L1Prep) 1'b0: Rx EI is detected according PIPE signal in Gen1 and according EIOS/PIPE signal in Gen2/Gen3 (vesc_reg41[3:1]) 1'b1: Rx EI is detected according to PIPE signal	1'b0 (Sim - rand)
0x5C8	vesc_reg48[12]	**cb_detect_rx_ei_all_sel_l1seq** (all lanes for L1Seq) 1'b0: Rx EI is detected according PIPE signal in Gen1 and according EIOS/PIPE signal in Gen2/Gen3 (vesc_reg41[3:1]) 1'b1: Rx EI is detected according to PIPE signal	1'b0 (Sim - rand)
0x5C8	vesc_reg48[13]	**cb_detect_rx_ei_all_sel_l2seq** (all lanes for L2Seq) 1'b0: Rx EI is detected according PIPE signal in Gen1 and according EIOS/PIPE signal in Gen2/Gen3 (vesc_reg41[3:1]) 1'b1: Rx EI is detected according to PIPE signal	1'b0 (Sim - rand)
0x5C8	vesc_reg48[14]	**cb_anylane_exit_rx_ei_sel_detect** (any lane for Detect) 1'b0: Rx EI exit is detected according to PIPE signal 1'b1: Rx EI exit is detected according PIPE signal in Gen1 and according EIOS/PIPE signal in Gen2/Gen3 (vesc_reg41[3:1])	1'b0

Table 77. VESC_REG 48: (Offset C8h): General configuration register

Offset	Bits	Description	Value
0x5C8	vesc_reg48[15]	**cb_anylane_exit_rx_ei_sel_comp** (any lane for Comp) 1'b0: Rx EI exit is detected according to PIPE signal 1'b1: Rx EI exit is detected according PIPE signal in Gen1 and according EIOS/PIPE signal in Gen2/Gen3 (vesc_reg41[3:1])	1'b0
0x5C8	vesc_reg48[16]	**cb_anylane_exit_rx_ei_sel_dis** (any lane for Disabled) 1'b0: Rx EI exit is detected according to PIPE signal 1'b1: Rx EI exit is detected according PIPE signal in Gen1 and according EIOS/PIPE signal in Gen2/Gen3 (vesc_reg41[3:1])	1'b0
0x5C8	vesc_reg48[17]	**cb_alllanes_exit_rx_ei_sel_poll** (all lane for Polling) 1'b0: Rx EI exit is detected according to PIPE signal 1'b1: Rx EI exit is detected according PIPE signal in Gen1 and according EIOS/PIPE signal in Gen2/Gen3 (vesc_reg41[3:1])	1'b0
0x5C8	vesc_reg48[18]	**cb_alllanes_exit_rx_ei_sel_loop** (all lane for Loop) 1'b0: Rx EI exit is detected according to PIPE signal 1'b1: Rx EI exit is detected according PIPE signal in Gen1 and according EIOS/PIPE signal in Gen2/Gen3 (vesc_reg41[3:1])	1'b0
0x5C8	vesc_reg48[19]	**cb_rst_ts_detection_during_speed_fix** 1'b0: Fix is not enabled 1'b1: Fix in Recovery.Speed to reset TS detection	**1'b1**
0x5C8	vesc_reg48[20]	**cb_delay_exit_from_comp** 1'b0: No effect 1'b1: Delay of one cycle during exit from Compliance	1'b0
0x5C8	vesc_reg48[21]	**cb_gen3_longer_eios_detect_en** 1'b0: Gen3 EIOS detection according to Spec (4 symbols) 1'b1: EIOS detection based on 8 symbols	1'b0
0x5C8	vesc_reg48[22]	**cb_gen3_l0srx_deskew_on_sds** 1'b0: Perform Gen3 de-skew on FTS during exit from L0sRx 1'b1: Perform Gen3 de-skew on SDS during exit from L0sRx	1'b0 (Sim - rand)
0x5C8	vesc_reg48[23]	**cb_gen2_l0srx_deskew_on_fts** 1'b0: Perform Gen2 de-skew on SKIP during exit from L0sRx 1'b1: Perform Gen2 de-skew on FTS during exit from L0sRx	**1'b1** **(1'b0 in B-Step)** (Sim - rand in B-step)

Table 77. VESC_REG 48: (Offset C8h): General configuration register

Offset	Bits	Description	Value
0x5C8	vesc_reg48[24]	**cb_second_l1soft_dis** 1’b0: Disable second L1Soft after return to D0 (bad fix) 1'b1: Second L1Soft might happen after return to D0 (bug)	**1'b1**
0x5C8	vesc_reg48[26:25]	**cb_recov_eq_counter_value_sel** Up/Dn wait time in Phase 0/1 2’b00: 0.3 us 2’b01: 0.6 us 2’b00: 0.9 us 2’b01: 1.2 us	**1'b01**
0x5C8	vesc_reg48[27]	**cb_l1_aspm_l1_timer_en** 1’b0: After detecting Rx EI in ASPM L1 exit condition valid immediately 1’b1: After detecting Rx EI in ASPM L1 exit condition valid after some time	**1'b1** (Sim - rand)
0x5C8	vesc_reg48[28]	**cb_l1_soft_l1_timer_en** 1’b0: After detecting Rx EI in Soft L1 exit condition valid immediately 1’b1: After detecting Rx EI in Soft L1 exit condition valid after some time	**1'b1** (Sim - rand)
0x5C8	vesc_reg48[29]	**cb_pipe_mux_delay_tx_ei_dis** 1’b0: PIPE Mux Tx EI is delayed by one cycle 1’b1: PIPE Mux Tx EI is not delayed by one cycle	1'b0 **1'b1** – for gen3 compliance testing
0x5C8	vesc_reg48[30]	**cb_pipe_mux_ei_start_block_fix_en** 1’b0: No effect 1’b1: Last Start Block after EIOS is masked (Bad fix)	1'b0
0x5C8	vesc_reg48[31]	**cb_pipe_mux_ei_data_valid_fix_dis** 1’b0: No effect 1’b1: Fix to leave TxDataValid high during TxEI (Bad fix)	1'b0

Table 78. VESC_REG 49: (Offset CCh): General configuration register

Offset	Bits	Description	Value
0x5CC	vesc_reg49[7:0]	**cb_custom_init_bus_num_load** The value will be loaded to Bus Number after Link Up	8'h0
0x5CC	vesc_reg49[8]	**cb_custom_send_pm_pme_msg** 1’b0: No effect 1’b1: Option to trigger PM_PME message	1'b0

Table 78. VESC_REG 49: (Offset CCh): General configuration register

Offset	Bits	Description	Value
0x5CC	vesc_reg49[9]	**cb_disable_pm_pme_msg** 1’b0: No effect 1’b1: Disable PM_PME message send	1'b0
0x5CC	vesc_reg49[10]	**cb_early_send_eios_fix_dis** 1’b0: EIOS send fix 1’b1:Fix is disabled	1'b0
0x5CC	vesc_reg49[11]	**cb_exit_ei_flag_fall_upon_rx_ei_en** 1’b0: No effect 1’b1: Rx EI exit flag is de-asserted upon Rx EI signal	**1'b1**
0x5CC	vesc_reg49[12]	**cb_exit_ei_flag_rise_upon_rx_ei_en** 1’b0: No effect 1’b1: Rx EI exit flag is asserted upon Rx EI signal	1'b0
0x5CC	vesc_reg49[13]	**cb_chan_arb_rr_fix_dis** 1’b0: Channel Arbiter is Round Robin (fix) 1’b1: Channel Arbiter is Round Robin only under stress traffic	1'b0
0x5CC	vesc_reg49[14]	**cb_chan_arb_vc0_cfg** 1’b0: Default order of channel in arbitration (VC0) 1’b1: Different order of channels for Up/Dn (VC0)	1'b0
0x5CC	vesc_reg49[15]	**cb_chan_arb_vc1_cfg** 1’b0: Default order of channel in arbitration (VC1) 1’b1: Different order of channels for Up/Dn (VC1)	1'b0
0x5CC	vesc_reg49[16]	**cb_l1_aspm_timer_sel** Select the l1 ASPM timer value (clock cycles) 1’b0: 30 1’b1: 60	1'b0
0x5CC	vesc_reg49[17]	**cb_l1_soft_timer_sel** Select the l1 Soft timer value (clock cycles) 1’b0: 30 1’b1: 60	1'b0
0x5CC	vesc_reg49[18]	**cb_init_l1_exit_en** 1’b0: L1 exit indication toward other ports is forced to zero 1’b1: Enable to assert L1 exit indication toward other ports	1'b0

Table 78. VESC_REG 49: (Offset CCh): General configuration register

Offset	Bits	Description	Value
0x5CC	vesc_reg49[19]	**cb_exit_l1_by_other_port_dis** 1'b0: Exit from L1 triggered by indication from other ports 1'b1: Exit from L1 by indication from other ports is disabled	1'b0
0x5CC	vesc_reg49[20]	**cb_l0s_gen2_exit_12_eie_en** 1'b0: Rx EI exit is detected by full EIEOS. 1'b1: Enable to detect Rx EI exit in gen2 by 12 EIE symbols	1'b0
0x5CC	vesc_reg49[21]	**cb_send_extra_skip_in_recov_cfg** 1'b0: No effect 1'b1: Send extra Skip during transition to Recovery.Cfg	1'b0
0x5CC	vesc_reg49[22]	**cb_gen2_4_eie_detect_en** 1'b0: Rx EI exit is detected by 8 or more EIE (also EIEOS) 1'b1: Enable to detect Rx EI exit in gen2 by 4 EIE symbols	1'b0
0x5CC	vesc_reg49[23]	**cb_dllp_detect_mask_during_tlp_ip_x1_en** 1'b0: No effect 1'b1: Mask DLLP detection during valid TLP in gen3 x1 mode	**1'b1**
0x5CC	vesc_reg49[24]	**cb_dllp_detect_mask_during_tlp_ip_x2_en** 1'b0: No effect 1'b1: Mask DLLP detection during valid TLP in gen3 x2 mode	1'b0
0x5CC	vesc_reg49[25]	**cb_dllp_detect_mask_during_tlp_ip_x4_en** 1'b0: No effect 1'b1: Mask DLLP detection during valid TLP in gen3 x4 mode	1'b0
0x5CC	vesc_reg49[26]	**cb_enable_extra_skip_after_l0** 1'b0: No effect 1'b1: Adds extra Skip in the beginning of Recovery state	1'b0
0x5CC	vesc_reg49[27]	**cb_entry_to_recov_speed_strech** 1'b0: No effect 1'b1: Stretches entry to Recovery.Speed indication	**1'b1**

Table 78. VESC_REG 49: (Offset CCh): General configuration register

Offset	Bits	Description	Value
0x5CC	vesc_reg49[28]	**cb_consider_eios_detected_on_rx_ei_rise** 1'b0: No effect 1'b1: EIOS detected indication is asserted on Rx EI rise (This can be used if Rx EI detection happens in the PHY and EIOS is not reliably detected)	1'b0
0x5CC	vesc_reg49[29]	**cb_redund_recov_after_l1_hot_reset_fix_dis** 1'b0: Fix to eliminate redundant Recovery in case of Hot Reset trigger during L1 state. 1'b1: Fix is disabled	1'b0
0x5CC	vesc_reg49[30]	**cb_redund_recov_after_l1_retrain_fix_dis** 1'b0: Fix to eliminate redundant Recovery in case of Link Retraining trigger during L1 state. 1'b1: Fix is disabled	1'b0
0x5CC	vesc_reg49[31]	Reserved	1'b0

Table 79. VESC_REG 50: (Offset D0h): General configuration register

Offset	Bits	Description	Value
0x5D0	vesc_reg50[1:0]	**cb_delay_ei_infer_detect_indication** Control the delays of EI inferring indication to PHY 2'b00: 4 cycles 1'b01: 8 cycles 1'b01: 12 cycles 1'b01: 16 cycles	2'b00
0x5D0	vesc_reg50[2]	**cb_delay_eios_detect_indication** 1'b0: No effect 1'b1: Delays EIOS detection indication to PHY for 2 cycles	2'b0
0x5D0	vesc_reg50[3]	**cb_gen2_rxvalid_rise_rst_pipedemux** 1'b0: No effect 1'b1: Reset PIPEDemux upon any RxValid rise in Gen2	1'b0
0x5D0	vesc_reg50[4]	**cb_gen3_rxvalid_rise_rst_pipedemux** 1'b0: No effect 1'b1: Reset PIPEDemux upon any RxValid rise in Gen3	1'b0/ **1'b1**
0x5D0	vesc_reg50[5]	**cb_dllsm_inactive_for_l0s_fix_dis** 1'b0: L0sPrep FSM doesn't enter L0s during DLLSM activity 1'b1: Disable the fix	1'b0

Table 79. VESC_REG 50: (Offset D0h): General configuration register

Offset	Bits	Description	Value
0x5D0	vesc_reg50[6]	**cb_pol_force_deemp_from_link_ctrl2_reg_en** 1'b0: No effect 1'b1: Forces TxDemph directly from link ctrl 2 register	1'b0
0x5D0	vesc_reg50[7]	**cb_rx_valid_drop_upon_rx_ei_en** 1'b0: No effect 1'b1: Drops RxValid upon Rx EI assertion in LaneReversal	**1'b1**
0x5D0	vesc_reg50[8]	**cb_rx_data_valid_drop_upon_rx_ei_en** 1'b0: No effect 1'b1: Drops RxDataValid upon Rx EI assertion in LaneReversal	**1'b1**
0x5D0	vesc_reg50[9]	**cb_blk_align_assert_during_recovery** 1'b0: No effect 1'b1: Block align control is asserted during Recovery state	**1'b1**
0x5D0	vesc_reg50[10]	**cb_blk_align_assert_during_configuration** 1'b0: No effect 1'b1: Block align control is asserted during Configuration state	**1'b1**
0x5D0	vesc_reg50[11]	**cb_blk_align_assert_during_l0s** 1'b0: No effect 1'b1: Block align control is asserted during L0sRx state	**1'b1**
0x5D0	vesc_reg50[12]	**cb_reset_lane_reverse_l0srx_to_recov_en** 1'b0: No effect 1'b1: Reset Valid in Lane Reversal block on transition from L0sRx to Recovery	1'b0
0x5D0	vesc_reg50[13]	**cb_reset_lane_reverse_recov_en** 1'b0: No effect 1'b1: Reset Valid in Lane Reversal block on entry to Recovery	1'b0
0x5D0	vesc_reg50[14]	**cb_sds_easy_detection** 1'b0: No effect 1'b1: Enable easier detection of SDS (without start/end DW)	**1'b1**
0x5D0	vesc_reg50[15]	**cb_mask_frame_for_descranbler** 1'b0: No effect 1'b1: Mask Framing error for descrambler (DFT)	1'b0

Table 79. VESC_REG 50: (Offset D0h): General configuration register

Offset	Bits	Description	Value
0x5D0	vesc_reg50[16]	**cb_mask_frame_error_in_recov_idle** 1’b0: No effect 1’b1: Mask Framing error in recovery idle (for descrambler)	1'b0
0x5D0	vesc_reg50[17]	**cb_clr_data_strm_valid_upon_frame_err_en** 1’b0: No effect 1’b1:Frame Error clears Data Stream Valid flag	1'b0
0x5D0	vesc_reg50[18]	**cb_clr_data_stream_valid_upon_bad_sync_hdr** 1’b0: No effect 1’b1:Bad Sync header clears Data Stream Valid flag	1'b0
0x5D0	vesc_reg50[19]	**cb_set_data_stream_valid_upon_sds_en** 1’b0: No effect 1’b1: SDS set the Data Stream Valid	1'b0/ **1’b1**
0x5D0	vesc_reg50[20]	**cb_set_data_stream_valid_upon_sds_after_err_dis** 1’b0: Setting Data Stream Valid is upon SDS if there was error 1’b1: Setting Data Stream Valid is upon SDS (This bit effects only if bit 19 is set)	1'b0/ **1’b1**
0x5D0	vesc_reg50[23:21]	**cb_reduce_post_fc_credits** Controls the Post Hdr FC credit reduction 3’d0 – Default value 3’d1 – Default value -4 3’d2 – Default value divided by 2 3’d3 – Default value divided by 2 plus 2 3’d4 – Default value divided by 2 minus 2 3’d5 – 8 credits 3’d6 – 6 credits 3’d7 – 4 credits	2'b0
0x5D0	vesc_reg50[24]	**cb_ignore_recovery_for_clk_req** 1’b0**:** port considered not idle if its LTSSM is in Recovery 1’b1: port considered idle if its LTSSM is in Recovery	1'b0
0x5D0	vesc_reg50[25]	**cb_mask_ts_detection_during_rx_ei_dis** 1’b0**:** TS detection is masked with Rx EI 1’b1:TS detection is not masked with Rx EI (minor bug)	1'b0

Table 79. VESC_REG 50: (Offset D0h): General configuration register

Offset	Bits	Description	Value
0x5D0	vesc_reg50[26]	**cb_dont_perform_eq_if_optimal_dis** 1'b0**:** Equalization is not triggered in Recovery entry if Equalization was done once well 1'b1: Equalization is triggered in Recovery entry even if Equalization was done once well	1'b0
0x5D0	vesc_reg50[27]	**cb_perform_eq_only_from_non_gen3_dis** 1'b0 **–** Equalization is triggered in Recovery entry only if rate is not Gen3 and the target link speed is Gen3 1'b1 **–** Equalization is triggered in Recovery entry if the target link speed is Gen3 (no matter if it comes from Gen3)	1'b0
0x5D0	vesc_reg50[28]	**cb_invert_start_equalization_w_preset** 1'b0: no change 1'b1: (Bug)	1'b0
0x5D0	vesc_reg50[29]	**cb_l0s_to_l0_without_skp_sds_en** 1'b0**:** No effect 1'b1: Enable to exit from L0sRx to L0 without SKP / SDS	1'b0
0x5D0	vesc_reg50[30]	**cb_recov_cfg_gen2_deemp_update_en** 1'b0: No effect 1'b1: Port updates de-emphasis for Gen2 in Recoevery.Cfg	1'b0**/1'b1** (Dn = 1) (Up = 0)
0x5D0	vesc_reg50[31]	**cb_recov_cfg_gen2_deemp_value** 1'b0: No effect 1'b1: Option to set value of -3.5dB while Port goes to Gen2 (Relevant if bit 30 is set)	1'b0

Table 80. VESC_REG 51: (Offset D4h): General configuration register

Offset	Bits	Description	Value
0x5D4	vesc_reg51[0]	**cb_recovery_lock_to_cfg_force** 1'b0: No effect 1'b1: Force recovery lock to cfg transition condition (DFT)	1'b0
0x5D4	vesc_reg51[1]	**cb_recovery_cfg_to_idle_force** 1'b0: No effect 1'b1: Force recovery cfg to idle transition condition (DFT)	1'b0

Table 80. VESC_REG 51: (Offset D4h): General configuration register

Offset	Bits	Description	Value
0x5D4	vesc_reg51[2]	**cb_recovery_got_idle_force** 1’b0: No effect 1’b1: Force got idle condition in recovery (DFT)	1'b0
0x5D4	vesc_reg51[3]	**cb_configuration_got_idle_force** 1’b0: No effect 1’b1: Force got idle condition in configuration (DFT)	1'b0
0x5D4	vesc_reg51[4]	**cb_recov_lock_to_detect_timeout_cancel** 1’b0: No effect 1’b1: Mask timeout exp for recovery lock to detect (DFT)	1'b0
0x5D4	vesc_reg51[5]	**cb_recov_cfg_to_detect_timeout_cancel** 1’b0: No effect 1’b1: Mask timeout exp for recovery cfg to detect (DFT)	1'b0
0x5D4	vesc_reg51[6]	**cb_recov_idle_to_detect_timeout_cancel** 1’b0: No effect 1’b1: Mask timeout exp for recovery idle to detect (DFT)	1'b0
0x5D4	vesc_reg51[7]	**cb_cfg_lane_num_to_detect_timeout_cancel** 1’b0: No effect 1’b1: Mask timeout exp for configuration lane num accept to detect (DFT)	1'b0
0x5D4	vesc_reg51[8]	**cb_cfg_complete_to_detect_timeout_cancel** 1’b0: No effect 1’b1: Mask timeout exp for configuration complete to detect (DFT)	1'b0
0x5D4	vesc_reg51[9]	**cb_cfg_idle_num_to_detect_timeout_cancel** 1’b0: No effect 1’b1: Mask timeout exp for configuration idle to detect (DFT)	1'b0
0x5D4	vesc_reg51[10]	**Mask Lane error status** 1’b0: No effect 1’b1: Mask lane error status in PCIE Secondary Capability (DFT)	1'b0
0x5D4	vesc_reg51[11]	**Mask Receiver error status** 1’b0: No effect 1’b1: Mask receiver error status in Advanced Error Reporting Capability (DFT)	1'b0

Table 80. VESC_REG 51: (Offset D4h): General configuration register

Offset	Bits	Description	Value
0x5D4	vesc_reg51[12]	**cb_force_rcvr_detected_according_to_xmode** 1'b0: No effect 1'b1: Rx Detection successful indication is forced.	1'b0
0x5D4	vesc_reg51[13]	**cb_reset_eios_det_on_pol_com_exit** 1'b0: No effect 1'b1: Reset EIOS detection upon exit from Polling Compliance	1'b0
0x5D4	vesc_reg51[14]	**cb_stay_in_p0_during_link_dis** 1'b0: During Link Disable PHY is directed to P1 (Spec) 1'b1: During Link Disable PHY is directed to stay in P0	1'b0
0x5D4	vesc_reg51[15]	**cb_dft_force_ts_detect** 1'b0: No effect 1'b0: DFT option to force TS detection	1'b0
0x5D4	vesc_reg51[16]	**cb_dft_force_enter_ei** 1'b0: No effect 1'b0: DFT option to force Tx EI entry	1'b0
0x5D4	vesc_reg51[17]	**cb_dft_force_idle_detect** 1'b0: No effect 1'b0: DFT option to force IDLE detection	1'b0
0x5D4	vesc_reg51[18]	**cb_dft_force_eios_detect** 1'b0: No effect 1'b0: DFT option to force EIOS detection	1'b0
0x5D4	vesc_reg51[19]	**cb_dft_force_exit_l1** 1'b0: No effect 1'b0: DFT option to force exit L1	1'b0
0x5D4	vesc_reg51[23:20]	**cb_gen3_preset_coeff_ctrl** Control of the coefficients in Preset table	4'h0
0x5D4	vesc_reg51[24]	**Force pipe rate signal** 1'b0: No Effect 1'b1: pipe rate is overwritten by bits [26:25]	1'b0
0x5D4	vesc_reg51[26:25]	**Pipe Rate force value** Value that is forced if bit 24 is set	2'h0
0x5D4	vesc_reg51[27]	**Force power dowm signal** 1'b0: No Effect 1'b1: power down is overwritten by bits [29:28]	1'b0

Table 80. VESC_REG 51: (Offset D4h): General configuration register

Offset	Bits	Description	Value
0x5D4	vesc_reg51[29:28]	**Power Down force value** Value that is forced if bit 27 is set	2'h0
0x5D4	vesc_reg51[30]	**Force Tx Electrical Idle** 1'b0: No Effect 1'b1: Tx Electrical Idle is overwritten by bits [31]	1'b0
0x5D4	vesc_reg51[31]	**Tx Electrical Idle force value** Value that is forced if bit 24 is set	1'h0

Table 81. VESC_REG 52: (Offset D8h): General configuration register

Offset	Bits	Description	Value
0x5D8	vesc_reg52[0]	**update_sel_deemph_variable_vesc** 1'b0: No Effect 1'b1: Option to update / force de-emphasis for Gen2	1'b0
0x5D8	vesc_reg52[1]	**update_sel_deemph_variable_value_vesc** 1'b0: No Effect 1'b1: Value of de-emphasis that can be loaded	1'b0
0x5D8	vesc_reg52[2]	**cb_dnport_equal_phase23_skip** 1'b0: No Effect 1'b1: Dn Ports skips Equalization Phase 2 and 3	1'b0 / **1'b1**
0x5D8	vesc_reg52[3]	**cb_ei_infer_en_for_loop** 1'b0: No Effect 1'b1: Enable the EI infer condition for Loopback Slave	1'b0
0x5D8	vesc_reg52[4]	**cb_gen1_exit_from_loop_fix_dis** 1'b0: Exit from Gen1 Loopback fix is enabled 1'b1: Exit from Gen1 Loopback fix is disabled	1'b0
0x5D8	vesc_reg52[5]	**cb_loop_target_rate_fix_dis** 1'b0: Loopback target rate fix is enabled 1'b1: Loopback target rate fix is disabled	1'b0
0x5D8	vesc_reg52[6]	**cb_loop_entry_to_active_slave_fix_dis** 1'b0: In Gen3 Loopback FSM waits for 2TS1 with loopback bit 1'b1: Fix is disabled (FSM doesn't wait for 2 TS1 indication)	1'b0

Table 81. VESC_REG 52: (Offset D8h): General configuration register

Offset	Bits	Description	Value
0x5D8	vesc_reg52[7]	**cb_gen2_loop_slave_deemp_fix_dis** 1'b0: Fix to update Gen2 de-emphasis in loopback is enabled 1'b1: Fix to update Gen2 de-emphasis in loopback is disabled	1'b0
0x5D8	vesc_reg52[8]	**cb_gen2_loop_slave_deemp_value** 1'b0: No Effect 1'b1: Option to force -3.5 dB de-emphasis value in loopback	1'b0
0x5D8	vesc_reg52[9]	**cb_update_deemph_pol_sel** 1'b0: Update of Gen2 de-emphasis is done from TS2 1'b1: Update of Gen2 de-emphasis is done from TS1 (fix) (Relevant to Polling state update)	**1'b1**
0x5D8	vesc_reg52[10]	**cb_update_deemph_recov_sel** 1'b0: Update of Gen2 de-emphasis is done from TS2 1'b1: Update of Gen2 de-emphasis is done from TS1 (fix) (Relevant to Recovery state update)	**1'b1**
0x5D8	vesc_reg52[11]	**cb_update_deemph_cfg_to_loop_en** 1'b0: No effect 1'b1: Enables update of Gen2 de-emphasis update during the transition from Configuration to Loopback state	**1'b1**
0x5D8	vesc_reg52[12]	**cb_update_deemph_recov_to_loop_en** 1'b0: No effect 1'b1: Enables update of Gen2 de-emphasis update during the transition from Recovery to Loopback state	**1'b1**
0x5D8	vesc_reg52[13]	**cb_stp_align_dllp_detect_x1_dis2** 1'b0: Additional Fix to ignore DLLP it STP Alignment block in order not to indicate false Framing Errors in x1 mode 1'b1: Fix is disabled	1'b0
0x5D8	vesc_reg52[14]	**cb_stp_align_dllp_detect_x2_dis2** 1'b0: Additional Fix to ignore DLLP it STP Alignment block in order not to indicate false Framing Errors in x2 mode 1'b1: Fix is disabled	1'b0

Table 81. VESC_REG 52: (Offset D8h): General configuration register

Offset	Bits	Description	Value
0x5D8	vesc_reg52[15]	**cb_stp_align_dllp_detect_x4_dis2** 1'b0: Additional Fix to ignore DLLP it STP Alignment block in order not to indicate false Framing Errors in x4 mode 1'b1: Fix is disabled	1'b0
0x5D8	vesc_reg52[16]	**cb_consider_polling_like_detect_for_l1_l2_fix_dis** 1'b0: For L1/L2 entry consider Polling like Detect 1'b1: Fix is disabled	1'b0
0x5D8	vesc_reg52[17]	**cb_gen3_loop_entry_con_ts_sel** 1'b0: Check 2 TS on all lanes in gen3 entry slave 1'b1: Check 2 TS on any lane in gen3 entry slave	1'b0
0x5D8	vesc_reg52[18]	**cb_gen3_loop_entry_con_ts_sel** 1'b0: No effect 1'b1: Enables to capture de-emphasis request from TS2 for Loopback in Gen2	1'b0
0x5D8	vesc_reg52[19]	**cb_force_TC_VC0_map_to_ff** 1'b0: No effect 1'b1: Forces TC to VC0 map to FF internally (if custom VC mode is enabled)	1'b0 / **1'b1**
0x5D8	vesc_reg52[20]	**cb_l1_accept_credit_update_fix_dis** 1'b0: Dn Port doesn't accept L1 till credits are returned 1'b1: Dn Port doesn't check credit returned in L1 ASPM FSM	1'b0
0x5D8	vesc_reg52[21]	**cb_auto_rate_change_accepted_in_detect_en** 1'b0: No effect 1'b1: Rate Change to Gen1 in Detect is not gated by PHY Status	1'b0
0x5D8	vesc_reg52[22]	**cb_memrd_credit_pending_fix_en** 1'b0: No effect 1'b1: MemRd credit Pending is added to MemWr flag (used for L1PrepASPM FSM on entry to L1)	1'b0 / **1'b1** (Sim - rand)
0x5D8	vesc_reg52[23]	**cb_not_tlp_mask_frame_error_x1_fix_dis** 1'b0: Prevent false Frame Error before TLP in x1 mode 1'b1: Fix is disabled	1'b0

Table 81. VESC_REG 52: (Offset D8h): General configuration register

Offset	Bits	Description	Value
0x5D8	vesc_reg52[24]	**cb_not_tlp_mask_frame_error_x2_fix_dis** 1'b0: Prevent false Frame Error before TLP in x2 mode 1'b1: Fix is disabled	1'b0
0x5D8	vesc_reg52[25]	**cb_not_tlp_mask_frame_error_x4_fix_dis** 1'b0: Prevent false Frame Error before TLP in x4 mode 1'b1: Fix is disabled	1'b0
0x5D8	vesc_reg52[26]	**cb_not_dllp_mask_frame_error_x1_fix_dis** 1'b0: Prevent false Frame Error before DLLP in x1 mode 1'b1: Fix is disabled	1'b0
0x5D8	vesc_reg52[27]	**cb_not_dllp_mask_frame_error_x2_fix_dis** 1'b0: Prevent false Frame Error before DLLP in x2 mode 1'b1: Fix is disabled	1'b0
0x5D8	vesc_reg52[28]	**cb_not_dllp_mask_frame_error_x4_fix_dis** 1'b0: Prevent false Frame Error before DLLP in x4 mode 1'b1: Fix is disabled	1'b0
0x5D8	vesc_reg52[29]	**cb_not_dllp_mask_frame_error_x4_fix_dis** 1'b0: fix to delay init dllp during entry to L0 1'b1: Disable the fix	1'b0
0x5D8	vesc_reg52[30]	**cb_consider_polling_like_detect_for_l2_exit_fix_dis** 1'b0: For L2 Aux HSM exit consider Polling like Detect 1'b1: Fix is disabled	1'b0
0x5D8	vesc_reg52[31]	**cb_gen3_hot_reset_change_en** 1'b0: No effect 1'b1: Gen3 change for Hot Reset (not required)	1'b0

Table 82. VESC_REG 53: (Offset DCh): General configuration register

Offset	Bits	Description	Value
0x5DC	vesc_reg53[0]	cb_init_fc_dllp_capture_fix_dis_vc0	1'b0
0x5DC	vesc_reg53[1]	cb_init_fc_dllp_fc1_flag_stretch_vc0	1'b0
0x5DC	vesc_reg53[2]	cb_init_fc_dllp_capture_fix_dis_vc1	1'b0
0x5DC	vesc_reg53[3]	cb_init_fc_dllp_fc1_flag_stretch_vc1	1'b0
0x5DC	vesc_reg53[4]	cb_loopback_slave_infer_fix_dis	1'b0
0x5DC	vesc_reg53[5]	cb_loopback_slave_exit_upon_rx_ei_fix_dis	1'b0
0x5DC	vesc_reg53[6]	cb_non_gen1_exit_from_loopback_upon_eios_en	1'b0
0x5DC	vesc_reg53[7]	**cb_l2_entry_fix_dis** 1'b0: Fix to wait empty Retry Buffer and Ack FIFO before sending enter L2 request DLLPs 1'b1: Fix is disabled	1'b0

Table 82. VESC_REG 53: (Offset DCh): General configuration register

Offset	Bits	Description	Value
0x5DC	vesc_reg53[8]	**cb_l2_entry_time_sel** Selects time between all Acked TLP to L2 entry request 1'b0: 15 cycles 1'b1: 255 cycles	1'b0
0x5DC	vesc_reg53[9]	**cb_reset_eieos_request** 1'b0: No effect 1'b1: Port requests to reset EIEOS during Equalization	1'b0
0x5DC	vesc_reg53[10]	**cb_prevent_l0srx_due_to_l2_fix_dis**	1'b0
0x5DC	vesc_reg53[11]	**cb_pm_aux_access_fix_dis** 1'b0: Doesn't allow to access PMCSR from Host Interface 1'b1: Allow to access PMCSR from Host Interface	1'b0
0x5DC	vesc_reg53[12]	**cb_rx_fc_queue_post_flush_dis_vc0** 1'b0: Fix to Flush Post Rx Queue when Link is down (VC0) 1'b1: Fix is disabled	1'b0
0x5DC	vesc_reg53[13]	**cb_rx_fc_ queue_post_flush_dis_vc1** 1'b0: Fix to Flush Post Rx Queue when Link is down (VC1) 1'b1: Fix is disabled	1'b0
0x5DC	vesc_reg53[14]	**cb_rx_fc_ queue_comp_flush_dis_vc0** 1'b0: Fix to Flush Post Rx Queue when Link is down (VC0) 1'b1: Fix is disabled	1'b0
0x5DC	vesc_reg53[15]	**cb_rx_fc_ queue_comp_flush_dis_vc1** 1'b0: Fix to Flush Post Rx Queue when Link is down (VC1) 1'b1: Fix is disabled	1'b0
0x5DC	vesc_reg53[16]	**cb_chan1_long_tlp_fix_dis** 1'b0: Fix to give dummy grant with delay for long TLPs (chan1) 1'b1: Fix is disabled	1'b0
0x5DC	vesc_reg53[17]	**cb_chan2_long_tlp_fix_dis** 1'b0: Fix to give dummy grant with delay for long TLPs (chan1) 1'b1: Fix is disabled	1'b0
0x5DC	vesc_reg53[18]	**cb_comp_queue_data_valid_fix_dis_vc0** 1'b0: Fix to leave Data Valid zero when not data (VC0) 1'b1: Fix is disabled	1'b0

Table 82. VESC_REG 53: (Offset DCh): General configuration register

Offset	Bits	Description	Value
0x5DC	vesc_reg53[19]	**cb_comp_queue_data_valid_fix_dis_vc1** 1'b0: Fix to leave Data Valid zero when not data (VC1) 1'b1: Fix is disabled	1'b0
0x5DC	vesc_reg53[20]	**cb_memrd_moderation_p2p_count_en_vc0** 1'b0: P2P MemRd moderation is disabled (VC0) 1'b1: P2P MemRd moderation is enabled (VC0) Bit is for Downstream Port (Reserved in Up/EP ports)	1'b0 (Dn)
0x5DC	vesc_reg53[21]	**cb_memrd_moderation_p2p_count_en_vc1** 1'b0: P2P MemRd moderation is disabled (VC1) 1'b1: P2P MemRd moderation is enabled (VC1) Bit is for Downstream Port (Reserved in Up/EP ports)	1'b0 (Dn)
0x5DC	vesc_reg53[22]	**cb_memrd_moderation_count_io_read_dis_vc0** 1'b0: I/O Rd moderation is enabled (VC0) 1'b1: I/O Rd moderation is disabled (VC0) Bit is for Downstream Port (Reserved in Up/EP ports)	1'b0 (Dn)
0x5DC	vesc_reg53[23]	**cb_memrd_moderation_count_io_read_dis_vc1** 1'b0: I/O Rd moderation is enabled (VC1) 1'b1: I/O Rd moderation is disabled (VC1) Bit is for Downstream Port (Reserved in Up/EP ports)	1'b0 (Dn)
0x5DC	vesc_reg53[24]	**cb_memrd_moderation_count_memrd_lock_dis_vc0** 1'b0: MemRd Lock moderation is enabled (VC0) 1'b1: MemRd Lock moderation is disabled (VC0) Bit is for Downstream Port (Reserved in Up/EP ports)	1'b0 (Dn)
0x5DC	vesc_reg53[25]	**cb_memrd_moderation_count_memrd_lock_dis_vc1** 1'b0: MemRd Lock moderation is enabled (VC1) 1'b1: MemRd Lock moderation is disabled (VC1) Bit is for Downstream Port (Reserved in Up/EP ports)	1'b0 (Dn)
0x5DC	vesc_reg53[31:26]	Reserved	0

Table 83. VESC_REG 54 (Offset 'hE0): General configuration register

Offset	Bits	Description	Value
0x5E0	vesc_reg54[0]	**cb_l1aspm_fsm_rst_end_recov** 1'b0: Fix to reset L1 ASPM at the end of Recovery 1'b1: Fix is disabled	1'b0

Table 83. VESC_REG 54 (Offset 'hE0): General configuration register

Offset	Bits	Description	Value
0x5E0	vesc_reg54[1]	**cb_l1soft_fsm_rst_end_recov** 1'b0: Fix to reset L1 Soft at the end of Recovery 1'b1: Fix is disabled	1'b0
0x5E0	vesc_reg54[2]	**cb_l1aspm_fsm_rst_no_eios** 1'b0: No effect 1'b1: Fix to reset L1 ASPM if eios is not received	1'b0
0x5E0	vesc_reg54[3]	**cb_l1soft_fsm_rst_no_eios** 1'b0: No effect 1'b1: Fix to reset L1 Soft if eios is not received	1'b0
0x5E0	vesc_reg54[4]	**cb_up_link_down_dn_hot_reset_fix_dis** 1'b0: Link Down of Upstream Port causes Dn Hot Reset 1'b1: Fix is disabled	1'b0
0x5E0	vesc_reg54[5]	**cb_rcvr_detect_extra_cycle_en** 1'b0: No effect 1'b1: Enable Extra cycle check for Receiver Detection	1'b0
0x5E0	vesc_reg54[7:6]	**cb_less_periodic_fc_update_sel** 2'b00 – 30us (default) 2'b01 – 500us 2'b10 – 1ms 2'b11 – 2ms	2'h0
0x5E0	vesc_reg54[8]	**cb_less_periodic_fc_update** 1'b0: No effect 1'b1: Enables constantly to send much less FC updates according to bits [7:6]	1'b0
0x5E0	vesc_reg54[9]	**cb_stop_replay_timer_upon_credit_en** 1'b0: No effect 1'b1: Enables to stop Replay Timer upon indication of credits	1'b0
0x5E0	vesc_reg54[11:10]	**cb_stop_replay_timer_set_sel** Selects the time of no credits to stop Replay Timer	2'h0
0x5E0	vesc_reg54[12]	**cb_ack_nak_timer_en** 1'b0: ACK/NAK Timer is not used (legacy) 1'b1: Enable the use of ACK/NAK Timer	1'b0

Table 83. VESC_REG 54 (Offset 'hE0): General configuration register

Offset	Bits	Description	Value
0x5E0	vesc_reg54[14:13]	**cb_ack_nak_timer_limit_sel** Selects different limit for ACK/NAK Timer Limit 2'd0 – Spec Values 2'd1 – Lower Values than Spec 2'd2 – Higher Values than Spec 2'd3 – Much Higher Values than Spec	2'b00
0x5E0	vesc_reg54[15]	**cb_gen12_eios_detect_fix_did** 1'b0: Fix to add RxValid bit when detecting EIOS 1'b1: Fix is disabled	1'b0
0x5E0	vesc_reg54[16]	**cb_l1_exit_without_presence_fix_dis** 1'b0: Fix to exit L1 if presence is not asserted 1'b1: Fix is disabled	1'b0
0x5E0	vesc_reg54[17]	**cb_exit_rx_ei_sel_any_all** 1'b0: Rx EI condition check "all lanes" 1'b1: Rx EI condition check "any lane"	1'b0
0x5E0	vesc_reg54[18]	**cb_extra_rd_req_grant_fix_dis** 1'b0: Fix to prevent extra read grant in case Completion Queue Slots are not available 1'b1: Fix is disabled (Bug) The fix is active in EMEP port only	1'b0 (EP)
0x5E0	vesc_reg54[19]	**cb_nak_b2b_after_ack_missed_fix_dis** 1'b0 : Fix to remember NAK that came b2b after two Acks 1'b1 : Fix is disabled	1'b0
0x5E0	vesc_reg54[20]	**cb_tlp_address_start_to_ack_fifo_fix_dis** 1'b0 : Fix to delay TLP address start write to ack FIFO 1'b1 : Fix is disabled	1'b0
0x5E0	vesc_reg54[21]	**cb_chan0_add_ipg_if_other_active_fix_dis** 1'b0: Adding extra cycle in grant if other channel pending 1'b1: Fix is disabled	1'b0

Table 83. VESC_REG 54 (Offset 'hE0): General configuration register

Offset	Bits	Description	Value
0x5E0	vesc_reg54[22]	**cb_chan1_add_ipg_if_other_active_fix_dis** 1’b0: Adding extra cycle in grant if other channel pending 1’b1: Fix is disabled	1'b0
0x5E0	vesc_reg54[23]	**cb_chan2_add_ipg_if_other_active_fix_dis** 1’b0: Adding extra cycle in grant if other channel pending 1’b1: Fix is disabled	1'b0
0x5E0	vesc_reg54[24]	**cb_chan3_add_ipg_if_other_active_fix_dis** 1’b0: Adding extra cycle in grant if other channel pending 1’b1: Fix is disabled	1'b0
0x5E0	vesc_reg54[25]	**cb_chan4_add_ipg_if_other_active_fix_dis** 1’b0: Adding extra cycle in grant if other channel pending 1’b1: Fix is disabled	1'b0
0x5E0	vesc_reg54[26]	**cb_chan5_add_ipg_if_other_active_fix_dis** 1’b0: Adding extra cycle in grant if other channel pending 1’b1: Fix is disabled	1'b0
0x5E0	vesc_reg54[27]	**cb_pm_dllp_req_sel** 1’b0: Fix to have gap on cycle between PM request for better timing of the signal sync 1’b1: Fix is disabled	1'b0
0x5E0	vesc_reg54[28]	**cb_clr_direct_to_recov_flag_fix_dis** 1’b0: Fix to clear the directed to recovery flag upon entry to Recovery state 1’b1: Fix is disabled (might cause redundant Recovery)	1'b0
0x5E0	vesc_reg54[29]	**cb_set_dir_speed_change_l0_fix_dis** 1’b0: Fix to set speed change flag (from L0) 1’b1: Fix is disabled	1'b0
0x5E0	vesc_reg54[30]	**cb_set_dir_speed_change_l1_fix_dis** 1’b0: Fix to set speed change flag (from L1) 1’b1: Fix is disabled	1'b0

Table 83. VESC_REG 54 (Offset 'hE0): General configuration register

Offset	Bits	Description	Value
0x5E0	vesc_reg54[31]	**cb_l2_custom_time_strobe_sel** 1'b0: L2 Custom Timers value is in 4 us units (max 1 ms) 1'b1: L2 Custom Timers value is in us units (max 256 us)	1'b0

Table 84. VESC_REG 55 (Offset 'hE4): General configuration register

Offset	Bits	Description	Value
0x5E4	vesc_reg55[0]	**cb_nph_credit_avail_margin_en** 1'b0: Fix to save one credit margin on User interface (NPH) 1'b1: Fix is disabled	1'b0
0x5E4	vesc_reg55[1]	**cb_npd_credit_avail_margin_en** 1'b0: Fix to save one credit margin on User interface (NPD) 1'b1: Fix is disabled	1'b0
0x5E4	vesc_reg55[2]	**cb_ph_credit_avail_margin_en** 1'b0: Fix to save one credit margin on User interface (PH) 1'b1: Fix is disabled	1'b0
0x5E4	vesc_reg55[3]	**cb_npd_credit_avail_margin_en** 1'b0: Fix to save one credit margin on User interface (PD) 1'b1: Fix is disabled	1'b0
0x5E4	vesc_reg55[4]	**cb_cplh_credit_avail_margin_en** 1'b0: Fix to save one credit margin on User interface (CPLH) 1'b1: Fix is disabled	1'b0
0x5E4	vesc_reg55[5]	**cb_cpld_credit_avail_margin_en** 1'b0: Fix to save one credit margin on User interface (CPLD) 1'b1: Fix is disabled	1'b0
0x5E4	vesc_reg55[6]	**cb_pme_status_load_fix_dis** 1'b0: Fix to load PME Status also on falling edge 1'b1: Fix is disabled (Reserved in Up/Dn and used in XHC EMEP)	1'b0 (XHC EP)

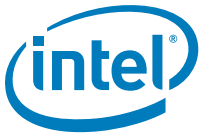


Table 84. VESC_REG 55 (Offset 'hE4): General configuration register

Offset	Bits	Description	Value
0x5E4	vesc_reg55[7]	**cb_d3_to_d0_reset_time_fix_en** 1'b0: Fix to allow a longer D3 to D0 Reset 1'b1: Fix is disabled (The fix is needed only in XHC EMEP to load back PMCSR)	1'b0 (XHC EP)
0x5E4	vesc_reg55[8]	**cb_pme_status_load_fix_en** 1'b0: No Effect 1'b1: Fix to load PME Status also on falling edge (Reserved in Up/Dn and used in XHC EMEP)	1'b0 (XHC EP)
0x5E4	vesc_reg55[9]	**cb_pme_enable_load_fix_en** 1'b0: No Effect 1'b1: Fix to load PME Enable on falling edge (Reserved in Up/Dn and used in XHC EMEP)	1'b0 (XHC EP)
0x5E4	vesc_reg55[10]	**cb_pme_d_state_load_fix_en** 1'b0: No Effect 1'b1: Fix to load D state on a change (Reserved in Up/Dn and used in XHC EMEP)	1'b0 (XHC EP)
0x5E4	vesc_reg55[11]	**cb_slow_clk_us_period_fix_dis** 1'b0: Fix to count accurate us tick on slow clock (100MHz) 1'b1: Without fix us tick is 1280 ns	1'b0
0x5E4	vesc_reg55[12]	**cb_req0_two_cycles_fc_credit_check_en** 1'b0: Port give grant if credit available for one cycle 1'b1: Port give grant if credit available for two cycle	**1'b1**
0x5E4	vesc_reg55[13]	**cb_req1_two_cycles_fc_credit_check_en** 1'b0: Port give grant if credit available for one cycle 1'b1: Port give grant if credit available for two cycle	**1'b1**
0x5E4	vesc_reg55[14]	**cb_req2_two_cycles_fc_credit_check_en** 1'b0: Port give grant if credit available for one cycle 1'b1: Port give grant if credit available for two cycle	**1'b1**
0x5E4	vesc_reg55[15]	**cb_req3_two_cycles_fc_credit_check_en** 1'b0: Port give grant if credit available for one cycle 1'b1: Port give grant if credit available for two cycle	**1'b1**

Table 84. VESC_REG 55 (Offset 'hE4): General configuration register

Offset	Bits	Description	Value
0x5E4	vesc_reg55[16]	**cb_req4_two_cycles_fc_credit_check_en** 1'b0: Port give grant if credit available for one cycle 1'b1: Port give grant if credit available for two cycle	**1'b1**
0x5E4	vesc_reg55[17]	**cb_req5_two_cycles_fc_credit_check_en** 1'b0: Port give grant if credit available for one cycle 1'b1: Port give grant if credit available for two cycle	**1'b1**
0x5E4	vesc_reg55[18]	**cb_req0_fc_avail_indication_early_dis** 1'b0: Port check credit available early indication 1'b1: Port check credit available sampled indication (Canceled due to timing issue)	1'b0
0x5E4	vesc_reg55[19]	**cb_req1_fc_avail_indication_early_dis** 1'b0: Port check credit available early indication 1'b1: Port check credit available sampled indication (Canceled due to timing issue)	1'b0
0x5E4	vesc_reg55[20]	**cb_req2_fc_avail_indication_early_dis** 1'b0: Port check credit available early indication 1'b1: Port check credit available sampled indication (Canceled due to timing issue)	1'b0
0x5E4	vesc_reg55[21]	**cb_req3_fc_avail_indication_early_dis** 1'b0: Port check credit available early indication 1'b1: Port check credit available sampled indication (Canceled due to timing issue)	1'b0
0x5E4	vesc_reg55[22]	**cb_req4_fc_avail_indication_early_dis** 1'b0: Port check credit available early indication 1'b1: Port check credit available sampled indication (Canceled due to timing issue)	1'b0
0x5E4	vesc_reg55[23]	**cb_req5_fc_avail_indication_early_dis** 1'b0: Port check credit available early indication 1'b1: Port check credit available sampled indication (Canceled due to timing issue)	1'b0
0x5E4	vesc_reg55[24]	**cb_stop_tx_delay_sel** 1'b0: StopTx is sampled by double sync on PCLK Clock (pipe). 1'b1: StopTx is sampled by one FF on PCLK Clock (pipe).	1'b0

Table 84. VESC_REG 55 (Offset 'hE4): General configuration register

Offset	Bits	Description	Value
0x5E4	vesc_reg55[25]	**cb_master_start_from_slave_value** 1'b0: During EQ Master starts from predefined coeffs 1'b1: During EQ Master starts from partner coeffs	1'b0
0x5E4	vesc_reg55[26]	**cb_reset_cgf_upon_link_down_sel** 1'b0: UP/EP clears its Cfg space upon Link Down 1'b1: UP/EP doesn't clear its Cfg space upon Link Down Used only in EP or Upstream Port	1'b0
0x5E4	vesc_reg55[26]	**cb_reset_cgf_upon_d3_to_d0_sel** 1'b0: UP/EP clears its Cfg space upon D3 to D0 DN doesn't clear its Cfg Space upon D3 to D0 1'b1: DN clears its Cfg space upon D3 to D0 UP/EP doesn't clear its Cfg Space upon D3 to D0 (This is under condition NSR = 0)	1'b0
0x5E4	vesc_reg55[30:28]	**force_rx_preset_hint_from_vesc** Value of Rx Preset Hit to force	3'h0
0x5E4	vesc_reg55[31]	**cb_force_rx_preset_hint** 1'b0: No effect 1'b1: Option to force Rx Preset Hint from [30:28]	1'b0

Table 85. VESC_REG 56 (Offset 'hE8): General configuration register (changes for ICL)

Offset	Bits	Description	Value
0x5E8	vesc_reg56[1:0]	**cb_wait_after_nak_timer_value_sel** Upstream Component: Selector for the wait time after L1 NAK was sent, before looking on requests Downstream Component: Selector for the wait time after L1 NAK was received, before new request 2'b00 – 15us 2'b01 – 20us 2'b02 – 25us 2'b03 – 30us	2'h0 (CIO Dn – 2'b01) (CIO Up – 2'b11)

Table 85. VESC_REG 56 (Offset 'hE8): General configuration register (changes for ICL)

Offset	Bits	Description	Value
0x5E8	vesc_reg56[3:2]	**cb_longer_wait_time_before_l1_sel** Selector for the idle time before entry to L1. If L0sTx is enabled the only valid value is 2'b00. 2'b00 – vesc_reg1[7:6] – (8,12,16,20us) 2'b01 – 50us 2'b02 – 60us 2'b03 – 70us	2'h0
0x5E8	vesc_reg56[4]	**cb_l1_eios_wait_time_en** 1'b0: Short wait for EIOS 1'b1: Enables a longer wait time for EIOS for Downstream Component (time controlled by bits [6:5])	1'b0
0x5E8	vesc_reg56[6:5]	**cb_l1_eios_wait_time_sel** Configures a wait time for EIOS 2'b00 – 5us 2'b01 – 7us 2'b02 – 9us 2'b03 – 11us (Intended to be used over tunnel for Upstream Port)	2'h0
0x5E8	vesc_reg56[7]	**cb_l1_eios_wait_time_sel** The following bit is used only if Port is configured to wait for EIOS before entry to L1 with a counter 1'b0: After waiting for EIOS before entry to L1 and not getting	1'b0
0x5E8	vesc_reg56[8]	**cb_eios_detect_l1seq_to_l1prep_en** 1'b0: No effect 1'b1: Enables EIOS detected indication from L1Seq to L1Prep	1'b0
0x5E8	vesc_reg56[9]	**cb_rst_l1_entry_timer_upon_pm_req_nak** 1'b0: Upon getting PM Req NAK port doesn't reset L1 entry counter (request will be after NAK timer [1:0]) 1'b1: 1'b0: Upon getting PM Req NAK port resets L1 entry counter (Request will be after L1 Idle entry timer [3:2])	1'b0

Table 85. VESC_REG 56 (Offset 'hE8): General configuration register (changes for ICL)

Offset	Bits	Description	Value
0x5E8	vesc_reg56[10]	**cb_fc_update_period_sel** 1'b0: 40 us (a bit more than in Spec) 1'b1: 30 us (Max Spec value)	1'b0
0x5E8	vesc_reg56[11]	**cb_after_l1_nak_wait_ful_idle_time** 1'b0: After Ports gets L1 NAK it waits - vesc_reg56[1:0] time 1'b1: After Ports gets L1 NAK it waits - vesc_reg56[3:2] time	1'b0
0x5E8	vesc_reg56[31:12]	Reserved	0

Table 86. VESC_REG 57 (Offset 'hEC): General configuration register

Offset	Bits	Description	Value
0x5EC	vesc_reg57[0]	**cb_unexpected_cmpl_pkt_drop_en** 1'b0: Unexpected Completion is not dropped 1'b1: Unexpected Completion is dropped	1'b0
0x5EC	vesc_reg57[1]	**cb_user_tick_wide_delay_sel** 1'b0: UsecTick wide signal is 10 cycles 1'b1: UsecTick wide signal is 6 cycles	1'b0
0x5EC	vesc_reg57[2]	**cb_send_skip_befor_sds_recov_dis** 1'b0: Skip is sent in Recovery.Idle (before SDS) – legacy 1'b1: Skip is not sent in Recovery.Idle (before SDS)	1'b0
0x5EC	vesc_reg57[3]	**cb_send_skip_befor_sds_config_dis** 1'b0: Skip is sent in Configuration.Idle (before SDS) - legacy 1'b1: Skip is not sent in Configuration.Ilde (before SDS)	1'b0
0x5EC	vesc_reg57[4]	**cb_skip_before_sds_master_dis** 1'b0: Skip is permitted during Cfg or Recov Idle states 1'b1: Skip send is disabled during Cfg or Recov Idle states	1'b0
0x5EC	vesc_reg57[5]	**cb_got_one_logic_idle_extend** 1'b0: Got one logic ide considered after 2 bytes of zero 1'b1: Got one logic ide considered after 4 bytes of zero	1'b0
0x5EC	vesc_reg57[6]	**cb_send_less_skip_gen12** (Gen1/Gen2) 1'b0: Skip are sent according to Spec 1'b1: Skip are sent with bigger interval	1'b0
0x5EC	vesc_reg57[7]	**cb_send_less_skip_gen3** (Gen3) 1'b0: Skip are sent according to Spec 1'b1: Skip are sent with bigger interval	1'b0

Table 86. VESC_REG 57 (Offset 'hEC): General configuration register

Offset	Bits	Description	Value
0x5EC	vesc_reg57[8]	**cb_init_periodic_skip_upon_imm_skip** 1'b0: Periodic Skip and Imm Skip are nor connected 1'b1: Reset Periodic Skip Timer if Imm Skip is sent	1'b0
0x5EC	vesc_reg57[9]	**cb_send_two_sds_en** 1'b0: One SDS is sent in Configuration / Recovery Idle states 1'b1: Two SDS are sent in Configuration / Recovery Idle states	1'b0
0x5EC	vesc_reg57[10]	**cb_reduce_recov_idle_timeout** 1'b0: Recovery Idle timeout is according to Spec (~2ms) 1'b1: Recovery Idle timeout is lower (0.5 … 1 ms)	1'b0
0x5EC	vesc_reg57[11]	**cb_reduce_config_idle_timeout** 1'b0: Configuration Idle timeout is according to Spec (~2ms) 1'b1: Configuration Idle timeout is lower (0.5 … 1 ms)	1'b0
0x5EC	vesc_reg57[12]	**cb_extra_rd_req_grant_fix_dis** 1'b0: Credit available is updated immediately 1'b1: Credit available is updated immediately after FF (legacy)	1'b0
0x5EC	vesc_reg57[13]	**cb_recov_cfg_long_ei_infer_en** 1'b0: EI inferring timeout in Recovery.Cfg according to Spec 1'b1: EI inferring timeout in Recovery.Cfg is higher than Spec	1'b0
0x5EC	vesc_reg57[14]	**cb_force_com_queue_avail** 1'b0: MemRd is limited by Completion queue (16 reads) 1'b1: MemRd is not limited by Completion queue. (Bit is used in EMEP)	1'b0
0x5EC	vesc_reg57[15]	**cb_adv_vc0_credits_as_vc1_buf** 1'b0: No effect 1'b1: Port advertises half of VC0 Credits	1'b0
0x5EC	vesc_reg57[16]	**l1_aspm_exit_triger_dis** 1'b0: external trigger cause exit from L1 ASPM 1'b1: Exit from L1 ASPM is not effected by external trig-ger	1'b0

Table 86. VESC_REG 57 (Offset 'hEC): General configuration register

Offset	Bits	Description	Value
0x5EC	vesc_reg57[17]	**l1_entry_vc0_avail_credit_sel** 1'b0: L1 entry is allowed only if all credits are available 1'b1: L1 entry is allowed only if some credits are available	1'b0
0x5EC	vesc_reg57[18]	**l1_entry_vc1_avail_credit_sel** 1'b0: L1 entry is allowed only if all credits are available 1'b1: L1 entry is allowed only if some credits are available	1'b0
0x5EC	vesc_reg57[19]	**cb_exit_l1_upon_pending_credit** 1'b0: Non Periodic Credit update doesn't trigger L1 exit 1'b1: Non Periodic Credit update trigger L1 exit	1'b0
0x5EC	vesc_reg57[20]	**cb_custom_l2_fall_to_detect_sel** 1'b0: No effect 1'b1: Recovery to Detect acceleration in case of finished badly custom L2 flow.	1'b0
0x5EC	vesc_reg57[21]	**cb_pme_sent_delay_sel** 1'b0: An extra delay PME sent indication 1'b1: Legacy behavior	**1'b1**
0x5EC	vesc_reg57[22]	**cb_retrain_during_l1_prep_aspm_fix_dis** 1'b0: Fix to mask retrain if L1 started 1'b1: Fix is disabled	1'b0
0x5EC	vesc_reg57[23]	**cb_eq_master_change_req_after_long_time** 1'b0: No effect 1'b1: After long time EQ Master phase does not end, Master changes its request to try negotiate Gen3 link	1'b0
0x5EC	vesc_reg57[27:24]	**cb_eq_master_change_req_after_long_time (or reject)** Preset to request after long time Master Phase doesn't end	4'h0
0x5EC	vesc_reg57[28]	**cb_reject_l1_during_retrain_fix_dis** 1'b0: Fix to reject L1 in request if Retrain Link pending 1'b1:Fix is disabled	1'b0
0x5EC	vesc_reg57[29]	**cb_l0s_rx_short_ei_pulse_fix_dis** 1'b0: Legacy behavior 1'b0: Exit L0s even if there was relatively short Rx EI	1'b0

Table 86. VESC_REG 57 (Offset 'hEC): General configuration register

Offset	Bits	Description	Value
0x5EC	vesc_reg57[31:30]	**cb_l0s_entry_time_substract_sel** Selects the time after entry to L0s where a Rx EI low + RxValid high will trigger exit from the L0sRx state (if bit 29 is 0) 2'b00 – 10 cycles 2'b00 – 15 cycles 2'b00 – 20 cycles 2'b00 – 25 cycles	2'b00

Table 87. VESC_REG 58 (Offset 'hF0): General configuration register

Offset	Bits	Description	Value
0x5F0	vesc_reg58[0]	**cb_adv_half_nph_vc0_credits** 1'b0: No effect 1'b1: Port advertises half of VC0 Credits (NPH)	1'b0
0x5F0	vesc_reg58[1]	**cb_adv_half_npd_vc0_credits** 1'b0: No effect 1'b1: Port advertises half of VC0 Credits (NPD)	1'b0
0x5F0	vesc_reg58[2]	**cb_adv_half_ph_vc0_credits** 1'b0: No effect 1'b1: Port advertises half of VC0 Credits (PH)	1'b0
0x5F0	vesc_reg58[3]	**cb_adv_half_pd_vc0_credits** 1'b0: No effect 1'b1: Port advertises half of VC0 Credits (PD)	1'b0
0x5F0	vesc_reg58[4]	**cb_adv_half_cpl_vc0_credits** 1'b0: No effect 1'b1: Port advertises half of VC0 Credits (PH)	1'b0
0x5F0	vesc_reg58[5]	**cb_adv_half_cpl_vc0_credits** 1'b0: No effect 1'b1: Port advertises half of VC0 Credits (PD)	1'b0
0x5F0	vesc_reg58[6]	**cb_flop_ts_param_during_skip_en** 1'b0: TS fields are ignored during Skip (Legacy) 1'b1: Fix to capture the values of TS during Skip	**1'b1 ?**
0x5F0	vesc_reg58[7]	**cb_enable_vc1_reg_sel** 1'b0: Raw version of vc1 enable bit is used for Reg Top 1'b1: Floped version of vc1 enable bit is used for Reg Top	1'b0

Table 87. VESC_REG 58 (Offset 'hF0): General configuration register

Offset	Bits	Description	Value
0x5F0	vesc_reg58[8]	**cb_enable_vc1_port_sel** 1'b0: Raw version of vc1 enable bit is used for Port 1'b1: Floped version of vc1 enable bit is used for Port	1'b0
0x5F0	vesc_reg58[9]	**cb_prolong_rx_valid_for_eios_det_dis** 1'b0 : Rx Valid is prolonged to enable EIOS detection 1'b1 : Fix is disabled	1'b0
0x5F0	vesc_reg58[10]	**cb_prolong_rx_data_valid_for_eios_det_dis** 1'b0 : Rx Valid is prolonged to enable EIOS detection (Gen3) 1'b1 : Fix is disabled	1'b0
0x5F0	vesc_reg58[11]	**cb_clr_eios_flag_upon_entry_to_l2_fix_dis** 1'b0 : Fix to clear EIOS flag on entry to L2 1'b1 : Fix is disabled	1'b0
0x5F0	vesc_reg58[12]	**cb_l2_delay_eios_gen1_fix_dis** 1'b0 : Extra delay for L2 Power Down Change in gen1 1'b1 : Fix is disabled	1'b0
0x5F0	vesc_reg58[13]	**cb_l2_delay_eios_non_gen1_fix_dis** 1'b0 : Extra delay for L2 Power Down Change in non gen1 1'b1 : Fix is disabled	1'b0
0x5F0	vesc_reg58[14]	**cb_l2_wait_for_rx_ei_before_speed_change_en** 1'b0 : On entry to L2 Port changes the speed after some time 1'b1 : On entry to L2 Port changes the speed after get-ting EI	1'b0
0x5F0	vesc_reg58[15]	**cb_l0x_rx_exit_upon_rx_valid_rise_fix_dis** 1'b0 : Fix to exit Rx L0s if Rx Valid rise 1'b1 : Fix is disabled	1'b0
0x5F0	vesc_reg58[16]	**cb_nak_b2b_after_ack_missed_fix_dis** 1'b0 : Fix to remember NAK that came b2b after two Acks 1'b1 : Fix is disabled	1'b0
0x5F0	vesc_reg58[16]	**cb_chan0_vc0_short_ipg_fix_dis** 1'b0 : Arbiter wait 1 cycles in Fine Adjust state 1'b1 : Arbiter wait 2 cycles in Fine Adjust state	1'b0

Table 87. VESC_REG 58 (Offset 'hF0): General configuration register

Offset	Bits	Description	Value
0x5F0	vesc_reg58[17]	**cb_chan1_ vc0_short_ipg_fix_dis** 1'b0: Arbiter wait 1 cycles in Fine Adjust state 1'b1: Arbiter wait 2 cycles in Fine Adjust state	1'b0
0x5F0	vesc_reg58[18]	**cb_chan2_ vc0_short_ipg_fix_dis** 1'b0: Arbiter wait 1 cycles in Fine Adjust state 1'b1: Arbiter wait 2 cycles in Fine Adjust state	1'b0
0x5F0	vesc_reg58[19]	**cb_chan3_ vc0_short_ipg_fix_dis** 1'b0: Arbiter wait 1 cycles in Fine Adjust state 1'b1: Arbiter wait 2 cycles in Fine Adjust state	1'b0
0x5F0	vesc_reg58[20]	**cb_chan0_vc1_short_ipg_fix_dis** 1'b0 : Arbiter wait 1 cycles in Fine Adjust state 1'b1 : Arbiter wait 2 cycles in Fine Adjust state	1'b0
0x5F0	vesc_reg58[21]	**cb_chan1_ vc1_short_ipg_fix_dis** 1'b0: Arbiter wait 1 cycles in Fine Adjust state 1'b1: Arbiter wait 2 cycles in Fine Adjust state	1'b0
0x5F0	vesc_reg58[22]	**cb_chan2_ vc1_short_ipg_fix_dis** 1'b0: Arbiter wait 1 cycles in Fine Adjust state 1'b1: Arbiter wait 2 cycles in Fine Adjust state	1'b0
0x5F0	vesc_reg58[23]	**cb_chan3_ vc1_short_ipg_fix_dis** 1'b0: Arbiter wait 1 cycles in Fine Adjust state 1'b1: Arbiter wait 2 cycles in Fine Adjust state	1'b0
0x5F0	vesc_reg58[24]	**cb_chan0_vc0_skip_update_credit_state_sel** 1'b0: No Effect 1'b1: Skip Update Credit state on channel 0 (This bit is valid for EP and reserved for Up/Dn)	(EP) 1'b0 (Sim - rand)
0x5F0	vesc_reg58[25]	**cb_chan1_ vc0_skip_update_credit_state_sel** 1'b0: No Effect 1'b1: Skip Update Credit state on channel 1 (This bit is valid for EP and reserved for Up/Dn)	(EP) 1'b0 (Sim - rand)
0x5F0	vesc_reg58[26]	**cb_chan2_vc0_skip_update_credit_state_sel** 1'b0: No Effect 1'b1: Skip Update Credit state on channel 2 (This bit is valid for EP and reserved for Up/Dn)	(EP) 1'b0 (Sim - rand)

Table 87. VESC_REG 58 (Offset 'hF0): General configuration register

Offset	Bits	Description	Value
0x5F0	vesc_reg58[27]	**cb_chan3_ vc0_skip_update_credit_state_sel** 1’b0: No Effect 1’b1: Skip Update Credit state on channel 3 (This bit is valid for EP and reserved for Up/Dn)	(EP) 1'b0 (Sim - rand)
0x5F0	vesc_reg58[28]	**cb_chan0_vc1_skip_update_credit_state_sel** 1’b0: No Effect 1’b1: Skip Update Credit state on channel 0 (This bit is valid for EP and reserved for Up/Dn)	(EP) 1'b0 (Sim - rand)
0x5F0	vesc_reg58[29]	**cb_chan1_ vc1_skip_update_credit_state_sel** 1’b0: No Effect 1’b1: Skip Update Credit state on channel 1 (This bit is valid for EP and reserved for Up/Dn)	(EP) 1'b0 (Sim - rand)
0x5F0	vesc_reg58[30]	**cb_chan2_vc1_skip_update_credit_state_sel** 1’b0: No Effect 1’b1: Skip Update Credit state on channel 2 (This bit is valid for EP and reserved for Up/Dn)	(EP) 1'b0 (Sim - rand)
0x5F0	vesc_reg58[31]	**cb_chan3_ vc1_skip_update_credit_state_sel** 1’b0: No Effect 1’b1: Skip Update Credit state on channel 3 (This bit is valid for EP and reserved for Up/Dn)	(EP) 1'b0 (Sim - rand)

Table 88. VESC_REG 59 (Offset 'hF4): Custom L1 Sub-states register

Offset	Bits	Description	Value
0x5F4	vesc_reg59[1:0]	**L1_sub1_idle_time_sel** Selects the minimum time to stay in L1 Sub1 Idle state 1’b00: 0 us 1’b01: 1 us 1’b10: 2 us 1’b11: 3 us	**2'b1**
0x5F4	vesc_reg59[3:2]	**L1_sub1_exit_time_sel** Selects the minimum time to stay in L1 Sub1 exit state 1’b00: 0 us 1’b01: 1 us 1’b10: 2 us 1’b11: 3 us	2'b0

Table 88. VESC_REG 59 (Offset 'hF4): Custom L1 Sub-states register

Offset	Bits	Description	Value
0x5F4	vesc_reg59[5:4]	**L1_sub2_idle_exit_time_sel** Selects the minimum time to stay in L1 Sub2 Idle state 1'b00: 4 us 1'b01: 5 us 1'b10: 6 us 1'b11: 7 us	2'b0
0x5F4	vesc_reg59[7:6]	**L1_idle_exit_time_sel** Selects the minimum time to stay in L1 Sub2 Idle state 1'b00: 0 ns 1'b01: 400 ns 1'b10: 800 ns 1'b11: 1200 ns	**2'b11**
0x5F4	vesc_reg59[8]	**cb_l1_sub1_cancel_l1idle_exit_time** 1'b0: After L1 Sub1 Port waits L1 Idle exit time 1'b1: After L1 Sub1 Port doesn't waits L1 Idle exit time	**1'b1**
0x5F4	vesc_reg59[9]	**cb_l1_sub2_cancel_l1idle_exit_time** 1'b0: After L1 Sub1 Port waits L1 Idle exit time 1'b1: After L1 Sub1 Port doesn't waits L1 Idle exit time	**1'b1**
0x5F4	vesc_reg59[11:10]	**cb_t_power_on_substract_sel** Selects how much to reduce the T_POWER_ON timer 1'b00: Reduce 0% 1'b01: Reduce 25% 1'b10: Reduce 50% 1'b11: Reduce 75%	2'b0
0x5F4	vesc_reg59[12]	**cb_dn_exit_l1_wait_for_stable_dis** 1'b0: Downstream Port waits for clock stable t exit L1 1'b1: Downstream Port doesn't waits for clock stable t exit L1	1'b0
0x5F4	vesc_reg59[13]	**cb_l1_sub1_skip_exit_state** 1'b0: No effect (normal exit) 1'b1: After L1 Sub1 Port doesn't wait for PhyStatus and proceed to state for clock stable waiting	1'b0

Table 88. VESC_REG 59 (Offset 'hF4): Custom L1 Sub-states register

Offset	Bits	Description	Value
0x5F4	vesc_reg59[14]	**cb_l1_sub2_skip_exit_state** 1'b0: No effect (normal exit) 1'b1: After L1 Sub2 Port doesn't wait for PhyStatus and proceed to state for clock stable waiting	1'b0
0x5F4	vesc_reg59[15]	**cb_clk_req_rise_delay_sel** 1'b0: Enables several flops filter on rising of CLKREQ (input) 1'b1: Filter is disabled	1'b0
0x5F4	vesc_reg59[16]	**cb_clk_req_fall_delay_sel** 1'b0: Enables several flops filter on falling of CLKREQ (input) 1'b1: Filter is disabled	1'b0
0x5F4	vesc_reg59[27:17]	Reserved	
0x5F4	vesc_reg59[29:28]	**alow_clock_freq_sel** 2'b00: 100 MHz (default mode) 2'b01: 60 MHz 2'b10: 50 MHz 2'b11: 30 MHz	2'b0
0x5F4	vesc_reg59[30]	**l1_idle_bigger_exit_timer** 1'b0: L1 Idle exit time is small – 0,400,800,1200 ns 1'b1: L1 Idle exit time is small – 0,2,4,6 us (Bits [7:6] selects one of four values)	1'b0
0x5F4	vesc_reg59[31]	**cb_force_exit_l1_sub** A DFT option to cause exit from L1 Sub-state	1'b0

Table 89. VESC_REG 60 (Offset 'hF8): General FPB register 1

Offset	Bits	Description	Value
0x5F8	vesc_reg60[0]	**cb_fpb_bdf_vector_clear_from_vesc** 1'b0: No effect 1'b1: Clears the FPB BDF Vector	1'b0
0x5F8	vesc_reg60[1]	**cb_fpb_bdf_vector_or_legacy_tlp_decode_range** 1'b0: FPB and Legacy are used with OR in TLP Decode 1'b1: FPB logic is used instead of Legacy in TLP Decode	1'b0
0x5F8	vesc_reg60[2]	**cb_fpb_bdf_vector_or_legacy_tlp_decode_secondary** 1'b0: FPB and Legacy are used with OR in TLP Decode 1'b1: FPB logic is used instead of Legacy in TLP Decode	1'b0

Table 89. VESC_REG 60 (Offset 'hF8): General FPB register 1

Offset	Bits	Description	Value
0x5F8	vesc_reg60[3]	**cb_fpb_bdf_vector_or_legacy_range_post** 1'b0: FPB and Legacy are used with OR in Rx Post Queue 1'b1: FPB logic is used instead of Legacy in Rx Post Queue	1'b0
0x5F8	vesc_reg60[4]	**cb_fpb_bdf_vector_or_legacy_range_comp** 1'b0: FPB and Legacy are used with OR in Rx Cmpl Queue 1'b1: FPB logic is used instead of Legacy in Rx Cmpl Queue	1'b0
0x5F8	vesc_reg60[5]	**cb_fpb_bdf_vector_or_legacy_range_non_post** 1'b0: FPB and Legacy are used with OR in Rx Non Post Queue 1'b1: FPB logic is used instead of Legacy in Rx Non Post Queue This bit is used only in Up Port (reserved for Dn)	1'b0
0x5F8	vesc_reg60[6]	**cb_fpb_bdf_vector_or_legacy_type1_to_type0** 1'b0: FPB and Legacy are used with OR in Rx Non Post Queue 1'b1: FPB logic is used instead of Legacy in Rx Non Post Queue This bit is used only in Up Port (reserved for Dn)	1'b0
0x5F8	vesc_reg60[7]	Reserved	1'b0
0x5F8	vesc_reg60[8]	**cb_fpb_mem_low_vector_clear_from_vesc** 1'b0: No effect 1'b1: Clears the FPB MEM LOW Vector	1'b0
0x5F8	vesc_reg60[9]	**cb_fpb_mem_low_vector_or_legacy_tlp_decode** 1'b0: FPB and Legacy are used with OR in TLP Decode 1'b1: FPB logic is used instead of Legacy in TLP Decode	1'b0
0x5F8	vesc_reg60[10]	**cb_fpb_mem_low_vector_or_legacy_range_post** 1'b0: FPB and Legacy are used with OR in RX Post Queue 1'b1: FPB logic is used instead of Legacy in RX Post Queue	1'b0
0x5F8	vesc_reg60[11]	**cb_fpb_mem_low_vector_or_legacy_range_non post** 1'b0: FPB and Legacy are used with OR in RX Non Post Queue 1'b1: FPB logic is used instead of Legacy in RX Non Post Queue	1'b0
0x5F8	vesc_reg60[15:11]	Reserved	0

Table 89. VESC_REG 60 (Offset 'hF8): General FPB register 1

Offset	Bits	Description	Value
0x5F8	vesc_reg60[16]	**cb_fpb_mem_high_vector_clear_from_vesc** 1'b0: No effect 1'b1: Clears the FPB MEM High Vector	1'b0
0x5F8	vesc_reg60[17]	**cb_fpb_mem_high_vector_or_legacy_tlp_decode** 1'b0: FPB and Legacy are used with OR in TLP Decode 1'b1: FPB logic is used instead of Legacy in TLP Decode	1'b0
0x5F8	vesc_reg60[18]	**cb_fpb_mem_high_vector_or_legacy_range_post** 1'b0: FPB and Legacy are used with OR in RX Post Queue 1'b1: FPB logic is used instead of Legacy in Rx Post Queue	1'b0
0x5F8	vesc_reg60[19]	**cb_fpb_mem_high_vector_or_legacy_range_non_post** 1'b0: FPB and Legacy are used with OR in RX Non Post Queue 1'b1: FPB logic is used instead of Legacy in Rx Non Post Queue	1'b0
0x5F8	vesc_reg60[23:20]	Reserved	0
0x5F8	vesc_reg60[24]	**cb_fpb_bdf_vector_or_legacy_dn_access_non_post_-queue** 1'b0: FPB logic is used instead of Legacy in Rx Non Post Queue 1'b1: FPB and Legacy are used with OR in Rx Non Post Queue This bit is used only in Up Port (reserved for Dn)	1'b0
0x5F8	vesc_reg60[25]	**cb_fpb_bdf_vector_or_legacy_dn_ac-cess_non_post_hnadler** 1'b0: FPB logic is used instead of Legacy in Rx NP Han-dler 1'b1: FPB and Legacy are used with OR in Rx NP Handler This bit is used only in Up Port (reserved for Dn)	1'b0
0x5F8	vesc_reg60[28:26]	Reserved	
0x5F8	vesc_reg60[29]	**FPB Clear Vector policy** 1'b0: FPB Vectors cleared when Vector is not enabled 1'b1: FPB Vectors cleared only on HW events (same events that clear Base/Limit, Secondary/Subordinate registers)	1'b0

Table 89. VESC_REG 60 (Offset 'hF8): General FPB register 1

Offset	Bits	Description	Value
0x5F8	vesc_reg60[31:30]	**FPB Capability type select** 2'b00: FPB Capability is a PCI type (regular) 2'b01: FPB Capability is a PCIE Extended Capability 2'b10: FPB Capability is a Designated VESC Capability 2'b11: No FPB Capability	2'b00

Table 90. VESC_REG 61 (Offset 'hFC): General FPB register 2

Offset	Bits	Description	Value
0x5FC	vesc_reg61[15:0]	**FPB Capability ID** Field that is take to FPB Capability ID and it depends on the Capability type that selected by vesc_reg60[31:30] vesc_reg60[31:30] == 2'b00 → Cap ID – [7:0] vesc_reg60[31:30] == 2'b01/2'b10 → Cap ID – [15:0]	16'b0
0x5FC	vesc_reg61[27:16]	Reserved	0
0x5FC	vesc_reg61[31:28]	DFT - Selectors for Muxes of Signals to Visa	4'h0

4.3.13.1 TBT Registers access through PCIE

The access is done through three registers in Upstream Port Vendor register Space (Reg10,11,12 - 0x530,0x534, 0x538).

- **Register 1 (0x530)** is a Command (two special bits: 30,31)
  - Bit 30 is a status bit that indicates that access is in progress (set by SW cleared by HW)
  - Bit 31 is a timeout bit that indicates that the returned data is invalid (loaded with ack)
- **Register 2 (0x534)** is a Write Data Register (simple Wr/Rd register)
- **Register 3 (0x538)** is a Read Data Register (Rd Only register) loaded with ack by HW.

Write command flow:

- PCIE Software writes Data to Write Data Register

- PCIE Software writes Command Register - bit 30 indicates to start write command

- PCIE Switch wrapper logic perform write of CIO register

- Ack and timeout are returned (bits 30 is cleared by ack, bit 31 is loaded from timeout input)

- SW read the Command Register to see if there is no timeout (bit 30 and 31 are zero)

Read command flow:

- PCIE Software writes Command Register - bit 30 indicates to start read command

- PCIE Switch wrapper logic perform read of CIO register.

- Ack and timeout are returned (bits 30 is cleared by ack,31 is loaded from timeout input)

- Input DW rd_data signal is loaded to Read Data Register based on ack input pulse.

- SW read the Command Register to see if there is no timeout (bit 30 and 31 are zero)

- PCIE Software can read Data Register (if transaction is finished and there is no timeout - bits 30,31)

See also Table 17, "Command Register Parameters" on page 84.

4.3.13.2 Custom PCIE-TBT Mailbox Registers

The registers TBT2PCIE/PCIE2TBT act as a Mailbox and enable communication between the SW and the CM/LC

- SW initiates a transaction through the PCIE2TBT Mailbox by setting PCIE2TBT with a message and setting the "Valid" bit
- CM/LC are interrupted on this transaction, CM/LC execute on the transaction
- Once done CM/LC sets the "Done" bit in TBT2PCIE with the proper command and data
- SW polls TBT2PCIE for the "Done" bit (and potential data as needed)
- SW clears the PCIE2TBT "Valid" bit, CM is interrupted on this transaction
- CM clears the TBT2PCIE "Done" bit
- SW should poll to see Done bit is cleared
- At this point the SW driver can issue another PCIE2TBT transaction as needed

4.3.13.3 Custom LTR Registers

Custom LTR registers are located under Vendor Defined Extended Capability that starts at offset 0x500.

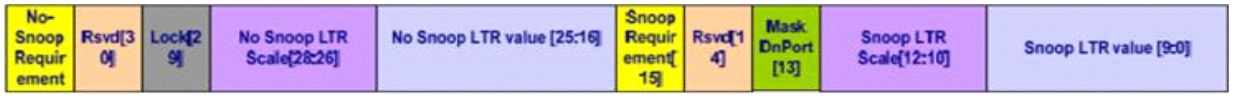
Downstream Port (offsets 0x53C, 0x540 and 0x544)

- Configurable LTRDnport registers for snoop / non-snoop (one DW similar to the Message)
  - register captures latency from LTR message (unless "lock" bit is set)
  - software or internal chip logic can override and lock this register.
  - change of the register triggers LTR message on Upstream Port (if conglomerated value was changed)
- Configurable bit in to ignore this Downstream Port LTR values for calculation
  - change of the register trigger LTR message on Upstream Port (if conglomerated value was changed)

Offset 0x53C - LTR Idle Value.

See Figure 22.

Figure 22. LTR Idle Value



Offset 0x540 - LTR Active Value (Same structure as Idle beside the bits 29 and 13 are reserved)

Offset 0x544 - LTR active timer initial value control (Rd / Wr DW)

Embedded Endpoint (offset 0x53C)

- Configurable **LTREMEP** register for LTR snoop / non-snoop latency (one DW as in Message)
  - — software or internal chip logic can load this register.
  - — change of the register triggers LTR message in Embedded Endpoint (if value was changed or "send" bit)

Figure 23. LTR Value of Embedded Endpoint

Note: "send" bit is self-cleared (cleared after the message has been sent)

Upstream Port (offsets 0x53C and 0x540)

- Configurable **LTRConglomerated** register for snoop / non-snoop
  - — register is calculated according to Spec (unless "lock" bit is set)
  - — software or internal chip logic can override this register.
  - — change of the register trigger LTR message on Upstream Port (if value was changed or "send" bit)
- Configurable **LSwitch** registers to enable control over Switch latency value.
  - — software or internal chip logic can override this register.
  - — change of the register triggers LTR message on Upstream Port (if conglomerated value was changed)

Offset 0x53C - LTR Conglomerated Value

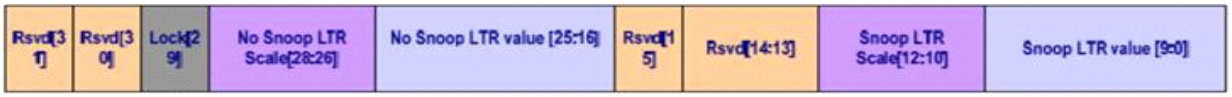
See Figure 24.

Figure 24. LTR Conglomerated Value

Offset 0x540 - LSwitch register

SeeFigure 25.

Figure 25. LSwitch register



Note: "send" bit is self-cleared (cleared after the message has been sent)

Offset 0x544 - BIOS mailbox (Rd / Wr)

Table 91. VESC_REG 49: (Offset CCh): General configuration register

Offset	Bits	Description	Value
0x544	vesc_reg15[0]	Hot plug filter indication, if read as 1, BIOS should clear the bit and continue normal flow, if read as 0 BIOS should exit the GPIO handler. This bit is only implemented in AR, not applicable for older projects.	1'b0
0x544	vesc_reg15[31:1]	Reserved	31'b0

4.3.14 Vendor Specific Enhanced Capability 2

Table 92 details the layout of register fields for the Second Vendor Specific Enhanced registers. These registers contain general purpose bits: different modes, dft bits and chicken bits. Vendor Registers might be loaded from FLASH. This capability only exists in PCIE Switch (Upstream and Downstream Ports).

Table 92. Vendor Specific Enhanced Registers 2 Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x600	VS2_CAP_0	31:0	PCI Express Enhance Capability Header	RO	0x7001000B
0x604	VS2_CAP_1	31:0	Vendor Specific Header	RO	0x04C28086
0x608	VS2_CAP_2	31:0	Vendor 2 Register 0 (VSEC2_REG0)	R/W	See following tables
0x60C	VS2_CAP_3	31:0	Vendor 2 Register 1 (VSEC2_REG1)	R/W	See following tables
0x610	VS2_CAP_4	31:0	Vendor 2 Register 2 (VSEC2_REG2)	R/W	See following tables
0x614	VS2_CAP_5	31:0	Vendor 2 Register 3 (VSEC2_REG3)	R/W	See following tables
0x618	VS2_CAP_6	31:0	Vendor 2 Register 4 (VSEC2_REG4)	R/W	See following tables
0x61C	VS2_CAP_7	31:0	Vendor 2 Register 5 (VSEC2_REG5)	R/W	See following tables
0x620	VS2_CAP_8	31:0	Vendor 2 Register 6 (VSEC2_REG6)	R/W	See following tables
0x624	VS2_CAP_9	31:0	Vendor 2 Register 7 (VSEC2_REG7)	R/W	See following tables
0x628	VS2_CAP_10	31:0	Vendor 2 Register 8 (VSEC2_REG8)	R/W	See following tables

Table 92. Vendor Specific Enhanced Registers 2 Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x62C	VS2_CAP_11	31:0	Vendor 2 Register 9 (VSEC2_REG9)	R/W	See following tables

Legacy Vendor Registers (Titan Ridge):

Reg 0 (0x8) - Custom PTM registers 1

Reg 1 (0xC) - Custom PTM registers 2

Reg 2 (0x10) - Custom PTM registers 3

Reg3 (0x14) - Custom PTM registers 4

Reg4 (0x18) - Custom PTM registers 5

Reg5 (0x1C) - Custom PTM registers 6

Reg6 (0x20) - Custom PTM registers 7

Reg7 (0x24) - Custom PTM registers 8

Reg8 (0x28) - Custom PTM registers 9

Reg9 (0x2C) - Custom PTM registers 10

Table 93. VESC2_REG 0 (Offset 'h08): Custom PTM registers 1

Offset	Bits	Description	Value
0x608	vesc2_reg0[0]	**facing_cio** 1'b0: Port facing Physical Link 1'b1: Port facing CIO Link	1'b0
0x608	vesc2_reg0[1]	**cfg_ptm_test_mode** 1'b0: No effect 1'b1: A test mode where Up request PTM time, but Downstream will provide the TMU time and not the time recovered by Upstream (Defined for Upstream Port and reserved in Downstream Ports)	1'b0

Table 93. VESC2_REG 0 (Offset 'h08): Custom PTM registers 1

Offset	Bits	Description	Value
0x608	vesc2_reg0[3:2]	**cfg_ptm_l1_policy** 2'b00: PTM Request is triggered according to counter only. Once Timer is expired Upstream exit L1. PTM Context stays valid all the time 2'b01: If Up is I L1, PTM Request is triggered if: Context is not Valid due to regular periodic expired. PTM Request was received in valid Downstream ports. (Dn Port can be masked by bit [4] individual per Dn Port) 2'b10: PTM Request is not triggered while Upstream is in L1 It will just invalidate its PTM Contexts when it expires. If Dn gets PTM Request it just sends PTM Respond (assumption is if PTM is needed a traffic will start) 2'b11: Reserved Defined for Upstream Port and reserved in Downstream Ports	2'b00
0x608	vesc2_reg0[4]	**Ptm_Dn_wake_Up_from_L1_dis** 1'b0: Received PTM Request triggers a request in Up Port 1'b1: Received PTM Request doesn't triggers a request in Up Port	1'b0
0x608	vesc2_reg0[31:5]	Reserved	'h0

Table 94. VESC2_REG 1 (Offset 'h0C): Custom PTM registers 2

Offset	Bits	Description	Value
0x60C	vesc2_reg1[7:0]	**cfg_rx_correction_pclk_x1_Up0** Pclk receive correction time value for Upstream in Xmode = 1	8'h0
0x60C	vesc2_reg1[15:8]	**cfg_rx_correction_pclk_x2_Up0** Pclk receive correction time value for Upstream in Xmode = 2	8'h0
0x60C	vesc2_reg1[23:16]	**cfg_rx_correction_pclk_x4_Up0** Pclk receive correction time value for Upstream in Xmode = 4	8'h0
0x60C	vesc2_reg1[31:24]	**cfg_rx_correction_swclk_Up0** swclk receive correction time value for Upstream	8'h0

Table 95. VESC2_REG 2 (Offset 'h10): Custom PTM registers 3

Offset	Bits	Description	Value
0x610	vesc2_reg2[7:0]	**cfg_tx_correction_pclk_x1_Up0** Pclk transmit correction time value for Upstream in Xmode = 1	8'h0
0x610	vesc2_reg2[15:8]	**cfg_tx_correction_pclk_x2_Up0** Pclk transmit correction time value for Upstream in Xmode = 2	8'h0
0x610	vesc2_reg2[23:16]	**cfg_tx_correction_pclk_x4_Up0** Pclk transmit correction time value for Upstream in Xmode = 4	8'h0

Table 95. VESC2_REG 2 (Offset 'h10): Custom PTM registers 3

Offset	Bits	Description	Value
0x610	vesc2_reg2[31:24]	**cfg_tx_correction_swclk_Up0** swclk transmit correction time value for Upstream	8'h0

Table 96. VESC2_REG 3 (Offset 'h14): Custom PTM registers 4

Offset	Bits	Description	Value
0x614	vesc2_reg3[14:0]	**cfg_time_between_requests** Configurable time range for Upstream between PTM Request messages	15'h0
0x614	vesc2_reg3[15]	Reserved	1'b0
0x614	vesc2_reg3[30:16]	**cfg_invalidation_timer_limit** Configurable time range for Upstream till PTM Context is invalidated	15'h0
0x614	vesc2_reg3[31]	Reserved	1'b0

Table 97. VESC2_REG 4 (Offset 'h18): Custom PTM registers 5

Offset	Bits	Description	Value
0x618	vesc2_reg4[1:0]	Reserved	2'h0
0x618	vesc2_reg4[2]	**cfg_send_ptm_resp_when_not_valid** 1'b1 : Enable send PTM response when PTM time is not valid	1'h0
0x618	vesc2_reg4[7:3]	cfg_ptm_iir_xy_filt_stren	5'h0
0x618	vesc2_reg4[11:8]	cfg_ptm_iir_tx_delay_filt_stren	4'h0
0x618	vesc2_reg4[16:12]	cfg_dump_limit	5'h0
0x618	vesc2_reg4[17]	cfg_filt_incr_en	1'h0
0x618	vesc2_reg4[31:18]	Reserved	0

Table 98. VESC2_REG 5 (Offset 'h1C): Custom PTM registers 6

Offset	Bits	Description	Value
0x61C	vesc2_reg5[0]	**force_invalidate_ptm_context_from_vesc** 1'b0: No Effect 1'b1: Triggers PTM invalidation Context	1'b0
0x61C	vesc2_reg5[1]	**invalidate_ptm_upon_link_down_dis** 1'b0: PTM Context is invalidated upon Link Down 1'b1: PTM Context is not invalidated upon Link Down	1'b0
0x61C	vesc2_reg5[2]	**invalidate_ptm_upon_link_disabled_dis** 1'b0: PTM Context is invalidated upon Link Disable 1'b1: PTM Context is not invalidated upon Link Disable	1'b0
0x61C	vesc2_reg5[3]	**invalidate_ptm_upon_hot_reset_dis** 1'b0: PTM Context is invalidated upon Hot Reset 1'b1: PTM Context is not invalidated upon Hot Reset	1'b0
0x61C	vesc2_reg5[4]	**invalidate_ptm_upon_entry_to_l2_dis** 1'b0: PTM Context is invalidated upon entry to L2 1'b1: PTM Context is not invalidated upon Link Down	1'b0
0x61C	vesc2_reg5[5]	**invalidate_ptm_upon_entry_to_l1_dis** 1'b0: PTM Context is invalidated upon entry to L1 1'b1: PTM Context is not invalidated upon entry to L1	1'b0

Table 98. VESC2_REG 5 (Offset 'h1C): Custom PTM registers 6

Offset	Bits	Description	Value
0x61C	vesc2_reg5[6]	**invalidate_ptm_upon_exit_from_d0_dis** 1'b0: PTM Context is invalidated upon exit from D0 1'b1: PTM Context is not invalidated upon exit from D0	1'b0
0x61C	vesc2_reg5[7]	Reserved	1'b0
0x61C	vesc2_reg5[8]	**force_send_ptm_from_vesc** 1'b0: No Effect 1'b1: Triggers PTM Request Message (Upstream Port)	1'b0
0x61C	vesc2_reg5[9]	**Send_ptm_upon_entry_to_l0_dis** 1'b0: PTM Request is triggered upon entry to L0 1'b1: PTM Request is not triggered upon entry to L0	1'b0
0x61C	vesc2_reg5[10]	**Send_ptm_upon_entry_to_d0_dis** 1'b0: PTM Request is triggered upon entry to D0 1'b1: PTM Request is not triggered upon entry to D0	1'b0
0x61C	vesc2_reg5[31:11]	Reserved	32'h0

Table 99. VESC2_REG 6 (Offset 'h20): Custom PTM registers 7

Offset	Bits	Description	Value
0x620	vesc2_reg6[7:0]	**cfg_phy_tx_latency_gen1** Latency of PHY Tx data path in ns in gen1	8'h0
0x620	vesc2_reg6[15:8]	**cfg_phy_tx_latency_gen2** Latency of PHY Tx data path in ns in gen2	8'h0
0x620	vesc2_reg6[23:16]	**cfg_phy_tx_latency_gen3** Latency of PHY Tx data path in ns in gen3	8'h0
0x620	vesc2_reg6[31:24]	Reserved	8'h0

Table 100. VESC2_REG 7 (Offset 'h24): Custom PTM registers 8

Offset	Bits	Description	Value
0x624	vesc2_reg7[7:0]	**cfg_phy_rx_latency_gen1** Latency of PHY Rx data path in ns in gen1	8'h0
0x624	vesc2_reg7[15:8]	**cfg_phy_rx_latency_gen2** Latency of PHY Rx data path in ns in gen2	8'h0
0x624	vesc2_reg7[23:16]	**cfg_phy_rx_latency_gen3** Latency of PHY Rx data path in ns in gen3	8'h0
0x624	vesc2_reg7[31:24]	Reserved	8'h0

Table 101. VESC2_REG 8 (Offset 'h28): Custom PTM registers 9

Offset	Bits	Description	Value
0x628	vesc2_reg8[5:0]	**cfg_p_t_d_port_select** Replace DN port number N by TMU debug block to get tmu time	6'h0
0x628	vesc2_reg8[6]	**cfg_p_t_d_en** 1'b1 : Enable TMU debug feature	1'h0
0x628	vesc2_reg8[31:7]	Reserved	0

Table 102. VESC2_REG 9 (Offset 'h2C): Custom PTM registers 10

Offset	Bits	Description	Value
0x62C	vesc2_reg9[14:0]	**cfg_p_t_m_time_btw_send** Configurable time range for Upstream between PTM Request messages	15'h0
0x62C	vesc2_reg9[15]	Reserved	1'b0
0x62C	vesc2_reg9[30:16]	**cfg_p_t_m_tmu_future_delay** Configurable time range for Upstream till PTM Context is invalidated	15'h0
0x62C	vesc2_reg9[31]	Reserved	1'b0

4.3.15 Secondary PCIE Extended Capability

The Secondary PCIE Extended Capability structure is required in all Ports that supports Gen3.

Figure 26 details the structure of register fields for Secondary PCIE registers and Table 103 describes the registers' fields.

Figure 26. Secondary PCIE Registers

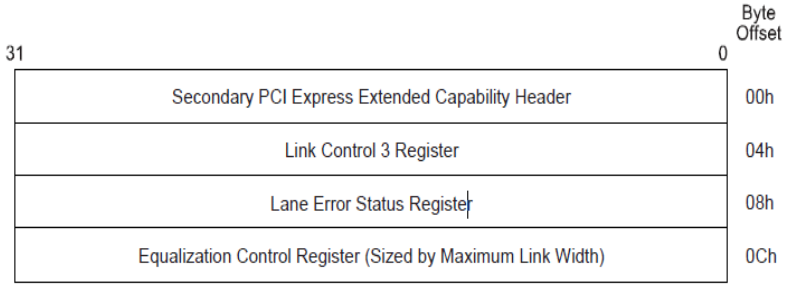


Table 103. Secondary PCIE Extended Capability Registers Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x700	SPCIE_CAP_0	31:0	PCI Express Enhance Capability Header	RO	Up - 32'h80010019 Dn - 32'h90010019 XHC - 2'h00010019
0x704	SPCIE_CAP_1	31:0	Link Control 3 Register	See PCIe Spec	32'h0
0x708	SPCIE_CAP_2	3:0	Lane Error Status (4 lanes)	RW1CS	4'h0
0x708	SPCIE_CAP_2	31:4	Lane Error Status (Reserved)	RO	28'h0
0x70C	SPCIE_CAP_3	15:0	Lane (0) Equalization Control	See PCIe Spec	16'h7F00
0x70C	SPCIE_CAP_3	31:16	Lane (1) Equalization Control	See PCIe Spec	16'h7F00
0x710	SPCIE_CAP_4	15:0	Lane (2) Equalization Control	See PCIe Spec	16'h7F00
0x710	SPCIE_CAP_4	31:16	Lane (3) Equalization Control	See PCIe Spec	16'h7F00

4.3.16 Latency Tolerance Reporting Capability

Latency Tolerance Reporting (LTR) Capability is an Extended Capability that allows software to provide platform latency information to components with Upstream Ports. This capability is implemented in Upstream Port and Embedded endpoint.

Figure 27 details the structure of register fields for LTR capability registers and Table 104 describes the registers' fields.

Figure 27. LTR Registers

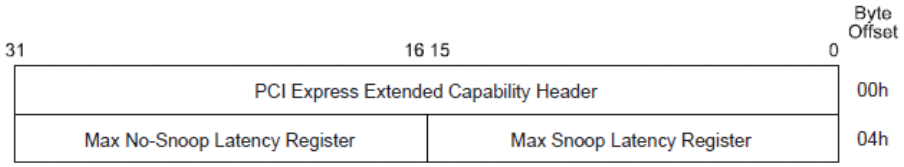


Table 104. LTR Capability Registers Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x800	LTR_CAP_0	31:0	PCI Express Enhance Capability Header	RO	32'hA0010018
0x804	LTR_CAP_1	15:0	Max Snoop Latency Register	See PCIe Spec	32'h0
0x804	LTR_CAP_1	31:16	Max Snoop Latency Register	See PCIe Spec	32'h0

4.3.17 Access Control Services Extended Capability

The ACS Extended Capability is an optional capability that provides enhanced access controls. In Thunderbolt it implemented in Downstream Ports of PCIE Switch. Figure 28 details the structure of register fields for Secondary PCIE registers and Table 105 describes the registers' fields.

Figure 28. ACS Extended Capability Structure

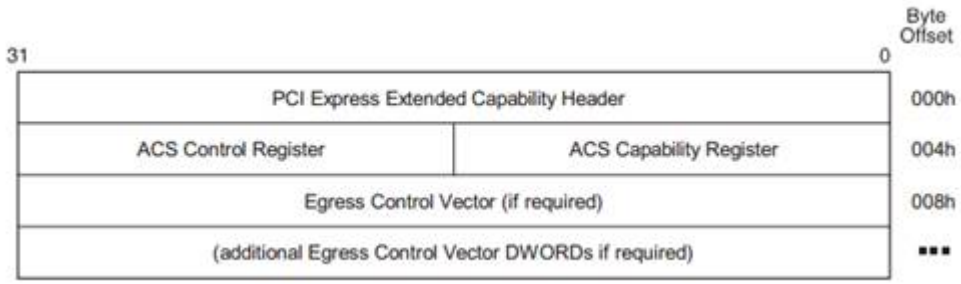


Table 105. Access Control Services Extended Capability Registers

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x900	ACS_CAP_0	31:0	PCI Express Enhance Capability Header	RO	32'h0001000D
0x904	ACS_CAP_1	15:0	ACS Capability Register	See PCIe Spec	16'h13
0x904	ACS_CAP_1	31:16	ACS Control Register	See PCIe Spec	16'h0

4.3.18 L1 PM Substates Extended Capability

The PCI Express L1 PM Substates Capability is an optional Extended Capability, that is required if L1 PM Substates is implemented at a Port. In Thunderbolt it implemented in Upstream Ports of PCIE Switch and intended to be used only in Host Router mode. Figure 29 details the structure of register fields for Secondary PCIE registers and Table 106 describes the registers' fields.

Figure 29. L1 PM Substates Extended Capability Structure

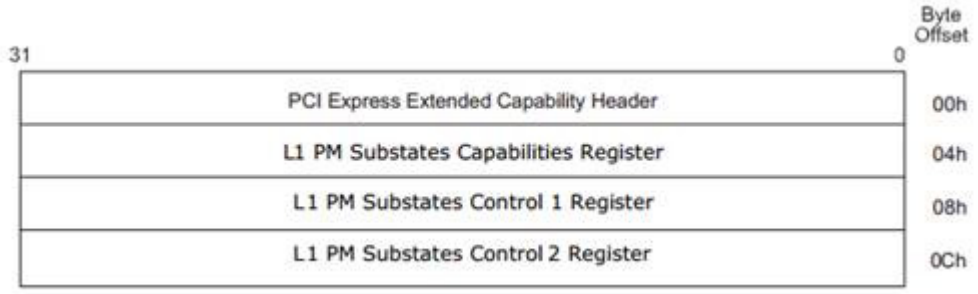


Table 106. L1 PM Substates Extended Capability Structure Registers

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0xA00	L1_SUB_CAP_0	31:0	PCI Express Enhance Capability Header	RO	32'hB001001E
0xA04	L1_SUB_CAP_1	31:0	L1 PM Substates Capability Register	See PCIe Spec	32'h0028001F
0xA08	L1_SUB_CAP_2	31:0	L1 PM Substates Control 1 Register	See PCIe Spec	32'h0
0xA0C	L1_SUB_CAP_3	31:0	L1 PM Substates Control 2 Register	See PCIe Spec	32'h28

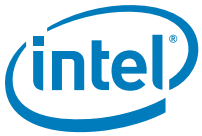
4.3.19 Precision Time Management Extended Capability

The Precision Time Measurement (PTM) Capability is an optional Extended Capability for discovering and controlling the distribution of a PTM Hierarchy. In Thunderbolt it implemented Upstream Port and it controls the PTM behavior of Upstream and Downstream Ports in PCIE Switch. Figure 30 details the structure of register fields PTM Capability registers and Table 107 describes the registers' fields.

Figure 30. PTM Extended Capability Structure

Table 107. PTM Extended Capability Registers

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0xB00	PTM_CAP_0	31:0	PCI Express Enhance Capability Header	RO	32'hC001001F
0xB04	PTM_CAP_1	31:0	PTM Capability Register	See PCIe Spec	32'h0
0xB08	PTM_CAP_2	31:0	PTM Control Register	See PCIe Spec	32'h0



4.4 xHCI Memory Mapped Address Space Registers

4.4.1 Host Controller Capability Registers

Table 108. CAPLENGTH - Capability Registers Length

Address Offset:0h
Default Value:80h
Access: RW/L;
Size:8 bits
This register is modified and maintained by BIOS

Bit	Access	Default Value	RST/PWR	Description
7:0	RW/L	80h	Core	Capability Registers Length (CAPLENGTH):

Table 109. HCIVERSION - Host Controller Interface Version Number

Address Offset:2-3h
Default Value:0100h
Access: RO;
Size:16 bits
This register is modified and maintained by BIOS

Bit	Access	Default Value	RST/PWR	Description
15:0	RO	0100h	Core	Host Controller Interface Version Number (HCIVERSION):

Table 110. HCSPARAMS1 - Structural Parameters 1

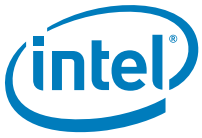
Address Offset:4-7h
Default Value:15000820h
Access: RW/L;
Size:32 bits
This register is modified and maintained by BIOS

Bit	Access	Default Value	RST/PWR	Description
31:24	RW/L	MaxPorts	Core	Number of Ports (MaxPorts): The value in this field reflects the highest numbered port in the controller, not the actual count of the number of ports. This allows for gaps in the port numbering, between USB2 and USB3 protocol capabilities.
23:19	RW/L	0h	Core	Reserved
18:8	RW/L	MaxInts	Core	Number of Interrupters (MaxInt):
7:0	RW/L	MaxSlots	Core	Number of Device Slots (MaxSlots):

Note: (Not for EDS) MaxPorts may vary depending upon the fuse settings that control the number of USB2 and USB3 ports in a given SKU.

Table 111. HCSPARAMS2 - Structural Parameters 2

Address Offset:8-Bh
Default Value:84000054h
Access: RW/L;
Size:32 bits



This register is modified and maintained by BIOS

Bit	Access	Default Value	RST/PWR	Description
31:27	RW/L	Ceiling (MaxSlots/ 2) +2 Bits4:0	Core	Max Scratchpad Buffers Lo (MaxScratchpadBufs):
26	RW/L	1h	Core	Scratchpad Restore (SPR):
25:21	RW/L	Ceiling (MaxSlots/ 2) +2 Bits9:5	Core	Max Scratchpad Buffers Hi (MaxScratchpadBufs):
20:8	RW/L	0h	Core	Reserved
7:4	RW/L	5h	Core	Event Ring Segment Table Max (ERSTMax):
3:0	RW/L	4h	Core	Isochronous Scheduling Threshold (IST):

Table 112. HCSPARAMS3 - Structural Parameters 3

Address Offset:C-Fh
Default Value:00040001h
Access: RW/L;
Size:32 bits
This register is modified and maintained by BIOS

Bit	Access	Default Value	RST/PWR	Description
31:16	RW/L	4h	Core	U2 Device Exit Latency (U2DEL):
15:8	RW/L	0h	Core	Reserved
7:0	RW/L	1h	Core	U1 Device Exit Latency (U1DEL):

Table 113. HCCPARAMS1 - Capability Parameters1

Address Offset:10-13h
Default Value:200071E9h
Access: RW/L;
Size:32 bits
This register is modified and maintained by BIOS

Bit	Access	Default Value	RST/PWR	Description
31:16	RW/L	2000h/ 2008h*	Core	xHCI Extended Capabilities Pointer (xECP): The Default value should be 2008h if NumUSB2 = 0
15:12	RW/L	7h	Core	Maximum Primary Stream Array Size (MaxPSASize):
11	RW/L	0b	Core	Contiguous Frame ID Capability (CFC)
10	RW/L	1b	Core	Stopped EDLTA Capabilty (SEC).
9	RW/L	1b	Core	Stopped - Short Packet Capability (SPC).
8	RW/L	1h	Core	Parse All Event Data (PAE)
7	RW/L	1h	Core	No Secondary SID Support (NSS):
6	RW/L	1h	Core	Latency Tolerance Messaging Capability (LTC):
5	RW/L	0h	Core	Light HC Reset Capability (LHRC):
4	RW/L	0h	Core	Port Indicators (PIND):
3	RW/L	0h	Core	Port Power Control (PPC):
2	RW/L	0h	Core	Context Size (CSZ):
1	RW/L	0h	Core	BW Negotiation Capability (BNC):
0	RW/L	1h	Core	64-bit Addressing Capability (AC64):

Table 114. DBOFF - Doorbell Offset

Address Offset:14-17h
Default Value:00003000h

Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:2	RO	C00h	Core	Doorbell Array Offset (DBAO):
1:0	RO	0h	Core	Reserved

Table 115. RTSOFF - Runtime Register Space Offset

Address Offset:18-1Bh
Default Value:00002000h
Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:5	RO	100h	Core	Runtime Register Space Offset (RTRSO):
4:0	RO	0h	Core	Reserved

Table 116. HCCPARAMS2 - Capability Parameters2

Address Offset:1C-1Fh
Default Value:0000002Ch
Access: RW/L;
Size:32 bits
This register is modified and maintained by BIOS

Bit	Access	Default Value	RST/PWR	Description
31:7	RW/L	0h	Core	Reserved
6	RW/L	0b	Core	Extended TBC Capability (ETC) - RO. This bit indicates if the TBC field in an Isoch TRB supports Burst Counts greater than 4. When this bit is 1, the Isoch TRB TD Size/TBC field presents the TBC value, and the TBC/RsvdZ field is RsvdZ. When this bit is 0, the TD Size/TCB field presents the TD Size value, and the TBC/RsvdZ presents the TBC value. This capability shall be enabled only of LEC = 1.
5	RW/L	1b	Core	Configuration Information Capability (CIC) - RO. This bit indicates if the xHC supports extended Configuration Information. When this bit is 1, the Configuration Value, Interface Number, and Alternate Setting fields in the Input Control Context are supported. When this bit is 0, the extended Input Control Context fields are not supported. Refer to section 6.2.5.1 for more information.
4	RW/L	0b	Core	Large ESIT Payload Capability (LEC) - RO. This bit indicates whether the xHC supports ESIT Payloads greater than 48K bytes. When this bit is '1', ESIT Payloads greater than 48K bytes are supported. When this bit is '0', ESIT Payloads greater than 48K bytes are not supported. Refer to section 6.2.3.8 for more information.
3	RW/L	1b	Core	Compliance Transition Capability (CTC) - RO. This bit indicates whether the xHC USB3 Root Hub ports support the Compliance Transition Enabled (CTE) flag. When this bit is '1', USB3 Root Hub port state machine transitions to the Compliance substate shall be explicitly enabled software. When this bit is '0', USB3 Root Hub port state machine transitions to the Compliance substate are automatically enabled. Refer to section 4.19.1.2.4.1 for more information.

Bit	Access	Default Value	RST/PWR	Description
2	RW/L	1b	Core	Force Save Context Capability (FSC) - RO. This bit indicates whether the xHC supports the Force Save Context Capability. When this bit is '1', the Save State operation shall save any cached Slot, Endpoint, Stream or other Context information to memory. Refer to Implementation Note "FSC and Context handling by Save and Restore", and sections 4.23.2 and 5.4.1 for more information.
1	RW/L	0b	Core	Configure Endpoint Command Max Exit Latency Too Large Capability (CMC) - RO. This bit indicates whether a Configure Endpoint Command is capable of generating a Max Exit Latency Too Large Capability Error. When this bit is '1', a Max Exit Latency Too Large Capability Error may be returned by a Configure Endpoint Command. When this bit is '0', a Max Exit Latency Too Large Capability Error shall not be returned by a Configure Endpoint Command. This capability is enabled by the CME flag in the USBCMD register. Refer to sections 4.23.5.2 and 5.4.1 for more information.
0	RW/L	1b	Core	U3 Entry Capability (U3C) - RO. This bit indicates whether the xHC Root Hub ports support port Suspend Complete notification. When this bit is '1', PLC shall be asserted on any transition of PLS to the U3 State. Refer to section 4.15.1 for more information.

4.4.2 Host Controller Operational Registers

Table 117. USBCMD - USB Command

Address Offset:80-83h
Default Value:00000000h
Access: RW; RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:15	RO	0h	Core	Reserved
14	RW	0b	Core	Extended TCB Enable (ETE). This flag indicates that the host controller implementation is enabled to support Transfer Burst Count values greater than 4 in Isoch TDs. This bit may be set only if ETC = 1.
13:12	RO	0h	Core	Reserved
11	RW	0h	Core	Enable U3 MFINDEX Stop (EU3S):
10	RW	0h	Core	Enable Wrap Event (EWE):
9	RW	0h	Core	Controller Restore State (CRS):
8	RW	0h	Core	Controller Save State (CSS):
7	RW	0h	Core	Light Host Controller Reset (LHCRST):
6:4	RO	0h	Core	Reserved
3	RW	0h	Core	Host System Error Enable (HSEE):
2	RW	0h	Core	Interrupter Enable (INTE):
1	RW	0h	Core	Host Controller Reset (HCRST):
0	RW	0h	Core	Run/Stop (RS):

Table 118. USBSTS - USB Status

Address Offset:84-87h

Default Value:00000001h
Access: RO; RW1C;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:13	RO	0h	Core	Rsvd3 (Rsvd3):
12	RO	0h	Core	Host Controller Error (HCE): HC does no set this bit.
11	RO	0h	Core	Controller Not Ready (CNR): HC does not set this bit
10	RW1C	0h	Core	Save/Restore Error (SRE):
9	RO	0h	Core	Restore State Status (RSS):
8	RO	0h	Core	Save State Status (SSS):
7:5	RO	0h	Core	Reserved
4	RW1C	0h	Core	Port Change Detect (PCD):
3	RW1C	0h	Core	Event Interrupt (EINT):
2	RW1C	0h	Core	Host System Error (HSE):
1	RO	0h	Core	Reserved
0	RO	1h	Core	HCHalted (HCH):

Table 119. PAGESIZE - Page Size

Address Offset:88-8Bh
Default Value:00000001h
Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:16	RO	0h	Core	Reserved
15:0	RO	1h	Core	Page Size (PAGESIZE):

Table 120. DNCTRL - Device Notification Control

Address Offset:94-97h
Default Value:00000000h
Access: RO; RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:16	RO	0h	Core	Reserved
15:0	RW	0h	Core	Notification Enable (N0_N15):

Table 121. CRCR_LO - Command Ring Low

Address Offset:98-9Bh
Default Value:00000000h
Access: RW; RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:6	RW	0h	Core	Command Ring Pointer (CRP):
5:4	RO	0h	Core	Reserved
3	RO	0h	Core	Command Ring Running (CRR):
2	RW1S	0h	Core	Command Abort (CA):
1	RW1S	0h	Core	Command Stop (CS):
0	RW	0h	Core	Ring Cycle State (RCS):

Table 122. CRCR_HI - Command Ring High

Address Offset:9C-9Fh
Default Value:00000000h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:0	RW	0h	Core	Command Ring Pointer (CRP):

Table 123. DCBAAP_LO - Device Context Base Address Array Pointer Low

Address Offset:B0-B3h
Default Value:00000000h
Access: RW; RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:6	RW	0h	Core	Device Context Base Address Array Pointer (DCBAAP):
5:0	RO	0h	Core	Reserved

Table 124. DCBAAP_HI - Device Context Base Address Array Pointer High

Address Offset:B4-B7h
Default Value:00000000h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:0	RW	0h	Core	Device Context Base Address Array Pointer (DCBAAP):

Table 125. CONFIG - Configure

Address Offset:B8-BBh
Default Value:00000000h
Access: RO; RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:10	RO	0h	Core	Reserved
9	RW	0h	Core	Configuration Information Enable (CIE):
8	RW	0h	Core	U3 Entry Enable (U3E):
7:0	RW	0h	Core	Max Device Slots Enabled (MaxSlotsEn):

Table 126. PORTSCXUSB2 - Port X Status and Control USB2 (X: 1 ... NumUSB2)

Address Offset: Port 1: 480-483h; repeated for each additional USB2 port as described below.
Default Value:000002A0h
Access: RO; RWS; RW;
Size:32 bits

Chassis Restore: S0iX (Regular)
Restore Group: VNNAON

There are NumUSB2 USB2 PORTSC registers at offsets :
480h, 490h, ... (480h + (NumUSB2-1)*10h)
The USB PORTSC registers should be accessed via DW writes for any modification.
Byte Writes have unintended behavior.

Bit	Access	Default Value	RST/PWR	Description
31	RW1S	0h	SUS	Warm Port Reset (WPR):

Bit	Access	Default Value	RST/PWR	Description
30	RW/L	0h	Core	Device Removable (DR):
29:28	RO	0h	Core	Reserved
27	RWS	0h	SUS	Wake on Over-current Enable (WOE):
26	RWS	0h	SUS	Wake on Disconnect Enable (WDE):
25	RWS	0h	SUS	Wake on Connect Enable (WCE):
24	RO	0h	SUS	Cold Attach Status (CAS):
23	RW1CS	0h	SUS	Port Config Error Change (CEC):
22	RW1CS	0h	SUS	Port Link State Change (PLC):
21	RW1CS	0h	SUS	Port Reset Change (PRC):
20	RW1CS	0h	SUS	Over-current Change (OCC):
19	RW1CS	0h	SUS	Warm Port Reset Change (WRC):
18	RW1CS	0h	SUS	Port Enabled Disabled Change (PEC):
17	RW1CS	0h	SUS	Connect Status Change (CSC):
16	RW	0h	SUS	Port Link State Write Strobe (LWS):
15:14	RWS	0h	SUS	Port Indicator Control (PIC):
13:10	RO	0h	SUS	Port Speed (Port_Speed):
9	RWS	1h	SUS	Port Power (PP):
8:5	RWS	5h	SUS	Port Link State (PLS):
4	RW1S	0h	SUS	Port Reset (PR):
3	RO	0h	SUS	Over-current Active (OCA):
2	RO	0h	Core	Reserved
1	RW1CS	0h	SUS	Port Enabled Disabled (PED):
0	RO	0h	SUS	Current Connect Status (CCS):

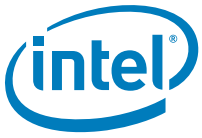
Table 127. PORTPMSCXUSB2 - Port X Power Management Status and Control USB2 (X: 1 … NumUSB2)

Address Offset: Port 1 484-487h
Default Value:00000000h
Access: RO; RW; RWS;
Size:32 bits
There are 6 USB2 PORTPMSC registers at offsets:
 484h, 494h, ... (484h + (NumUSB2-1)*10h)

Bit	Access	Default Value	RST/PWR	Description
31:28	RWS	0h	SUS	Port Test Control (PTC) :
27:17	RO	0h	SUS	Reserved
16	RW	0h	SUS	Hardware LPM Enable (HLE):
15:8	RWS	0h	SUS	L1 Device Slot (L1DS):
7:4	RWS	0h	SUS	Host Initiated Resume Duration (HIRD) :
3	RWS	0h	SUS	Remote Wake Enable (RWE):
2:0	RO	0h	SUS	L1 Status (L1S):

Table 128. PORTHLPMX - Port X Hardware LPM Control Register (X: 1 … NumUSB2)

Address Offset:Port 1 48C-48Fh
Default Value:00000000h
Access: RO; RWS; RW;
Size:32 bits
There are PORTHLPM registers at offsets :
48Ch, 49Ch, ... (48Ch + (NumUSB2-1)*10h)
This register is reset only by platform hardware during cold reset or in response to a Host Controller Reset (HCRST).



The definition for the fields depend on the protocol supported. For USB3 this register is reserved and shall be treated by software as RsvdP. For USB2 the definition is given below. Fields contain parameters necessary for xHC to automatically generate an LPM Token to the downstream device.

Bit	Access	Default Value	RST/PWR	Description
31:14	RO	0h	Core	RESERVED
13:10	RW	0h	SUS	Host Initiated Resume Duration-Deep (HIRDD): System software sets this field to indicate to the recipient device how long the xHC will drive resume if an exit from L1. The HIRDD value is is encoded as follows: 0h: 50 us (default) 1h: 125 us 2h: 200 us ... Fh: 1.175ms The value of 0h is interpreted as 50 us. Each incrementing value adds 75 us to the previous value.
9:2	RWS	0h	SUS	L1 Timeout (L1TO): Timeout value for L1 inactivity timer. This field shall be set to 00h by assertion of PR to '1'. Following are permissible values: 00h: 128 us (default) 01h: 256 us. ... FFh: 65,280us
1:0	RWS	0h	SUS	Host Initiated Resume Duration Mode (HIRDM): Indicates which HIRD value should be used. Following are permissible values: 0: Initiate L1 using HIRD only time out (default) 1: Initiate HIRDDon timeout. If rejected by device, initiate L1 using HIRD 2,3: Reserved

Table 129. PORTSCXUSB3 - Port X Status and Control USB3 (X: 1 ... NumUSB3)

Address Offset: See Below
Default Value:000002A0h
Access: RO; RWS; RW;
Size:32 bits

Chassis Restore: S0iX (Regular)
Restore Group: VNNAON

The USB3 PORTSC registers are at offsets:
First USB3 port: 480h+NumUSB2*10h
Next USB3 port : First USB3 Port + 10h
and so on...

Final USB3 Port : First USB3 Port + (NumUSB3-1)*10h)
The USB PORTSC registers should be accessed via DW writes for any modification.
Byte Writes have unintended behavior.

Bit	Access	Default Value	RST/PWR	Description
31	RW1S	0h	SUS	Warm Port Reset (WPR):
30	RW/L	0h	Core	Device Removable (DR):
29:28	RO	0h	Core	Reserved
27	RWS	0h	SUS	Wake on Over-current Enable (WOE):

Bit	Access	Default Value	RST/PWR	Description
26	RWS	0h	SUS	Wake on Disconnect Enable (WDE):
25	RWS	0h	SUS	Wake on Connect Enable (WCE):
24	RO	0h	SUS	Cold Attach Status (CAS):
23	RW1CS	0h	SUS	Port Config Error Change (CEC):
22	RW1CS	0h	SUS	Port Link State Change (PLC):
21	RW1CS	0h	SUS	Port Reset Change (PRC):
20	RW1CS	0h	SUS	Over-current Change (OCC):
19	RW1CS	0h	SUS	Warm Port Reset Change (WRC):
18	RW1CS	0h	SUS	Port Enabled Disabled Change (PEC):
17	RW1CS	0h	SUS	Connect Status Change (CSC):
16	RW	0h	SUS	Port Link State Write Strobe (LWS):
15:14	RWS	0h	SUS	Port Indicator Control (PIC):
13:10	RO	0h	SUS	Port Speed (Port_Speed):
9	RWS	1h	SUS	Port Power (PP):
8:5	RWS	5h	SUS	Port Link State (PLS):
4	RW1S	0h	SUS	Port Reset (PR):
3	RO	0h	SUS	Over-current Active (OCA):
2	RO	0h	Core	Reserved
1	RW1CS	0h	SUS	Port Enabled Disabled (PED):
0	RO	0h	SUS	Current Connect Status (CCS):

Table 130. PORTPMSCX - Port X Power Management Status and Control USB3(X: 1 … NumUSB3)

Address Offset: See Below
Default Value:00000000h
Access: RO; RW; RWS;
Size:32 bits
The USB3 PORTPMSC registers are at offsets:

First USB3 port: 484h+NumUSB2*10h

Next USB3 port : First USB3 Port + 10h

and so on...

Final USB3 Port : First USB3 Port + (NumUSB3-1)*10h)

Bit	Access	Default Value	RST/PWR	Description
31:17	RO	0h	Core	Reserved
16	RW	0h	SUS	Force Link PM Accept (FLA):
15:8	RWS	0h	SUS	U2 Timeout (U2TO):
7:0	RWS	0h	SUS	U1 Timeout (U1TO):

Table 131. PORTLIX - Port X Link Info USB3 (X: 1 … NumUSB3)

Address Offset:See Below
Default Value:00000000h
Access: RO;
Size:32 bits
The USB3 PORTLI registers are at offsets:

First USB3 port: 488h+NumUSB2*10h

Next USB3 port : First USB3 Port + 10h

and so on...

Final USB3 Port : First USB3 Port + (NumUSB3-1)*10h)

Bit	Access	Default Value	RST/PWR	Description
31:16	RO	0h	Core	Reserved
15:0	RO	0h	Core	Link Error Count (LEC):

4.4.3 Host Controller Runtime Registers

Table 132. MFINDEX - Microframe Index

Address Offset:2000-2003h
Default Value:00000000h
Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:14	RO	0h	Core	Rsvd1 (Rsvd1):
13:0	RO	0h	Core	Microframe Index (MI):

Table 133. IMANx - Interrupter x Management

Address Offset:2020-2023h, 2040-2043h,...,2020+(MaxInts-1)*20h-2023+(MaxInts-1)*20h
Default Value:00000000h
Access: RO; RW; RW1C;
Size:32 bits
There are MaxInts IMAN registers.
x = 1, ..., MaxInts

Bit	Access	Default Value	RST/PWR	Description
31:2	RO	0h	Core	Rsvd1 (Rsvd1):
1	RW	0h	Core	Interrupt Enable (IE):
0	RW1C	0h	Core	Interrupt Pending (Interrupt Pending):

Table 134. IMODx - Interrupter x Moderation

Address Offset:2024-2027h, 2044-2047h, ..., 2024+(MaxInts-1)*20h-2027+(MaxInts-1)*20h
Default Value:00000FA0h
Access: RW;
Size:32 bits
There are MaxInts IMOD registers.
x = 1, ..., MaxInts

Bit	Access	Default Value	RST/PWR	Description
31:16	RW	0h	Core	Interrupt Moderation Counter (IMODC):
15:0	RW	0FA0h	Core	Interrupt Moderation Interval (IMODI):

Table 135. ERSTSZx - Event Ring Segment Table Size x

Address Offset:2028-202Bh, 2048-204Bh, ..., 2028+(MaxInts-1)*20h-202B+(MaxInts-1)*20h
Default Value:00000000h
Access: RO; RW;
Size:32 bits
There are MaxInts ERSTSZ register.
x = 1, ..., MaxInts

Bit	Access	Default Value	RST/PWR	Description
31:16	RO	0h	Core	Rsvd1 (Rsvd1):
15:0	RW	0h	Core	Event Ring Segment Table Size (ERSTS):

Table 136. ERSTBA_LOx - Event Ring Segment Table Base Address Low x

Address Offset:2030-2033h, 2050-2053h, ..., 2030+(MaxInts-1)*20h-2033+(MaxInts-1)*20h
Default Value:00000000h
Access: RO; RW;
Size:32 bits
There are MaxInts ERSTBA_LO registers
x = 1, ..., MaxInts

Bit	Access	Default Value	RST/PWR	Description
31:6	RW	0h	Core	Event Ring Segment Table Base Address Register (ERSTBA_LO):
5:0	RO	0h	Core	Rsvd1 (Rsvd1):

Table 137. ERSTBA_HIx - Event Ring Segment Table Base Address High x

Address Offset:2034-2037h, 2054-2057h, ..., 2034+(MaxInts-1)*20h-2037+(MaxInts-1)*20h
Default Value:00000000h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:0	RW	0h	Core	Event Ring Segment Table Base Address (ERSTBA_HI):

Table 138. ERDP_LOx - Event Ring Dequeue Pointer Low x

Address Offset:2038-203Bh, 2058-205Bh, ..., 2038+(MaxInts-1)*20h-203B+(MaxInts-1)*20h
Default Value:00000000h
Access: RW; RW1C;
Size:32 bits
There are MaxInts ERDP_LO registers.
x = 1, ...,MaxInts

Bit	Access	Default Value	RST/PWR	Description
31:4	RW	0h	Core	Event Ring Dequeue Pointer (ERDP):
3	RW1C	0h	Core	Event Handler Busy (EHB):
2:0	RW	0h	Core	Dequeue ERST Segment Index (DESI):

Table 139. ERDP_HIx - Event Ring Dequeue Pointer High x

Address Offset:203C-203Fh, 205C-205Fh, ..., 203C+(MaxInts-1)*20h-203F+(MaxInts-1)*20h
Default Value:00000000h
Access: RW;
Size:32 bits
There are MaxInts ERDP_HI registers.
x = 1, ..., MaxInts

Bit	Access	Default Value	RST/PWR	Description
31:0	RW	0h	Core	Event Ring Dequeue Pointer (ERDP):

4.4.3.1 Doorbell Registers

Table 140. DOORBELL1 - Door Bell 1, 2, ..., 32

Address Offset:3000-3003h, 3004-3007h, ..., 307C-307Fh
Default Value:00000000h
Access: RW; RO; RD back always 0
Size:32 bits

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Bit	Access	Default Value	RST/PWR	Description
31:16	RW	0h	Core	DB Stream ID (DBSID):
15:8	RO	0h	Core	Rsvd1 (Rsvd1):
7:0	RW	0h	Core	DB Target (DBT):

4.4.4 Host Controller Extended Capability Registers

Table 141. Summary of Extended Capabilities

Capability	ID	Start	End	Cap. Size	Valid Length
USB2 Supported Protocol Capability	2d	8000h	801Bh	7 DW	7 DW
USB3.1 Supported Protocol Capability	2d	8020h	806Fh	20 DW	12 DW
Intel Vendor Defined Capability	192d	8070h	846Bh	255DW	71 DW
USB Legacy Support Capability	1d	846Ch	84F3h	34 DW	2 DW
Intel Vendor Defined Capability (Port Disable Override Capability)	198d	84F4h	84FFh	3 DW	3 DW
Intel Vendor Defined Capability (HW State Access)	199d	8500	85FFh	64DW	5 DW
Intel Vendor Defined Capability (Chicken bit mirror from PCI Config)	194d	8600h	86FFh	64 DW	64 DW
USB Debug Capability	10d	8700h	873Fh	16 DW	16 DW
Intel Vendor Defined Capability (Debug Device Config)	195d	8740h	87FFh	48 DW	7 DW
Intel Vendor Defined Capability (SSIC Policy and Implementation specific Registers)	196d	8800h	88FFh	64 DW	TBD
Intel Vendor Defined Capability (SSIC local and remote registers)	197d	8900h	8C33h	205 DW	(1 + (68 * NumSSICPorts)) DW upto 3 SSIC ports
Intel Vendor Defined Capability (EP Type Based Port Lock)	200d	8CFCh	8E0Fh	68 DW	(4+Maxports) DW
Intel Vendor Defined Capability (Global Time Synch.)	201d	8E10h	8E27h	6 DW	6 DW
Intel Vendor Defined Capability (Dublin Policy Registers)	202d	8E58h	8E8Fh	36 DW	29 DW
Intel Vendor Defined Capability (VTIO Registers)	203d	9000h	902Fh	12 DW*	12 DW

Note: *VTIO capability needs to be in its own 4K Page and is not shared with any other Capability

4.4.4.1 Supported Protocol Extended Capability

Table 142. Speed ID Mapping

Prot. Capability	Default Speed ID Value	Definition	Bit Rate	Protocol	Equivalent PSI Dword values			
					PLT	PFD	PSIE	PSIM
USB2 Capability	1	Full Speed	12 Mb/s	USB 2.0	0	0	2	12
	2	Low Speed	1.5 Mb/s	USB 2.0	0	0	1	1500
	3	High Speed	480 Mb/s	USB 2.0	0	0	2	480
USB3.1 Capability	4	Super Speed	5 Gb/s	USB 3.0	0	1	3	5
	5	Super Speed Plus	10 Gb/s	USB 3.0	0	1	3	10
	6	SSIC-G1A-L1	1.248 Gb/s	USB 3.0	0	1	2	1248
	7	SSIC-G2A-L1/ SSIC-G1A-L2	2.496 Gb/s	USB 3.0	0	1	2	2496
	8	SSIC-G3A-L1/ SSIC-G2A-L2/ SSIC-G1A-L4	4.992 Gb/s	USB 3.0	0	1	2	4992
	9	SSIC-G1B-L1	1.4576 Gb/s	USB 3.0	0	1	2	1457
	10	SSIC-G2B-L1/ SSIC-G1B-L2	2.9152 Gb/s	USB 3.0	0	1	2	2915
	11	SSIC-G3B-L1/ SSIC-G2B-L2/ SSIC-G1B-L4	5.8304 Gb/s	USB 3.0	0	1	2	5830

Table 8 HS-BURST: RATE Series and GEARs

RATE A-series (Mbps)	RATE B-series[1] (Mbps)	High-Speed GEARs
1248	1457.6	HS-G1 (A/B)
2496	2915.2	HS-G2 (A/B)
4992	5830.4	HS-G3 (A/B)

Table 143. XECP_SUPP_USB2_0 - XECP_SUPP_USB2_0

Address Offset:8000-8003h
Default Value:Varies based on SKU
Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:24	RO	2h	Core	USB Major Revision: 2.0
23:16	RO	0h	Core	USB Minor Revision
15:8	RO	8h / 10h*	Core	Next Capability Pointer Not for EDS: This value changes based on SKU.
7:0	RO	2h	Core	Supported Protocol ID

Note: If a SKU exists where all USB3 ports are disabled, or if NumUSB3=0, then the Next Capability Pointer above is set to 10h.

Table 144. XECP_SUPP_USB2_1 - XECP_SUPP_USB2_1

Address Offset:8004-8007h
Default Value:20425355h
Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:00	RO	20425355h	Core	XECP_SUPP_USB2_1 (XECP_SUPP_USB2_1) : Namestring USB

Table 145. XECP_SUPP_USB2_2 - XECP_SUPP_USB2_2

Address Offset:8008-800Bh
Default Value:30090F01h
Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:28	RO	3h	Core	Protocol Speed ID Count: 3 USB 2.0 Speed (High, Full, Low)
27:21	RO	0h	Core	Rsvd0 (Rsvd0) :
20	RW/L	1h	Core	BESL LPM Capability (BLC) - Bit is set to '1' to indicate that the the ports described by this xHCI Supported Protocol Capability will apply BESL timing to BESL and BESLD fields of the PORTPMSC and PORTHLPMC registers. This field can be modified and maintained by BIOS under Access Control
19	RW/L	1h	Core	Protocol Defined - Hardware LMP Capability (HLC) : This field can be modified and maintained by BIOS under Access Control
18	RO	0h	Core	Protocol Defined - Integrated Hub Implementation (IHI) :
17	RO	0h	Core	Protocol Defined - High SPeed Only (HSO) :
16	RO	1h	Core	Reserved
15:8	RW/L	NumUSB2	Core	Compatible Port Count: Note (Not for EDS): The compatible port count varies based upon SKU - controlled by the USB2 Port Config Fuse This field can be modified and maintained by BIOS under Access Control
7:0	RO	1h	Core	Compatible Port Offset :

Note: "Compatible Port Count" will vary depending upon the fuse settings that control the number of USB2 ports in a given SKU

Table 146. XECP_SUPP_USB2_3 - XECP_SUPP_USB2_3

Address Offset:800C-800Fh
Default Value:0h
Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:5	RO	0h	Core	Reserved
4:0	RO	0h	Core	Protocol Slot Type

Table 147. XECP_SUPP_USB2_4 - XECP_SUPP_USB2_4 (Full Speed)

Address Offset:8010-8013h
Default Value:000C0021h

Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:16	RO	Ch	Core	Protocol Speed ID Mantissa (PSIM)
15:9	RO	0h	Core	Rsvd0 (Rsvd0)
8	RO	0h	Core	PSI Full Duplex (PFD)
7:6	RO	0h	Core	PSI Type (PLT)
5:4	RO	2h	Core	Protocol Speed ID Exponent (PSIE)
3:0	RO	1h	Core	Protocol Speed ID Value (PSIV)

Table 148. XECP_SUPP_USB2_5 - XECP_SUPP_USB2_5 (Low Speed)

Address Offset:8014-8017h
Default Value:05DC0012h
Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:16	RO	05DCh	Core	Protocol Speed ID Mantissa (PSIM)
15:9	RO	0h	Core	Rsvd0 (Rsvd0)
8	RO	0h	Core	PSI Full Duplex (PFD)
7:6	RO	0h	Core	PSI Type (PLT)
5:4	RO	1h	Core	Protocol Speed ID Exponent (PSIE)
3:0	RO	2h	Core	Protocol Speed ID Value (PSIV)

Table 149. XECP_SUPP_USB2_6 - XECP_SUPP_USB2_6 (High Speed)

Address Offset:8018-801Bh
Default Value:01E00023h
Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:16	RO	1E0h	Core	Protocol Speed ID Mantissa (PSIM)
15:9	RO	0h	Core	Rsvd0 (Rsvd0)
8	RO	0h	Core	PSI Full Duplex (PFD)
7:6	RO	0h	Core	PSI Type (PLT)
5:4	RO	2h	Core	Protocol Speed ID Exponent (PSIE)
3:0	RO	3h	Core	Protocol Speed ID Value (PSIV)

Table 150. XECP_SUPP_USB3_0 - XECP_SUPP_USB3_0

Address Offset:8020-8023h
Default Value:03000802h
Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:24	RO	3h	Core	USB Major Revision: 3.0
23:16	RO	1h	Core	USB Minor Revision: 0.1
15:8	RO	14h	Core	Next Capability Pointer
7:0	RO	2h	Core	Supported Protocol ID

Table 151. XECP_SUPP_USB3_1 - XECP_SUPP_USB3_1

Address Offset:8024-8027h
Default Value:20425355h

Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:00	RO	20425355h	Core	XECP_SUPP_USB3_1 (XECP_SUPP_USB2_1) : Namestring USB

Table 152. XECP_SUPP_USB3_2 - XECP_SUPP_USB3_2

Address Offset:8028-802Bh
Default Value:10000610h
Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:28	RO	8h	Core	Protocol Speed ID Count
27:16	RO	0h	Core	Rsvd0 (Rsvd0) :
15:8	RO	NumUSB3	Core	Compatible Port Count : (Not for EDS): The compatible port count varies based on SKU - controlled by the USB3 Port config fuses
7:0	RO	NumUSB2+1	Core	Compatible Port Offset:

Note: (Not for EDS) "Compatible Port Count" will vary depending upon the fuse settings that control the number of USB3 ports in a given SKU

Table 153. XECP_SUPP_USB3_3 - XECP_SUPP_USB3_3

Address Offset:802C-802Fh
Default Value: 0h
Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:5	RO	0h	Core	Reserved
4:0	RO	0h	Core	Protocol Slot Type

Table 154. XECP_SUPP_USB3_4 - XECP_SUPP_USB3_4 (Super Speed)

Address Offset:8030-8033h
Default Value:00050134h
Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:16	RO	5h	Core	Protocol Speed ID Mantissa (PSIM)
15:9	RO	0h	Core	Rsvd0 (Rsvd0)
8	RO	1h	Core	PSI Full Duplex (PFD)
7:6	RO	0h	Core	PSI Type (PLT)
5:4	RO	3h	Core	Protocol Speed ID Exponent (PSIE)
3:0	RO	4h	Core	Protocol Speed ID Value (PSIV)

Table 155. XECP_SUPP_USB3_5 - XECP_SUPP_USB3_5 (Super Speed Plus)

Address Offset:8034-8037h
Access: RO;

Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:16	RO	Ah	Core	Protocol Speed ID Mantissa (PSIM)
15:9	RO	0h	Core	Rsvd0 (Rsvd0)
8	RO	1h	Core	PSI Full Duplex (PFD)
7:6	RO	0h	Core	PSI Type (PLT)
5:4	RO	3h	Core	Protocol Speed ID Exponent (PSIE)
3:0	RO	5h	Core	Protocol Speed ID Value (PSIV)

Table 156. XECP_SUPP_USB3_6 - XECP_SUPP_USB3_6 (SSIC-G1A-L1)

Address Offset:8038-803Bh
Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:16	RO	4E0h	Core	Protocol Speed ID Mantissa (PSIM)
15:9	RO	0h	Core	Rsvd0 (Rsvd0)
8	RO	1h	Core	PSI Full Duplex (PFD)
7:6	RO	0h	Core	PSI Type (PLT)
5:4	RO	2h	Core	Protocol Speed ID Exponent (PSIE)
3:0	RO	6h	Core	Protocol Speed ID Value (PSIV)

Table 157. XECP_SUPP_USB3_7 - XECP_SUPP_USB3_7 (SSIC-G2A-L1/SSIC-G1A-L2)

Address Offset:803C-803Fh
Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:16	RO	9C0h	Core	Protocol Speed ID Mantissa (PSIM)
15:9	RO	0h	Core	Rsvd0 (Rsvd0)
8	RO	1h	Core	PSI Full Duplex (PFD)
7:6	RO	0h	Core	PSI Type (PLT)
5:4	RO	2h	Core	Protocol Speed ID Exponent (PSIE)
3:0	RO	7h	Core	Protocol Speed ID Value (PSIV)

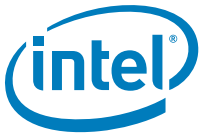
Table 158. XECP_SUPP_USB3_8 - XECP_SUPP_USB3_8 (SSIC-G3A-L1/SSIC-G2A-L2/SSIC-G1A-L4)

Address Offset:8040-8043h
Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:16	RO	1380h	Core	Protocol Speed ID Mantissa (PSIM)
15:9	RO	0h	Core	Rsvd0 (Rsvd0)
8	RO	1h	Core	PSI Full Duplex (PFD)
7:6	RO	0h	Core	PSI Type (PLT)
5:4	RO	2h	Core	Protocol Speed ID Exponent (PSIE)
3:0	RO	8h	Core	Protocol Speed ID Value (PSIV)

Table 159. XECP_SUPP_USB3_9 - XECP_SUPP_USB3_9 (SSIC-G1B-L1)

Address Offset:8044-8047h



Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:16	RO	5B1h	Core	Protocol Speed ID Mantissa (PSIM)
15:9	RO	0h	Core	Rsvd0 (Rsvd0)
8	RO	1h	Core	PSI Full Duplex (PFD)
7:6	RO	0h	Core	PSI Type (PLT)
5:4	RO	2h	Core	Protocol Speed ID Exponent (PSIE)
3:0	RO	9h	Core	Protocol Speed ID Value (PSIV)

Table 160. XECP_SUPP_USB3_10 - XECP_SUPP_USB3_10

Address Offset:8048-804Bh
Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:16	RO	B63h	Core	Protocol Speed ID Mantissa (PSIM)
15:19	RO	0h	Core	Rsvd0 (Rsvd0)
8	RO	1h	Core	PSI Full Duplex (PFD)
7:6	RO	0h	Core	PSI Type (PLT)
5:4	RO	2h	Core	Protocol Speed ID Exponent (PSIE)
3:0	RO	Ah	Core	Protocol Speed ID Value (PSIV)

Table 161. XECP_SUPP_USB3_11 - XECP_SUPP_USB3_11 (SSIC-G3B-L1/SSIC-G2B-L2/ SSIC-G1B-L4)

Address Offset:804C-804Fh
Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:16	RO	16C6h	Core	Protocol Speed ID Mantissa (PSIM)
15:9	RO	0h	Core	Rsvd0 (Rsvd0)
8	RO	1h	Core	PSI Full Duplex (PFD)
7:6	RO	0h	Core	PSI Type (PLT)
5:4	RO	2h	Core	Protocol Speed ID Exponent (PSIE)
3:0	RO	Bh	Core	Protocol Speed ID Value (PSIV)

4.4.4.2 Vendor Defined Capability (Chicken Bits)

Table 162. HOST_CTRL_CAP_REG - Host Controller Capability

Address Offset:8070-8073h
Default Value:0000B0C0h
Access: RW;
Size:32 bits
This register is not subject to HW save and restore.

Bit	Access	Default Value	RST/PWR	Description
31:24	RW/L	00h	Core	Reserved

Bit	Access	Default Value	RST/PWR	Description
23:16	RW/L	45h	Core	Save Length Indicates the number of DWords in this capability starting at 8090h, that need to be saved and restored This value needs to be updated as new chicken bit registers are added. 45h -> 81A7h is the last valid byte to be saved
15:8	RW/L	FFh	Core	Next Capability Pointer
7:0	RW/L	C0h	Core	Supported Protocol ID

Table 163. HOST_CLR_MASK_REG - Override EP Flow Control

Address Offset:8078-807Bh
Default Value:00000000h
Access: WO, RD back always 0;
Size:32 bits
This register is not subject to HW save and restore.

Bit	Access	Default Value	RST/PWR	Description
31:10	RO	0h	Core	RESERVED
9:5	WO	0h	Core	5bits of slot number as a default configuration. It can scale to max of 128 slots
4:1	WO	0h	Core	4bits of EP number
0	WO	0h	Core	This is a register that is used to clear the internal scheduler's mask that is used to stop scheduling a particular EP. Bit0 indicates the direction of the EP

Table 164. HOST_CLR_IN_EP_VALID_REG - Clear Active IN EP ID Control

Address Offset:807C-807Fh
Default Value:00000000h
Access:WO, Read back to 0;
Size:32 bits
This register is not subject to HW save and restore.

Bit	Access	Default Value	RST/PWR	Description
31:0	WO	0h	Core	Clear Active IN EP ID Control (HOST_CLR_IN_EP_VALID_REG): This register is used to clear the internal valid IN EP array that TRM stored in order to guarantee one IN EP per port. This register allows software to clear the valid bit of each port IN EP. This field indicates the port number. For a 2port configuration, only bit1:0 are valid. It can scale for the max number of ports that we support.

Table 165. HOST_CLR_PMASK_REG - Clear Poll Mask Control

Address Offset:8080-8083h
Default Value:00000000h
Access: WO, Read back to 0;
Size:32 bits
This register is not subject to HW save and restore.

Bit	Access	Default Value	RST/PWR	Description
31:10	RO	0h	Core	RESERVED

Bit	Access	Default Value	RST/PWR	Description
9:5	WO	0h	Core	5bits of slot number as a default configuration. It can scale to max of 128 slots
4:1	WO	0h	Core	4bits of EP number
0	WO	0h	Core	This is a register that is used to clear the internal scheduler's poll mask that is used to indicate whether we need to poll this EP. This is used for USB2. Bit0 indicates the direction of the EP

Table 166. HOST_CTLR_OCRD_REG - Port Credit Control

Address Offset:8084-8087h
Default Value:00000000h
Access: WO, Read back to 0;
Size:32 bits
Not for EDS
This register is not subject to HW save and restore.

Bit	Access	Default Value	RST/PWR	Description
31	WO	0h	Core	Write 1 to force XFER state return to IDLE
30	WO	0h	Core	Write 1 to force CPL state return to IDLE
29	WO	0h	Core	Add one credit to a port
28	WO	0h	Core	Subtract one credit from a port
27:8	RO	0h	Core	RESERVED
7:0	WO	0h	Core	This is a register that is used to add or subtract a per port credit or to control the TRM's XFER and CPL states. port number

Table 167. HOST_CTRL_TEST_BUS_LO - Test Bus Low

Address Offset:8088-808Bh
Default Value:00000000h
Access: RO;
Size:32 bits
Not for EDS
This register is not subject to HW save and restore.

Bit	Access	Default Value	RST/PWR	Description
31:0	RO	0h	Core	Test Bus Low (HOST_CTRL_TEST_BUS_LO): Host controller test bus low 32bits. This is used to read the internal states and other important signals. The host control test bus is gathered from different internal modules for its important states and control/status information. We have a 64bits register that allows us to read a bus of 64bits

Table 168. HOST_CTRL_TEST_BUS_HI - Test Bus High

Address Offset:808C-808Fh
Default Value:00000000h
Access: RO;
Size:32 bits
Not for EDS
This register is not subject to HW save and restore.

Bit	Access	Default Value	RST/PWR	Description
31:0	RO	0h	Core	Test Bus High (HOST_CTRL_TEST_BUS_HI): Host controller test bus high 32bits. This is used to read the internal states and other important signals. The host control test bus is gathered from different internal modules for its important states and control/status information. We have a 64bits register that allows us to read a bus of 64bits

Table 169. HOST_CTRL_TRM_REG - Host Control Transfer Manager (TRM)

Address Offset:8090-8093h
Default Value:4C1BD105h
Access: RW;
Size:32 bits
This register contains fields which control the behavior of the Transfer Manager in the XHC. The functions controlled by this register are made available largely for debug/diagnostic purposes. This configurability is above and beyond that defined in the xHCI specification.
NOT for EDS

Bit	Access	Default Value	RST/PWR	Description
31	RW	0h	Core	Reserved. It must set to 0.
30	RW	1h	Core	1: Enables a special function which we will detect NAK received and go into a single packet pace mode so that we don’t burst ahead. 0: Disables this function.
29	RW	0h	Core	1: Disables the error check for Data Move stream state. It will generate a transfer event with prime PIPE error completion code if error detected. 0: Enable the error check.
28	RW	0h	Core	1: Disables the error check for prime PIPE stream state. It will generate a transfer event with prime PIPE error completion code if error detected. 0: Enable the error check.
27	RW	1h	Core	This bit has been modified for its usage since PPTA0. It is used to allow NO-OP TRB to be treated in a same way as link TRB. In other words, it will update the internal context when it is fetched while the internal context cache TRB FIFO is empty. 1: enabled the cache function 0: disable the function
26	RW	1h	Core	This is a special internal condition enable for CPL engine which it enables all EP halt conditions detected to cause the proper actions in a response. 1: enabled 0: disabled Note: only default condition of 1 is validated.

Bit	Access	Default Value	RST/PWR	Description
25	RW	0h	Core	This is a special internal branch condition control in XFER engine which does the EP transfer ring process. When this bit is set, a retry condition identified by completion engine will cause XFER engine to stop what it is currently in progress and start over from state IDLE. 1: enabled the branch condition 0: disabled.
24	RW	0h	Core	This is a special internal branch condition control in XFER engine which does the EP transfer ring process. When this bit is set, the XFER will not continue even if the next TRB is identified as a non DMA TRB. The engine will then wait for the next scheduled request for this EP. 1: enabled the branch condition 0: disabled.
23	RW	0h	Core	When ERDP register is updated by software, it is expected as an atomic function since this is a 64bit register. It is expected that the ERDP (64bits register) is updated together when ERDP high 32 is written. We have this bit designed to ignore the atomic operation required from software for ERDP low 32bits. When this bit is set to 1, it will update the ERDP low 32bits when software issues a CPU write to the ERDP low 32 bit. 1: ignore atomic operation 0: not ignore.
22	RW	0h	Core	Setting this bit to 1 will force an internal doorbell ring on the EP that it has received a response.
21	RW	0h	Core	0: Drop ERDYs received when not in a flow control state. 1: Do not drop ERDYs received when not in a flow control state. Note: We typically drop unexpected ERDY
20	RW	1h	Core	0: Disable timeout of TRB error processing. 1: Enable timeout of a TRB processing in few critical states that possibly have a deadlock for unexpected reason. A vendor defined completion code is generated in the event of a timeout during TRB processing.
19	RW	1h	Core	This big is modified to enable a feature where we can control whether or not to report an event with completion code of Missed Service Error when a short packet response has been received not in the expected service interval. 1: enables all completion event that supposedly is short to the MSE. 0: Disable this function so that the xHC engine will report an event of with Short packet indication and another event with MSE at the end of the TD.
18	RW	0h	Core	This bit is modified to enable the NOOP TRB as a TD when Missing Service Interval Error has encountered. This is only for PPT B0, LPT and CB. 1: enabled 0: disabled

Bit	Access	Default Value	RST/PWR	Description
17	RW	1h	Core	Enable a special branch condition of the XFER ring process state. This is to ensure that we have a DMA request issued to DMA engine during a PHASE1 process of the TTE. 1: enabled 0: disabled
16	RW	1h	Core	0: Disable error reporting for this case. 1: Enable error reporting if a SETUP TRB contains the following: bRequest = SET_ADDRES bmRequestType = (DTD) Host-to-device, Type = Standard, & Recipient = Device
15	RW	1h	Core	Enables a special internal state branch condition for periodic EP during its transfer ring process. If we have identified that the next TRB is a non DMAnable TRB such as LINK TRB, or Event data TRB, then this bit enables XFER engine to continue process the next TRB as if the ENT bit of the TRB is set. 1: enable 0: disable
14	RW	1h	Core	XFER engine has a new function that provides a support to ISO EP within a long PCIe delayed system. The long delay can cause missing service interval while pending response has not all been returned. This bit enables engine to identify a MSI condition and stored the context bit for a pending response so that we can process a MSI event when pending response received. 1: enables this function 0: disable this function
13	RW	0h	Core	0: Bulk and interrupt endpoints use burst size defined by endpoint context. 1: Force the Bulk and Interrupt endpoints use a burst size of 1.
12	RW	1h	Core	0: ENT bit is ignored. 1: ENT bit is processed. The transfer engine will service the next TRB.
11	RW	0h	Core	Setting this bit to 1 will force the transfer engine to set the packet boundary flag. This flag is an important flag which may cause a deadlock. This is a safety feature that we pluged in.
10	RW	0h	Core	This bit is modified to support PPTB0, LPT and CP for a feature that we will clear the single IN EP array based on ISO flush or short flush. 0: Indicate that we do not need to clear IN EP array based on flush conditions. 1: indicate that we do clear IN EP array based on flush conditions
9	RW	0h	Core	Setting this bit to 1 will force the transfer engine state machine to exit the CPL_WAIT state. This is designed to avoid unexpected deadlock in CPL_WAIT state.
8	RW	1h	Core	0: Disable internal TRB cache invalidation. 1: Enable internal TRB cache invalidation auto detect function This will allow engine to handle more than 4TRBs per packet.

Bit	Access	Default Value	RST/PWR	Description
7	RW	0h	Core	0: USB3 responses with NumPkts equal to 0 will be treated as a flow control condition. 1: USB3 responses with NumPkts equal to 0 will not be treated as a flow control condition.
6	RW	0h	Core	0: Babble errors will not disable the port. 1: Babble errors will disable the auto detect function This will allow engine to handle more than 4TRBs per packet.
5	RW	0h	Core	Enable a function which we can clear mask of an EP on any response of that EP. 0: Clear the scheduler mask normally. 1: Clear the scheduler mask on each received packet.
4	RW	0h	Core	This bit is designed to allow XFER engine to do a transfer without checking against the available port credit. 0: Advertises accurate buffer credit information to the scheduler. 1: Advertises non-zero buffer credits to the scheduler. (e.g. never backpressure back on buffer credit information)
3	RW	0h	Core	0: Process stalls reported by the DMA engine. 1: Ignore stall response received reported by the DMA engine.
2	RW	1h	Core	This bit is added for bug FR4836. It is to ring internal doorbell on that EP (applies to USB2 HS Bulk OUT and Control EPs) that receives NYET response. 1: Enable the feature 0 : Disabled
1	RW	0h	Core	0: obay the NPKT0 and EOB flow control. 1: Ignore received flow control for implied NRDY (e.g EOB or NPKT=0) for USB3 only
0	RW	1h	Core	0: Disable TD pacing for IN endpoint. 1: Enable TD pacing for IN endpoints.

Table 170. HOST_CTRL_SCH_REG - Host Control Scheduler

Address Offset:8094-8097h
Default Value:00008100h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31	RW	0h	Core	disable repeat scheduler service of usb2 periodic
30:27	RW	0h	Core	enable scheduler limiter functions to block async. traffic types across ports while periodic pending.
26	RW	0h	Core	enable pkt pending notification to usb3 ports
25	RW	0h	Core	disable async. burst limitation while periodic in progress
24	RW	0h	Core	disable marking overlap flag on all TT periodic INs.
23	RW	0h	Core	disable blocking of async. scheduling while periodic active to same port
22	RW	0h	Core	Setting this bit enables pipelining of multiple OUT EPs (across diff ports). This will help boost the performance for multiple ports OUT test case.

Bit	Access	Default Value	RST/PWR	Description
21	RW	0h	Core	enable “strobe” method of USB2 port periodic done check (off by default)
20:13	RW	0h	Core	TTE Host Control
31:22	RW	0h	Core	Scheduler: Reserved
21	RW	0h	RW	Scheduler: Enable Stop serving packets to disabled port
20:17	RW	0h	Core	TTE: Reserved
16	RW	0h	Core	disable deferred split error request on speculative IN with data payload and no TRB.
15	RW	1h	Core	TTE: disable split error request w/NULL pointer on speculative INs with data payload and no TRB.
14	RW	0h	Core	TTE: Disable checking of missed microframes
13	RW	0h	Core	TTE: Disable interrupt complete split limit to 3 micro frames
12:11	RW	0h	Core	Cmd Mgr: Cache size control reg 0: 64 1: 32 2,3: 16
10:9	RW	0h	Core	Cmd Mgr: Allow dynamically setting different max EP allowed. The max EP supported scales with the scratch pad size. This allows driver to allocate small memory sizes if it needed. 0: 32 eps 1: 16 eps 2: 8 eps 3: 4 eps
8	RW	1h	Core	Cmd Mgr: Enables scratch pad function
7	RW	0h	Core	Scheduler: enable check to stop scheduling on port that are not connected
6	RW	0h	Core	Scheduler: disable 1 pack scheduling limit when ISO pending in present microframe
5:4	RW	0h	Core	Scheduler: scheduler sort pattern 00 (default) search ISO ahead of interrupt within each service interval 01 - search USB2-ISO, USB3-ISO, USB2-Interrupt, USB3-Interrupt within each service interval 10 - search strictly by interval 11 - search all ISO intervals ahead interrupt intervals and within each interval, USB2 ahead of USB3
3	RW	0h	Core	Scheduler: enable TTE overlap prevention on interrupt OUT EPs (at cost of possible service interval slip)
2	RW	0h	Core	Scheduler: enable TTE overlap prevention on interrupt IN EPs (at cost of possible service interval slip)
1	RW	0h	Core	Scheduler: Deisable TRM active IN EP valid check function
0	RW	0h	Core	Scheduler: Disable poll delay function

Table 171. HOST_CTRL_ODMA_REG - Host Control ODMA

Address Offset:8098-809Bh
Default Value:14003002h
Access: RO; RW;
Size:32 bits
This register contains a number of fields that provide a specific level of configurability for the OUT DMA. Engine in the XHC. This configurability is above and beyond that defined in the xHCI specification.

NOT for EDS

Bit	Access	Default Value	RST/PWR	Description
31:24	RW	14h	Core	The value in this field dictates the wait time (in u-seconds) between retries initiated from the Set Address Finite State Machine
23	RW	0h	Core	RESERVED
22	RW	0h	Core	This bit controls the b2b write (with-in pkt) capability of IDMA DM engine. 0 : b2b write is enabled 1 : b2b write is disabled
21	RW	0h	Core	This bit controls the de-coupling of Context+CPL actions from DataMover Handler. 0 : De-couple Context Processing + CPL Engine handshake from DataMover Handler 1 : Disable de-coupling of Context Processing + CPL Engine handshake From DataMover Handler (Old mode)
20	RW	0h	Core	This bit adds the pipe stage in CPL Engine handshake to de-couple CPL Engine handshake from the Control logic. 0 : De-couple CPL Engine handshake from the control logic (DataMover or Context Handler) 1 : Disable de-coupling CPL Engine handshake from the control logic (DataMover or Context Handler)
19	RW	0h	Core	Reserved
18	RW	0h	Core	Setting this field will enable ACK FIFO credit accounting. ODMA will ensure that ample room exists in the ACK FIFO for expected device responses prior to initiating a given DP
17	RW	0h	Core	Setting this field will backpressure the Set Address Finite State Machine based on the availability of ACK FIFO credits
16	RW	0h	Core	Setting this field will disable the enforced wait time between retries initiated from the Set Address Finite State Machine
15	RW	0h	Core	Setting this field will prohibit ODMA from automatically dropping all deferred packets received on ISOCHRONOUS endpoints
14	RW	0h	Core	Setting this field will immediately force an EP timeout on all outstanding EPs on a given port when a port disconnect is detected
13	RW	1h	Core	Setting this field will enable ACK FIFO individual credit accounting mechanisms for Async vs. Periodic Endpoints. ODMA will ensure that ample room exists in the ACK FIFO for expected device responses prior to initiating a given DP
12	RW	1h	Core	0: Employs a 1us EP Transaction Base Timer. Enables a Timeout range from 16us to 64us 1: Employs a 125us EP Transaction Base Timer. Enables a Timeout range from 2ms to 8ms
11	RW	0h	Core	Setting this field will prohibit the Set Address Finite State Machine Credit Handshake with TTE Logic
10	RW	0h	Core	Setting this field will disable the EP Transaction Timer function when the Command Manager is performing a Stop Endpoint Command or when the LTSSM is in Recovery

Bit	Access	Default Value	RST/PWR	Description
9	RW	0h	Core	Setting this field prohibits the Set Address Finite State Machine from being flow controlled when an ACK with NPKT=0 is received in response to the SETUP DP initiated during SET_ADDRESS
8	RW	0h	Core	Setting this field generates a pulse that clears the ownership of the context semaphore that is shared between the Out DMA Response and Completion Finite State Machines
7	RW	0h	Core	Setting this field generates a pulse that implicitly returns all of the Out DMA ACK credits on all ports
6	RW	0h	Core	Setting this field generates a pulse that returns the Out DMA Set Address Finite State Machine into the IDLE state
5	RW	0h	Core	Setting this field generates a pulse that returns the Out DMA Completion Finite State Machine into the IDLE state
4	RW	0h	Core	Setting this field generates a pulse that returns the Out DMA Response Finite State Machine into the IDLE state
3	RW	0h	Core	Setting this field generates a pulse that returns the Out DMA Read Finite State Machine into the IDLE state
2:1	RW	1h	Core	Controls the duration of the EP Transaction Timeout (depends on the setting of bit[12]) 0: 64us ([12]=0) or 8ms ([12]=1) EP Transaction Timeout 1: 32us ([12]=0) or 4ms ([12]=1) EP Transaction Timeout 2: 16us ([12]=0) or 2ms ([12]=1) EP Transaction Timeout 3: EP Transaction Timer is DISABLED
0	RW	0h	Core	0: Enables the EP Transaction Timeout Function 1: Disables the EP Transaction Timeout Function

Table 172. HOST_CTRL_IDMA_REG - Host Control IDMA

Address Offset:809C-809Fh
Default Value:00000402h
Access: RW;
Size:32 bits
This register contains a number of fields that provide a specific level of configurability for the IN DMA. Engine in the XHC. This configurability is above and beyond that defined in the xHCI specification.
NOT for EDS

Bit	Access	Default Value	RST/PWR	Description
31	RW	0h	Core	HCRST WDT Enable Setting this bit will enable the WDT for HC Reset flow.
30	RW	0h	Core	Setting this field will allow the Event Manager to treat either Transfer Manger (when 1) or Completion Engine (when 0) Event requests with higher priority.
29	RW	0h	Core	Setting this field will allow the Doorbell Manager to post events on a given transfer ring
28:26	RW	0h	Core	RESERVED
25	RW	0h	Core	Setting this field will cause the TTE Address FIFO to flush when bit[18] is strobed.

Bit	Access	Default Value	RST/PWR	Description
24	RW	0h	Core	0: Flush the Asynchronous Address FIFO when bit[18] is strobed 1: Flush the Periodic Address FIFO when bit[18] is strobed
23:19	RW	0h	Core	The value in this field indicates the port number of the address FIFO to flush when bit[18] is strobed
18	RW	0h	Core	Setting this field will generate a strobe causing a give Periodic or Asynchronous Address FIFO to flush. FIFO flushed is a function of bits [25:19]
17	RW	0h	Core	0: All response acknowledges (ACKs) are put in the periodic header FIFO in XPPE 1: Only periodic response acknowledges (ACKs) are put in the periodic header FIFO in XPPE
16	RW	0h	Core	0: Default IDMA Pointer Buffer Room to a default value of 8. Requires a strobe of bit[3] to take effect. 1: Default IDMA Pointer Buffer Room to a default value of 4. Requires a strobe of bit[3] to take effect.
15	RW	0h	Core	Setting this field will prohibit IDMA from automatically dropping received DPs when a given endpoint currently has no outstanding transactions
14	RW	0h	Core	Setting this field will prohibit IDMA from automatically dropping received DPs when a given endpoint is currently in a flow controlled state
13	RW	0h	Core	Setting this field will prohibit IDMA from automatically dropping all deferred packets received on ISOCHRONOUS endpoints
12	RW	0h	Core	Setting this field will immediately force an EP timeout on all outstanding EPs on a given port when a port disconnect is detected
11	RW	0h	Core	Setting this field will disable sequence number context checking when NRDY or STALL TP are received
10	RW	1h	Core	0: Employs a 1us EP Transaction Base Timer. Enables a Timeout range from 16us to 64us 1: Employs a 125us EP Transaction Base Timer. Enables a Timeout range from 2ms to 8ms
9	RW	0h	Core	Setting this field will disable the EP Transaction Timer function when the Command Manager is performing a Stop Endpoint Command or when the LTSSM is in Recovery
8	RW	0h	Core	Setting this field enables the Compliance Isochronous mode of operation. It bounds the upper limit on the NPKT field for all ISO Acknowledgments generated from the Host to the value of 2.
7	RW	0h	Core	Setting this field generates a pulse that clears the ownership of the context semaphore that is shared between the IN DMA Acknowledge and Data Mover Finite State Machines
6	RW	0h	Core	Setting this field generates a pulse that returns the IN DMA Data Mover Finite State Machine into the IDLE state
5	RW	0h	Core	Setting this field generates a pulse that returns the IN DMA Acknowledge Finite State Machine into the IDLE state
4	RW	0h	Core	Setting this field generates a pulse that implicitly returns all of the IN DMA Data Packet credits on all ports

Bit	Access	Default Value	RST/PWR	Description
3	RW	0h	Core	Setting this field generates a pulse that clears all the Read and Write Pointers associated with the various DMA Address FIFOs causing them to appear empty
2:1	RW	1h	Core	Controls the duration of the EP Transaction Timeout (depends on the setting of bit[10]) 0: 16us ([10]=0) or 2ms ([10]=1) EP Transaction Timeout 1: 32us ([10]=0) or 4ms ([10]=1) EP Transaction Timeout 2: 64us ([10]=0) or 8ms ([10]=1) EP Transaction Timeout 3: EP Transaction Timer is DISABLED
0	RW	0h	Core	0: Enables the EP Transaction Timeout Function 1: Disables the EP Transaction Timeout Function

Table 173. HOST_CTRL_PORT_CTRL - Global Port Control

Address Offset:80A0-80A3h
Default Value:0003F80Fh
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31	RW	0	Core	Overflow Error Detection Enable
30:12	RW	3h	Core	HBUF Water Mark
11	RW	1h	Core	CPL Cut Thru Enable
10:4	RW	0h	Core	Reserved
3:0	RW	Fh	Core	Reserved

Table 174. PMCTRL – Power Management Control

Address Offset:80A4-80A7h
Default Value:0h
Access: RW;
Size:32 bits
Chassis Restore: S0iX (Regular)
Restore Group: VNNAON

Bit	Access	Default Value	RST/PWR	Description
31	RW	0b	SUS	Async PME Source Enable This field allows the async PME source to be allowed to generate PME. This is specifically required for SOC's that do not allow for any clock other than RTC to be available during RTD3.
30	RW	0b	SUS	Legacy PME Source Enable This field allows the legacy PME source to be used in PME generation. The legacy source is in reference to the source prior to the RTD3 changes.

Bit	Access	Default Value	RST/PWR	Description
29	RW	0b	SUS	Reset Prep Power Gate Trigger Disable This field controls the actions taken for due to reset warn. 1 – Reset Warn will trigger a HW autonomous Power Gate 0 – Reset Warn will not trigger a HW autonomous Power Gate
28	WO	0b	SUS	Internal PME flag Clear This Write-Only bit can be used to clear the internal PME flag. SW write to '1' will clear the PME flag. SW write to '0' will have no effect and be ignored by the controller. Read always return '0'.
27	RW	0h	SUS	Disable D3 Power Gating without Save 0 - D3 Power Gating is enabled 1 - D3 Power Gating is disabled when Save is not done.
26	RW	0b	SUS	XLFPSCOUNTSRC (Source for LFPS OFF Counter) 0: Central RTC Counter for LFPS detection 1: Local Counter for LFPS detection
25	RW	0b	SUS	XELFPSRTC (Enable LFPS Filtering on RTC) 0: Use Oscillator clock for LFPS Filtering during P3 1: Use RTC Clock for LFPS Filtering during P3
24	RW	1b	SUS	XMPHYSPGDD0I2 (ModPhy Sus Well Power Gate Disable for D0I2) 0 : Modphy sus well power gating enabled 1 : Modphy sus well power gating disabled
23	RW	1b	SUS	XMPHYSPGDD0I3 (ModPhy Sus Well Power Gate Disable for D0I3) 0 : Modphy sus well power gating enabled 1 : Modphy sus well power gating disabled
22	RW	0b	SUS	XMPHYSPGDRTD3 (ModPhy Sus Well Power Gate Disable for RTD3) 0 : Modphy sus well power gating enabled 1 : Modphy sus well power gating disabled
21:18	RW	Bh	SUS	XD3RTCPTTM (D3 RTC Port Timer Tick Multiplier) This register will be the multiplication factor for determining SSIC Wake Detection Frequency and RXDET based on the " U3 LFPS Periodic Sampling OFF Time Control" value. If this field is 9h and this register is Bh, frequency for RXDET and SSIC H8EXIT detection while MODPHY SUS Power gating is enabled would be 99ms.
17	RW	0b	SUS	Reserved

Bit	Access	Default Value	RST/PWR	Description
16	RW	1b	SUS	SS AON LFPS Detector Enable This field controls the LFPS ownership between the gated and AON domain for the case when the controller is not power gated. 1: Allow the LFSP Detector in AON to own LFPS detection when the port is in PS3 for U2/U3 (not RxD) regardless of port ownership (i.e. AON owns U2/U3 exit for all PS3 U2/U3 exit). 0: Allow the LFPS Detector in AON to own the LFPS detection only when the AON owns the port and in U2/U3 (not RxD), otherwise the gated domain LFPS detector will handle U2/U3 wake.
15:8	RW	FFh	SUS	SS U3 LFPS Detection Threshold This field controls the threshold used to determine when a valid U3 Wake is detected through when using the unfiltered LFPS source. The value on this field will reflect the binary count required to have been detected on the counter being clocked by the unfiltered lfps source to result in a valid U3 wake detection. This field requires comprehension of the Source Clock or Raw LFPS detection.
7:4	RW	9h	SUS	U3 LFPS Periodic Sampling OFF Time Control This field controls the OFF time for the LFPS periodic sampling for USB3 Ports This field is also used for SSIC H8 Exit and RXDET Polling multiplying it with XD3RTCPTTM 0x0 – periodic sampling is disabled. 0x1 – OFF time is 1ms 0x2 – OFF time is 2ms …. 0xF – OFF time is 15ms A speed up mode shall be implemented where this field is in units of us. i.e. 0x1 = 1 us OFF time, 0x2 = 2 us OFF time, etc.
3	RW	0h	SUS	PS3 LFPS Source Select 0 – LFPS Source is unfiltered 1 – LFPS Source is filtered (Rx-Elec-Idle) LFPS Source is Rx-Elec-Idle for any non PS3 state.

Bit	Access	Default Value	RST/PWR	Description
2	RW	1h	SUS	XHCI Engine Autonomous Power Gate Exit Reset Policy Controls when the xHCI engine is brought out of reset due to a power ungate. 0 – Engine is brought out of reset when D3 to D0 is triggered. This allows for a quick power up sequence while leaving the virtual PCIe LTSSM in L23 is power ungate is not due to D3 to D0. 1 – Engine is brought out of reset along with the rest of the IP. This is required for PMC save/restore flow.
1	RW	0h	SUS	USB2 Port Wake Unit Coupling Policy Controls the trigger for USB3 Port Wake Units to initiate Port Level Power Off Preparation. 1 – RTD3 Triggered 0 – Port Triggered when in L1, L2 or Disabled, Disconnected
0	RW	0h	SUS	USB3 Port Wake Unit Coupling Policy Controls the trigger for USB3 Port Wake Units to initiate Port Level Power Off Preparation. 0 – RTD3 Triggered 1 – Port Triggered when in PS3 due to RxDetect, U3, U2 or Disabled

Table 175. PGCBCTRL – PGCB Control

Address Offset:80A8-80ABh
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:29	RW	0h	SUS	RESERVED FOR FUTURE USE
28	RW	0h	SUS	Power Gate Disable Override 0: When cleared, Power gating (D3, D0i3,D0i2) will be disabled until ACCTRL is set 1: When Set, Power gating is enabled even if ACCTRL is not set. IP-Inaccessible and Function Disable Powergating is not affected by ACCTRL.
27:26	RW	0h	SUS	RESERVED FOR FUTURE USE These bits were also used for following functionaliy for SPTLP, DNV, LBG, BXT* and AR, and the default value was "0h". KBPH onward, these bits are moved to 0x81C8 offset location. Bit-2 and bit-1 of IP-Inaccessible Hysteresis Timer 00_0 : 50us 00_1 : 100us 01_0 : 150us 01_1 : 200us 00_0 : 250us 00_1 : 300us 01_0 : 350us 11_1 : 400us

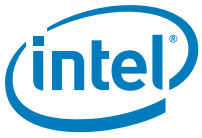
Bit	Access	Default Value	RST/PWR	Description
25:24	RW	1h	SUS	PGCB Force Clocks Off Ack to PGCB Power Stable count: cfg_trsvd1[1:0] For Warm Reset: Value representing the minimum number of delay clocks between "ip_pgcb_force_clocks_on_ack" de-assertion to PWRSTABLE Value decoding (in aux_clk) : '00': 1 clock '01': 2 clocks '10': 8 clocks '11': 256 clocks These bits were also used for following functionality for SPTLP, DNV, LBG, BXT* and AR, and the default value was "0h". KBPH onward, these bits are moved to 0x81C8 offset location. Bit-24 : Reset Prep Override Disable When cleared, will allow for reset prep to be ACK'ed regardless of the state of the controller i.e. controller may not have prepared for reset. When set, will require reset prep to be ACK'ed only when the controller has prepared for reset. Bit-25 : Bit '0' of IP-Inaccessible Hysteresis Timer 00_0 : 50us 00_1 : 100us 01_0 : 150us 01_1 : 200us 00_0 : 250us 00_1 : 300us 01_0 : 350us 11_1 : 400us

Bit	Access	Default Value	RST/PWR	Description
23:22	RW	1h	SUS	PGCB PG Ready Ack to PGCB Force Clocks De-assertion count: cfg_trsvd0[1:0] For Warm Reset: Value representing the minimum number of delay clocks between "pgcb_ip_pg_rd_ack_b" assertion to "pgcb_ip_force_clocks_on" de-assertion Value decoding (in aux_clk) : '00': 1 clock '01': 2 clocks '10': 8 clocks '11': 256 clocks These bits were also used for following functionality for SPTLP, DNV, LBG, BXT* and AR, and the default value was "0h". KBPH onward, these bits are moved to 0x81C8 offset location. CDH Aggregation Minimum Wait Time : This field controls the minimum time that we must wait for resets to propagate before allowing Power Up flow to complete. The Power Up flow requires special handling of clocks, reset and sleep signaling which requires the CDH to monitor reset propagation. This timer allow for flexibility on when we consider all resets propagated. 0h - Disabled 1h - 2 clocks 2h - 4 clocks 3h - 8 clocks 4h - 16 clocks 5h - 32 clocks 6h - 64 clocks 7h - 128 clocks

Bit	Access	Default Value	RST/PWR	Description
				PGCB POK Assertion to PGCB Reset De-assertion count: cfg_tpokup[1:0] For IP-inaccessible Exit: Value representing the minimum number of delay clocks between "pgcb_pok" assertion to "pgcb_force_rst_b" de-assertion. Value decoding (in aux_clk) : '00': 1 clock '01': 2 clocks '10': 8 clocks '11': 256 clocks These bits were also used for following functionality for SPTLP, DNV, LBG, BXT* and AR, and the default value was "3h". KBPH onward, these bits are moved to 0x81C8 offset location.
21:20	RW	1h	SUS	CDH Aggregation Minimum Wait Time : This field controls the minimum time that we must wait for resets to propagate before allowing Power Up flow to complete. The Power Up flow requires special handling of clocks, reset and sleep signaling which requires the CDH to monitor reset propagation. This timer allow for flexibility on when we consider all resets propagated. 0h - Disabled 1h - 2 clocks 2h - 4 clocks 3h - 8 clocks 4h - 16 clocks 5h - 32 clocks 6h - 64 clocks 7h - 128 clocks

Bit	Access	Default Value	RST/PWR	Description
19:18	RW	1h	SUS	PGCB POK De-assertion to PGCB Power Gate Ready ACK count: cfg_tpokdown[1:0] For IP-Inaccessible PG: Value representing the minimum number of delay clocks between "pgcb_pok" de-assertion to "pgcb_isol_latchen" de-assertion In our case, the "pgcb_isol_latchen" is only used/toggle when D0i2 state retention is enabled. For IP-Accessible PG: Doesn't get used. For WarmReset : Value representing the minimum number of delay clocks between "pgcb_pok" de-assertion to "pgcb_ip_pg_rdy_ack_b" Value decoding (in aux_clk) : '00': 1 clock '01': 2 clocks '10': 8 clocks '11': 256 clocks These bits were also used for following functionality for SPTLP, DNV, LBG, BXT* and AR, which KBPH onward got moved to 0x81C8 offset location. Bit-19 : CDH Reset Propagation Aggregation Control This bit will indicate the mode of operation for the CDH Reset Propagation Aggregator. It allows for a mode where the aggregation will wait for an indication from each CDH before proceeding OR ignore the CDH indication before proceeding. Regardless of the mode, the aggregator will enforce the CDH Aggregation Mini Wait Time. 0 - Aggregate all the CDH indications before triggering the CDH Aggregation Mini Wait Time. Once the Min Wait Time is met a notification to the Power Sequencer/Control will be initiated 1 - Trigger the CDH Aggregation Mini Wait Time w/o waiting for CDH indication. Once the Min Wait time is met a notification to the Power Sequencer/Control will be initiated. Bit-18 : MMP_PFET_REQ_OVRD This bit will disable the MMP PFET request condition for PGCB control. 1 - MMP PFET Request Ignored 0 - Default
17:16	RW	1h	SUS	PGCB Clock Gate Request to PGCB Sleep: cfg_tclkgate[1:0] Value representing the minimum number of delay clocks required between the assertion of "pgcb_ip_clkgate_b" to the deassertion of "pgcb_sleep" on PG exit. (This is only applicable for IP-Accessible PG with state-retention enabled.) Please see the description of cfg_tsleepact for more details.

Bit	Access	Default Value	RST/PWR	Description
15:14	RW	1h	SUS	PGCB Sleep Deassertion to PGCB ISM Unlock Req: cfg_tsleepinactiv[1:0] For IP-Accessible PG (with state retention): Value representing the minimum number of delay clocks required between the deassertion of "pgcb_sleep" to the deassertion of "pgcb_ip_*_lock_req_b". For IP-Inaccessible PG (or with state-retention disabled): Value representing the minimum number of delay clocks required between the deassertion of "pgcb_sleep" to the deassertion of "pgcb_isol_en_b".
13:12	RW	1h	SUS	PGCB Prim Reset Deassertion to PGCB Next State: cfg_tirstup[1:0] For IP-Accessible PG: Value representing the number of delay clocks required between the deassertion of "pgcb_force_prim_rst_b" to the assertion of "pgcb_ip_clkgate_req_b" (or the deassertion of "pgcb_ip_*_lock_req_b if state retention is disabled). For IP-Inaccessible PG: Value representing the number of delay clocks required between the deassertion of "pgcb_force_prim_rst_b" to the deassertion of "pgcb_pmc_save_req_b". Please see the description of cfg_tsleepact for more details.
11:10	RW	1h	SUS	PGCB Side Reset Deassertion to PGCB Prim Reset Deassertion: cfg_tsiderstup[1:0] Value representing the number of delay clocks required between the deassertion of "pgcb_force_rst_b" to the deassertion of "pgcb_force_prim_rst_b". (This is only applicable for IP-Accessible PG.) Please see the description of cfg_tsleepact for more details.
9:8	RW	1h	SUS	PGCB Latch Isolation High to PGCB Clock Ungate Request: cfg_tlatchen[1:0] Value representing the number of delay clocks required between the assertion of "pgcb_isol_latchen" to the deassertion of "pgcb_ip_clkgate_req_b". Please see the description of cfg_tsleepact for more details.
7:6	RW	1h	SUS	PGCB Isolation Deassertion to PGCB Latch Isolation High Count: cfg_tdeisolate[1:0] Value representing the minimum number of delay clocks required between the deassertion of "pgcb_isol_en_b" to the assertion of "pgcb_isol_latchen". Please see the description of cfg_tsleepact for more details.



Bit	Access	Default Value	RST/PWR	Description
5:4	RW	1h	SUS	PGCB Reset Assertion to PGCB Power Down Request Count: cfg_tresetact[1:0] For IP-Accessible PG (with state retention): Value representing the minimum number of delay clocks required between the assertion of "pgcb_force_prim_rst_b" (and "pgcb_force_rst_b") to the assertion of "pgcb_pmc_pg_req_b". For IP-Inaccessible PG (or with state-retention disabled): Value representing the minimum number of delay clocks required between the assertion of "pgcb_force_prim_rst_b" (and "pgcb_force_rst_b") to the assertion of "pgcb_sleep". Please see the description of cfg_tsleepact for more details.
3:2	RW	1h	SUS	PGCB Isolation Assertion to PGCB Reset Assertion Count: cfg_tisolate[1:0] Value representing the minimum number of delay clocks required between the assertion of "pgcb_isol_en_b" to the assertion of "pgcb_force_prim_rst_b" and "pgcb_force_rst_b". Please see the description of [1:0] for more details.
1:0	RW	1h	SUS	PGCB Sleep Assertion to PGCB Isolation Enable Count: cfg_tsleepact[1:0] For IP-Accessible PG (with state retention): Value representing the minimum number of delay clocks required between the assertion of "pgcb_sleep" (and the deassertion of "pgcb_isol_latchen") to the assertion of "pgcb_isol_en_b". For IP-Inaccessible PG (or with state-retention disabled): Value representing the minimum number of delay clocks required between the deassertion of "pgcb_isol_latchen" to the assertion of "pgcb_isol_en_b", as well as the minimum number of delay clocks required between the assertion of "pgcb_sleep" to the assertion of "pgcb_pmc_pg_req_b". Common for all cfg_t* inputs: '00': 1 clock '01': 2 clocks '10': 8 clocks '11': 256 clocks For any of the cfg_t* inputs that an IP may feel are a don't-care and the IP does not feel they will be useful for post-silicon debug, the recommendation is to tie the input to 2'b01 (2 clocks). Otherwise, the inputs may be tied to another relevant value or connected to a configuration register. Note: These signals may only change while pgcb_pwrupidle is asserted, if pgcb_pwrupidle is deasserted it should be valid and stable. (It may change the same cycle that ip_pgcb_pg_rdy_req_b asserts.)

Table 176. DEVIDLECTRL – Device Idle Control Register

Address Offset:80AC-80AFh
Access: RW;

Size:32 bits
Chassis Restore: S0iX (Regular)
Restore Group: VNNAON

Bit	Access	Default Value	RST/PWR	Description
31:4	RO	0h	SUS	RESERVED
4	RO	0h	SUS	Interrupt Request Capable (IRC): Set to '1' by HW if it is capable of generating an interrupt on command completion, else '0'.
3	RWC	1h	SUS	RR: RestoreRequired. When set (by HW), SW must restore state to the IP. The state may have been lost due to a reset or full power lost. SW clears the bit by writing a '1'. This bit will be set on initial power up.
2	RW	0h	SUS	DevIdle (DEVIDLE). SW sets this bit to '1' to move the function into the DevIdle state. Writing this bit to '0' will return the function to the fully active D0 state (D0i0)
1	RO	0h	SUS	IR: Interrupt Request. SW sets this bit to '1' to ask for an interrupt to be generated on completion of the command. SW must clear or set this on each write to this register.
0	RO	0h	SUS	CIP: Command-In-Progress. HW sets this bit on a 1->0 or 0->1 transition of bit [2]. While set, the other bits in this register are not valid and it is illegal for SW to write to any bit in this register. When clear all the other bits in the register are valid and SW may write to any bit. If Interrupt Request bit [1] was set for the current command, HW may clear this bit before the interrupt has been made visible to SW, since when SW actually handles a particular interrupt is not visible to the HW. SW writes to this bit have no effect.

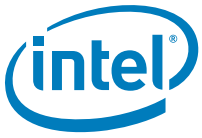
Table 177. HOST_CTRL_MISC_REG - Host Controller Misc Reg

Address Offset:80B0-80B3h
Default: 0h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31	RW	0h	Core	USB2 LTR Mechanism Disable This controls the inclusion of the USB2 LTR based on link state as defined in the LTR HAS. Setting this bit will disable USB2 LTR and will expose a NO Requirement from USB2 thus not impacting the aggregated LTR value for the controller.
30	RW	0h	Core	USB2 Line State Debounce During Port Reset Policy This register controls how the debounce is enforced during the Port Reset phase. 0 – do not enable the line state debounce during port reset. 1 – enable the line state debounce during port reset.

Bit	Access	Default Value	RST/PWR	Description
29	RW	0h	Core	TTE PEXE Credit Fix Disable When set, it disables a fix implemented to re-deem PEXE credits when a port is disconnected.
28	RW	0h	Core	TTE Scheduling Policy This register controls a fix made to prevent over-scheduling by not account for 188B in each uFrame. Setting this bit will disable the fix and allow for over-scheduling.
27	RW	0h	Core	USB3 ITP Delta Timer Source Select This register selects the source for the delta timer tracking used for ITP generation. 0 – the source is a 16.666 ns tick generated from a crystal reference clock 1 - the source is a 16.666 ns tick generated from the aux_cclk. This field needs to remain in sync with Frame Timer Source Select to ensure the are both set or both cleared. There is no support for any other combination.
26	RW	0h	Core	Frame Timer Source Select This register controls the source for the frame timer. 0 – the source for the frame timer is a crystal reference clock 1 – the source for the frame timer is the aux_cclk.
25	RW	0h	Core	uFrame Masking Enable If set, enables the uFrame tick to be masked due to ports being in U3/NC. This controls a fix made to disable the auto masking of uFrame tick due to port state w/o any pipeline idle condition. When cleared, we rely on gating of frame timer due to proper port state and idleness tracking from the pipeline.
24	RW	0h	Core	Late FID Check Disable This register disables the Late FID Check performed when starting an ISOCH stream.

Bit	Access	Default Value	RST/PWR	Description
23	RW	0h	Core	Late FID TTE Count Adjust Disable 0: The value of "Frame Late Skip Count" starts at "1" for TTE Endpoints and "0" for non-TTE Endpoints. This represents an adjustment for the number of SI missed. 1: The value of "Frame Late Skip Count" starts at "0" for both TTE Endpoints and non-TTE Endpoints. Bit 22='0' on this register negates the need for this adjustment. OLD DEF (NEED TO REMOVE) Alarm Set Flag Disable 0: Scheduler performing its "first-round" check on periodic endpoints will assert this flag if an alarm is set. If this flag is asserted, then the Scheduler will be allowed to set the nfirst flag for endpoints in the "second-round" check of periodic endpoints. This prevents a race condition where no wakeup alarm is set in the first round for a new endpoint and then the disable PLL shutdown signal is cleared in the second round due to the setting of nfirst. This would only happen if there was one periodic endpoint and only for new doorbell rings that result in the unmask array bit being set in the proximity of the transition between the first-round and the second-round. 1: (Chicken-bit operation) The flag is disabled Note: This bit was created for COE HSD 4796077.
22	RW	0h	Core	Late FID "Difference Calculation" Legacy 0: Late Frame-ID uses the new "Difference Calculation" to compute how may SI the TD is late. 1: Late Frame-ID uses the legacy "Difference Calculation" to compute how may SI the TD is late. OLD DEF (NEED TO REMOVE) Polling Doorbell Rang Disable 0: Polling State Machine will not move on from Bulk/ Control Endpoint until a DMA transfer is reported by the TRM. Polling State Machine behaves as if the Doorbell is still asserted. This prevents a TD consisting of a single Link TRB from consuming the scheduling opportunity for a NAK'd/NYET Endpoint after a new Doorbell and thus never waking the Link for the Doorbell. 1: (Chicken-bit operation) The flag is disabled. Note: This bit was created for COE HSD 4547808.
21	RW	0h	Core	ERDY Flag Disable 0: An ERDY received on any Interrupt Endpoint will force the backbone clock high until the next µframe to allow that Endpoint’s TRM Pending Mask to be cleared. 1: (Chicken-bit operation) The flag is disabled. Note: This bit was created for COE HSD 4903177 for CHV/ANS/SPTLP.



Bit	Access	Default Value	RST/PWR	Description
20	RW	0h	Core	Enable LTR DB Device Clear 1: TBD. This bit was created by Shweta K. 0: (Chicken-bit operation) Note: This bit was created for COE HSD 4796697,4796465
19	RW	0h	Core	USB2 Resume Cx Inhibit Disable Controls if USB2 L1 Resume is allowed to contribute to "DMA Active" which will inhibit Cx state. 0 – USB2 L1 Resume is allowed to inhibit Cx via "DMA Active" 1 – USB2 L1 Resume is NOT allowed to inhibit Cx via "DMA Active" When cleared, Cx will only be inhibited when the DMA traffic for the port begins.
18	RW	0b	Core	Late FID TTE Disable 0: Late Frame-ID Check is enabled for TTE Endpoints. 1: Late Frame-ID Check is disabled for TTE Endpoints. OLD DEF (NEED TO REMOVE) Extra uFrame This register controls the extra number of uFrames added onto the advancing of late FID check.
17	RW	0b	Core	Late FID uframe Check Disable 0: "Frame ID Match" only asserts in uframe=7 for non-TTE Endpoints (Frame before match). 1: "Frame ID Match" can assert in any uframe.
16	RW	0b	Core	Late FID Extra Interval [Index 0] This register controls the extra number of intervals added onto the advancing of late FID check. Essentially a bias used to correct for possible errors in implementation.
15:0	RW	37Fh (895d)	Core	Valid Isoch Scheduling Range This register defines the window in milliseconds from the current Frame that will be considered for scheduling in an upcoming Frame. Anything scheduled outside of this window will be considered as late and will trigger the Missed Service Error.

Table 178. HOST_CTRL_MISC_REG2 - Host Controller Misc Reg2

Address Offset:80B4-80B7h
Default: 0h
Access: RW;

Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:29	RW	0h	Core	Short Packet Advance Throttling 0 - Limit SPA to 4 TRB's 1 - Limit SPA to 16 TRB's 2 - limit SPA to 64 TRB's 3 - limit SPA to 128 TRB's 4 - limit SPA to 512 TRB's 5 - limit SPA to 1024 TRB's 6 - limit SPA to 2048 TRB's 7 - Disabled
28	RW	0h	Core	Disable Scheduler FrameID check – New policy to enable/ disable Scheduler's FrameID check capability. This mode is added as a part of adding CFC=1 capability. 0 – Enable Scheduler FrameID check 1 – Disable Scheduler FrameID check Note, this policy is only supported by the version of the controller that supports CFC=1 capability. Also, this policy should only be used when CFC=1 is enabled.
27	RW	0b	Core	Setting this bit will disable reporting "Isoc Buffer Overrun" event when Babble is detected in Isoc pipe, but instead the xHC will report Babble error.
26	RW	0h	Core	Setting this disable the fix added in TRM Engine to avoid the bug related to missing event for TTE Isoc EP when TRM Cache Invalidation for last pkt of the last TD.
25	RW	0b	Core	Disable clearing the USB2 and Periodic LTR tracking upon HCReset () 0 - Clear USB2 and Periodic LTR tracking upon HCReset 1 - Don't clear USB2 and Periodic LTR tracking upon HCReset. This is added as a part of COE bug fix for HSD #140409942.
24	RW	0b	Core	Disable dropping Scheduler request for the case where the doorbell for requested EP is not active when Scheduler initiates the request. 0 - Drop Scheduler request when Doorbell is NOT active. 1 - Always service the Scheduler request (Legacy behavior) This is added as a part of COE bug fix for HSD #1207912771.
23	RW	0b	Core	Disable dropping TTE request for the case where the doorbell for requested EP is not active when TTE Engine initiates the request. 0 - Drop TTE request when Doorbell is NOT active. 1 - Always service the TTE request (Legacy behavior) This is added as a part of COE bug fix for HSD #1207912771.

Bit	Access	Default Value	RST/PWR	Description
22	RW	0b	Core	Disabled Xfer Engine fix of not clearing EDTLA to prevent Stream Context EDTLA tracking bug. 0 - Xfer Engine will not clear EDTLA for normal transfer and will only allow to clear during advancing (Short Pkt, Missed Service etc). 1 - Xfer Engine will clear EDTLA when it detects the case where there is no ED at the end of the TD and hence no Accumulated Length tracking required (Legacy behavior). This is added as a part of COE bug fix for HSD #1403911591.
21:14	RW	0h	Core	Reserved
13	RW	0h	Core	Enable Hammock Harbor Frame Index Not Running 0: "Frame Index Not Incrementing" will not drive the BLIF (bytes left in frame) value to zero. Frame Index Not Incrementing is detected when either the clock request or clock acknowledgment are zero. 1: (Chicken-bit operation) "Frame Index Not Incrementing" will drive the BLIF value to zero. This bit applies to GEN2 and forward (Excluding Alpine Ridge). Note: This bit was created for COE HSD 1403966148
12	RW	0h	Core	Disable ODMA IDT fix Disabling the fix will revert to old behavior where new TRM request could be proceeded while Context update for IDT HDR is still in progress. This behavior could lead to data corruption issue if EP cache swapping is active around IDT handling. 0 - Enable the fix 1 - Disable the fix
11	RW	0h	Core	ODMA Context Ownership Release Control Bit (PING fix) - 0 = ODMA RESP State Machine will release the context ownership while sending header out. This allows CMPL State Machine to process completion while header is presented to the Port. 1 = ODMA RESP State Machine will hold on to the context ownership while sending header out. This blocks CMPL State Machine to process completion while header is presented to the Port.
10	RW	0h	Core	Disable IDMA CERR fix - Enabling the fix will reset CERR count upon good response 0 - Enable the fix 1 - Disable the fix
9	RW	0h	Core	100ms Watch Dog Timer When set, it will enable 100ms Watch Dog Timer for Aux PM FSM for phystatus assertion else watch dog timer is 300ms.
8	RW	0h	Core	Enable Watch Dog Timer When set, it will enable 100/300ms watch dog timer for AUX PM FSM for phystatus assertion.

Bit	Access	Default Value	RST/PWR	Description
7	RW	0h	Core	Enable/Disable SuperSpeedPlus Isoc Pipelining feature 1 - Enable the SSP isoc pipelining feature 0 - Disable sthe SSP isoc pipelining feature. When disable, the controller will treat SSP isoc EPs similar to SS isoc EPs.
6	RW	0h	Core	When set, it will ungate the trunk clock gating for PIPE clock when there is flush whe DBC/EXI HHH is not idle.
5	RW	0b	Core	Frame Timer Select This register defines the frame timer used for all frame timer derived ticks. 0 - Frame timer in the VNN is the source for all frame timer related tracking. 1 - Frame timer in the Gated VNN is the source for all frame timer related tracking.
4	RW	0h	Core	Clear CCS on CAS When set, XHCI port will not clear the CAS when CCS is set. (BUGDE 5076358)
3	RW	0h	Core	On Default - Enables Root Hub s/m to arc to DBC_DISCONNECTED from ERROR and RESET states if the reason to enter into those state was a prior connection failure to exchange Link Capabilities Set "1" - Keep the Root hub s/m in ERROR or RESET as the case may be , on a successful connection as a DBC if the first attempt was failed due to PortConfigTimeout
2	RW	0h	Core	Warm Port Reset on Disconnected Port Disable When set, disables the generation of a WPR on a disconnected port.
1:0	RW	0b	Core	RESERVED

Table 179. SSPE – Super Speed Port Enable

Address Offset:80B8-80BBh

Default Value:0h

Access: RW;
Size:32 bits
Chassis Restore: S0iX (Regular)
Restore Group: VNNAON

Bit	Access	Default Value	RST/PWR	Description
31	RW	0	SUS	Delay power down entry if Rx LFPS is active. Setting this bit will block the controller's power down entry seq (for Sx/D3/D0i2 etc) if Rx LFPS is active. The power down entry will happen once a device stops sending LFPS.
30	RW	0	SUS	Enable Clearing of CCS for HCReset - Setting this bit clears the USB3 port's PORTSC.CCS bit upon HCReset.
29	RW	0	SUS	Disable Raw Lfps Detection Based Wake from P3 This bit is used to disable RTL fix provided to separate RawLFPS and RxElecIDle detection 0: Transition port to RESUME based on raw LFPS detection 1 : Transition port to RESUME based Filtered RxElecIdle detection

Bit	Access	Default Value	RST/PWR	Description
28	RW	0	SUS	EXI Override Disable
27:NumUSB3	RO	0h	SUS	RESERVED
(NumUSB3-1):0	RW	1h	SUS	USB3 Port Enable This field controls whether SuperSpeed capability is enabled for a given USB3 port. When set to 1, Enables SS termination Enables PORTSC to to see the connects on the ports. When set to 0, Disables SS termination Blocks PORTSC from reporting attach/connect. Places port in the lowest power state.

Table 180. SSPITPE – Super Speed Port ITP Enable

Address Offset:80BC-80BFh
Default Value:0h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:NumUSB3	RO	0h	SUS	RESERVED
(NumUSB3-1):0	RW	All 1's	Core	ITP Transmit Enable Width is scaled with USB3 Port Count

Table 181. AUX_CTRL_REG - AUX Reset Control

Address Offset:80C0-80C3h
Default Value:015FC0F0h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31	WO	0h	Core	This allows software to fire a reset that is equivalent to fundamental reset. Using this bit should only be for debug/ test purpose. 1: normal 0: asserted one fundamental reset
30	RW	0h	Core	This will enable hc_rst to complete when OC is detected on a Port 0: Fix is enabled (Default) 1: Fix is Disabled
29	RW	0h	Core	This bit enables AUX reset control module to assert the pcie_phy_reset either from PIPE reset or from Aux power up reset only. The pcie_phy_reset is an internal signal for CB PHY only. 1: PIPE PHY reset 0: Aux PowerUp Reset

Bit	Access	Default Value	RST/PWR	Description
28	RW	0h	Core	This bit enables the AUX PM control module to assert mac_phy_powerdown state to P1 as soon as PERST# is deasserted. If disabled, then the AUX PM control state will follow its nature cause to determine the power down states for PIPE. 1: enabled 0: disabled
27	RW	0h	Core	This bit enables the internal reset control module to immediately start a reset assertion process when PERST# is deasserted without waiting for PCIe device is out of D3 state. This is for warm reboot only. The PERST# can still have impact as a reset if the xHC is in D3 and allow PERST# as a powerup reset bit set. 1: enabled PERST# as an immediately reset 0: disabled
26	RW	0h	Core	This bit disables the PERST# to cause an internal reset. 1: disabled the PERST# 0: enabled
25	RW	0h	Core	This bit enables a speed up function or AUX reset at startup. Normally we wait for 20ms after AUX power level has reached. When in speed up mode, we wait only around 3-4us. 1: enabled for fast sim 0: disabled
24	RW	1h	SUS	When set to 1 ignore a port reset that is caused by a USBport link went down.
23	RW	0h	SUS	When set to 1 ignore main powerup reset to USB PHY PIPE reset
22	RW	1h	SUS	When set to '1' allow software to fire a cold reset to USB port logic
21	RW	0h	SUS	When set to '1' ignore HC reset to reset the USB2 Port logic
20	RW	1h	SUS	When set to '1' ignore HC reset to the USB PHY power-on reset
19	RW	1h	SUS	When set to '1' enable the HC liked reset caused by PCIe link down condition detected. If PCIe link down detected, a link down reset will always be fired to PCIe core.
18	RW	1h	SUS	When set to '1' enable EEPROM reload on every main power-up
17	RW	1h	SUS	When set to '1' ignore HC reset to the PCIe PHY PIPE reset
16	RW	1h	SUS	When set to '1' ignore the LTSSM of USB link state transition caused reset to USB PHY PIPE reset
15	RW	1h	SUS	When set to '1' ignore warm reset of the portSC to the USB PHY power on reset
14	RW	1h	SUS	When set to '1' allow PCIe link down to cause a reset to the rest of the core as the HC reset would.
13	RW	0h	SUS	When set to '1' ignore hot reset to the USB3 port logic
12	RW	0h	SUS	When set to '1' ignore warm reset to the USB3 port logic
11	RW	0h	SUS	When set to '1' ignore main power up reset to USB3 port logic
10	RW	0h	SUS	When set to '1' ignore main power up reset to USB2 port logic

Bit	Access	Default Value	RST/PWR	Description
9	RW	0h	SUS	When set to '1' ignore main power up reset to PCIe core
8	RW	0h	SUS	When set to '1' ignore main power up reset to PCIe PHY
7	RW	1h	SUS	When set to '1' ignore HC reset to the USB PHY
6	RW	1h	SUS	When set to '1' ignore warm reset to the USB PHY
5	RW	1h	Core	When set to `1`, it enables the reset isolation function that we have added during HC reset or Per port reset.
4	RW	1h	SUS	When set to '1' allow main power off condition to trigger a main power domain reset
3	RW	0h	SUS	When set to '1' ignore waiting for PERST# deassertion during main power show down.
2	RW	0h	SUS	When fundamental reset is asserted during AUX power up, if this bit is set, then we will ignore PERST# such that purely wait for timeout to deassert fundamental reset.
1	RW	0h	SUS	Indicates a fundamental reset 0: no reset
0	WO	0h	SUS	Write 1 to this register will cause a fundamental reset if the bit1 is also written to 1

Table 182. HOST_BW_OV_SS_REG - Super Speed Bandwidth Overload

Address Offset:80C4-80C7h
Default Value:004A4008h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:24	RO	0h	Core	RESERVED
23:12	RW	4A4h	Core	Max. TT BW allowed. see white paper
11:0	RW	8h	Core	BW calculation: Overhead per packet for SS BW calculations. See white paper.

Table 183. HOST_BW_OV_HS_REG - High Speed TT Bandwidth Overload

Address Offset:80C8-80CBh
Default Value:0001A01Fh
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:24	RO	0h	Core	RESERVED
23:12	RW	01Ah	Core	BW calculation: Overhead per packet for HS-TT BW calculations. see white paper.
11:0	RW	01Fh	Core	BW calculation: Overhead per packet for HS BW calculations. see white paper.

Table 184. HOST_BW_OV_FS_LS_REG - Bandwidth Overload Full Low Speed

Address Offset:80CC-80CFh
Default Value:00014080h
Access: RW;
Size:33 bits

Bit	Access	Default Value	RST/PWR	Description
31:24	RO	0h	Core	RESERVED

Bit	Access	Default Value	RST/PWR	Description
23:12	RW	14h	Core	BW calculation: Overhead per packet for FS BW calculations. see white paper.
11:0	RW	080h	Core	BW calculation: Overhead per packet for LS BW calculations. see white paper.

Table 185. HOST_BW_OV_SYS_REG - System Bandwidth Overload

Address Offset:80D0-80D3h
Default Value:00032010h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:24	RO	0h	Core	RESERVED
23:12	RW	32h	Core	BW calculation: Overhead per TT packet for System BW calculations. see white paper.
11:0	RW	10h	Core	BW calculation: Overhead per packet for System BW calculations. see white paper.

Table 186. HOST_CTRL_SCH_ASYNC_DELAY_REG - Scheduler Async Delay

Address Offset:80D4-80D7h
Default Value:00000000h
Access: RW;
Size:32 bits
Global defaults for inserting delays between packets in the scheduler for async. types.

Bit	Access	Default Value	RST/PWR	Description
31:20	RO	0h	Core	RESERVED
19	RW	0h	Core	High-Speed Bulk Delay Enable
18:16	RW	0h	Core	High-Speed Bulk Delay Default (0=125us,1=250us,2=500us,3=1ms,…)
15	RW	0h	Core	Full-Speed Bulk Delay Enable
14:12	RW	0h	Core	Full-Speed Bulk Delay Default (0=125us,1=250us,2=500us,3=1ms,…)
11	RW	0h	Core	High-Speed Control Delay Enable
10:8	RW	0h	Core	High-Speed Control Delay Default (0=125us,1=250us,2=500us,3=1ms,…)
7	RW	0h	Core	Full-Speed Control Delay Enable
6:4	RW	0h	Core	Full-Speed Control Default (0=125us,1=250us,2=500us,3=1ms,…)
3	RW	0h	Core	Low-Speed Control Delay Enable
2:0	RW	0h	Core	Low-Speed Control Delay Default (0=125us,1=250us,2=500us,3=1ms,…)

Table 187. DUAL_ROLE_CFG0 Dual Role Configuration Register 0

Address Offset:80D8-80DBh
Access: RW;
Size:32 bits
Device Mode control.
All bits in this register must be in the Always ON Power domain (ungated SUSor AON – as appropriate)

Bit	Access	Default Value	RST/PWR	Description
31:0	RW	0h	SUS	Reserved

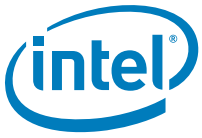


Table 188. DUAL_ROLE_CFG1 Dual Role Configuration Register 1

Address Offset:80DC-80DFh
Access: RO;
Size:32 bits
Device Mode control.
All bits in this register must be in the Always ON Power domain (ungated SUS or AON – as appropriate)

Bit	Access	Default Value	RST/PWR	Description
31:0	R0	0h	SUS	Reserved

Table 189. AUX_CTRL_REG1 - (PM_MISC_REG) AUX Power Management Control

Address Offset:80E0-80E3h
Default Value:808DBCA0h
Access: RW;
Size:32 bits
Chassis Restore: S0iX (Regular)
Restore Group: VNNAON

Bit	Access	Default Value	RST/PWR	Description
31	RW	1h	SUS	D3 Hot function enable register. This bit is from pin input which is set "1". But we allow software to alter it if it is needed. 1: D3 hot enabled 0: D3 hot not enabled.
30	RW	0h	SUS	This bit enables the gate-off the core clock when AUX PM control is in low power state. 1: enabled to gate off the core clock 0: disable this function
29	RW	0h	SUS	This bit is there for a bug fix where we need to ensure that phystatus did not get lost during the rate change where clock switch logic takes some cycles to complete such that the PCie's core clock is at half of the PCIe PHY pclk. 1: extended phystatus assertion 0: not extended phystatus
28	RW	0h	SUS	Disable the overwrite function in AUX PM control module for its initiated rate change. 1: AUX PM control module will not alter the PCIe rate change function . 0: allows AUX PM control module to initiate its PCIE rate change when it needs to enable P2 overwrite P1 function.
27	RW	0h	SUS	Enable AUX reset module to treat every PERST# as a fundamental reset 1: enabled 0: disabled
26	RW	0h	SUS	This is a test/control bit. This bit is designed to control the lowest powerdown state of the PCIe that AUX PM module signaled to PIPE is P1. 1: always drive to P1 instead of P2 0: drive as normal operation
25	RW	0h	SUS	When set to 1 set the SSV flag.
24	RW	0h	SUS	When set to 1 clear the SSV flag

Bit	Access	Default Value	RST/PWR	Description
23	RW	1h	SUS	A debug control bit which is used to enable save&restore function. 1: enabled 0: disabled
22	RW	0h	SUS	Reserved
21	RW	0h	SUS	This bit sets the internal save_restore_enable flag to 0 when written to 1. Software is expected to clear this bit after it wrote this bit to 1. This is for test/debug purpose of the save&restore function. 1: clear the internal flag save_restore_enable 0: allows regular save&restore function to proceed.
20	RW	0h	SUS	0: Speculative upstream for Debug and SS/SSP port will detect WPR 1: No speculative upstream till port configuration is completed
19:18	RW	3h	SUS	Controls the drive strength of the IO buffer
17	RW	0h	SUS	1: On disconnect from U2P3 and U3, SS/SSP port will go to RXDET (Disconnect state directly) 0: On disconnect from U2P3 and U3, SS/SSP port will go initiate a P2 receiver detection before going into RXDET (Legacy behavior)
16	RW	1h	SUS	1: Disable USB3 port clock gating 0: Enable USB3 port clock gating
15	RW	1h	SUS	1: Enable P3 mode in RxDetect 0: Disable P3 mode in RxDetect
14	RW	0h	SUS	1: Enable USB3 PIPE reset when out of P3 mode 0: Disable USB3 PIPE reset when out of P3 mode
13	RW	1h	SUS	This bit enables the AUX PM control state machine to take over txelecidle signal of the PIPE during several special conditions. 1: Allow mask to mac_phy_txeleidle of PCIe core. 0: Disable the mask
12	RW	1h	SUS	This bit enables the PCIe status function. 1: xHC as a PCIe device will generate the PME message. 0: xHC as a PCIe device will not generate any PME nor report PME status.
11	RW	1h	SUS	When set to '1' enable isolation function for dual power zone.
10	RW	1h	SUS	This bit allows the AUX PM control module to decide whether we entered into P2 overwrite condition based on the power down state of the PCIe core is at P1 or the LTSSM of PCIe core is in L1. What we used to have is based on P1 of the PCIe core mac_phy_powerdown signal. This is not correct because LTSSM can be in RX detect to result a P1 of power down state. To preserve our old function, we add this chicken bit. 1: P2OverWrite function based on LTSSM in L1 0: P2Pverwrite function based on PCIe core PIPE mac_phy_powerdown is in P1.
9	RW	0h	SUS	When set to '1' disable core clock gating based on low power state entered

Bit	Access	Default Value	RST/PWR	Description
8	RW	0h	SUS	When set to '1' enable PHY status timeout function which is designed to cover the PCIePHY issue that we may have not able to detect the PHY status toggle. This is a safety feature in case we have gotten into a deadlock during PHY status acknowledgment.
7	RW	1h	SUS	When set to '1' ignore the aux_pm_en reg from PCIe core to continue the remote wake/clock switching support
6	RW	0h	SUS	When set to '1' enable P2 overwrite P1 when PCIe core has indicated the transition from P0 to P1. This is to enable entering the even lower power state.
5	RW	1h	SUS	When set 1 '1' enable the remote wake function by allowing P2 clock/switching and P2 entering
4:1	RW	0h	SUS	Forced PM state
0	WO	0h	SUS	When set to '1' force PM state to go to the state indicated in bit 4:1

Table 190. BATTERY_CHARGE_REG - Battery Charge

Address Offset:80E4-80E7h
Default Value:00000000h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:29	RW	0h	SUS	0 - Battery charge spec ver. 1.1. 1 - Always enable battery charge DM_SRC if not connected. Don't wait for portable device detect. (spec. ver. 1.2) 2 - Short DP/DM for non-BC spec. devices. 3 - Hybrid non-BC + BC mode auto-detect. A-sequence. 4 - Hybrid non-BC + BC mode auto-detect. B-sequence.
28	RW	0h	SUS	0 - Normal mode 1 - Apple mode (experimental)
27:4	RW	0h	Core	Reserved
3	RW	0h	SUS	0 - Battery charging disabled (Physical Port #3) 1 - Battery charging enabled (Physical Port #3)
2	RW	0h	SUS	0 - Battery charging disabled (Physical Port #2) 1 - Battery charging enabled (Physical Port #2)
1	RW	0h	SUS	0 - Battery charging disabled (Physical Port #1) 1 - Battery charging enabled (Physical Port #1)
0	RW	0h	SUS	0 - Battery charging disabled (Physical Port #0) 1 - Battery charging enabled (Physical Port #0)

Table 191. HOST_CTRL_WATERMARK_REG - Port Watermark

Address Offset:80E8-80EBh
Default Value:00800080h
Access: ;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:16	RW	80h	Core	RBUF water mark
15:0	RW	00h	Core	Reserved

Table 192. HOST_CTRL_PORT_LINK_REG - SuperSpeed Port Link Control

Address Offset:80EC-80EFh
Default Value:18010000h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:27	RW	3h	Core	When bit 26 is set to 1, this field indicates LTSSM state to be forced for test mode.When bit 26 is set to 0, this field is overloaded for normal operation mode. Bit 31 indicates polarity check mode 0: Only the 8th consecutive TS1/TS2 1: Any TS1/TS2 Bit 30 indicates TS2 link function check mode 0: Only the 8th consecutive TS2 1: Any TS2 Bit 29 indicates TS2 scrambler disable TX mode 0: do not return scrambler disable bit from RX 1: return scrambler disable bit from RX
26	RW	0h	Core	Reserved
25	RW	0h	Core	0: Normal operation mode 1: Direct link to U0 This bit is for test purpose only. It shall be written 0 in normal operation mode.
24:21	RW	0h	Core	Reserved
20	RW	0h	Core	0: Disable link error slave count 1: Enable link error slave count
19	RW	0h	Core	1: enable TS receive to complete U1/U2/U3 exit LFPS handshake 0: disable TS receive to complete U1/U2/U3 exit LFPS handshake
18	RW	0h	Core	1: enable logic idle receive to exit Polling.Configuration and Recovery.Configuration 0: disable logic idle receive to exit Polling.Configuration and Recovery.Configuration
17	RW	0h	Core	This bit specifies the port initialization timeout value. 1: 20us – 21us 0: 19us – 20us
16:15	RW	2h	Core	This field defines the latency to drive the PHY to enter low power mode 0: 4 cycles 1: 8 cycles 2: 16 cycles 3: 32 cycles
14:12	RW	0h	Core	This value defines the minimum time for the link to stay in Recovery.Active other than from U3. The granuity is 128us.
11:9	RW	0h	Core	This value defines the minimum time for the link to stay in Polling.Active and Recovery.Active from U3. The granuity is 128us.
8	RW	0h	Core	0: Normal operation mode 1: Force link to accept power management command
7	RW	0h	Core	0: Normal operation mode 1: Direct link to Recovery from U0

Bit	Access	Default Value	RST/PWR	Description
6	RW	0h	Core	0: Normal operation mode 1: Link fast training mode This bit should be written 0 in normal operation.
5	RW	0h	Core	0: Enable link scrambler 1: Disable link scrambler
4	RW	0h	Core	0: Normal operation mode 1: Direct link to U3 from U0 This bit is for test purpose only. It shall be written 0 in normal operation mode.
3	RW	0h	Core	0: Normal operation mode 1: Direct link to U2 from U0 This bit is for test purpose only. It shall be written 0 in normal operation mode.
2	RW	0h	Core	0: Normal operation mode 1: Direct link to U1 from U0 This bit is for test purpose only. It shall be written 0 in normal operation mode.
1	RW	0h	Core	0: Disable link loopback master mode 1: Enable link loopback master mode
0	RW	0h	Core	0: Enable link compliance mode 1: Disable link compliance mode

Table 193. USB2_LINK_MGR_CTRL_REG1 - USB2 Port Link Control 1, 2, 3, 4

Address Offset:80F0-80FFh
Default Value:See Below. Note: The default value can be different based on different configuration of this design
Access: RW;
Size:128 bits
These set of registers are used to control the USB set of timers. They are spread over 4 registers each 32 bits wide.

Bit	Access	Default Value	RST/PWR	Description
127: 125	RO	0h	SUS	RESERVED
124:123	RW	0h	SUS	additional guardband for L1 advance prewake. 00 = +0 us 01 = +1uF 10 = +2uF 11=+4uF
122	RW	0h	SUS	select L1 min idle duration that will be driven to Scheduler. Either drive '0' or based on L1 Timeout value
121	RW	0h	SUS	Enable periodic_prewake to prevent L1 entry if in U0, or wake from L1 if already in U2.
119:118	RO	0h	SUS	RESERVED
117: 105	RW	40h	SUS	#of microseconds after detecting U2 remote wake condition to reflect K
104: 92	RW	3Fh	SUS	# of microseconds after entering U2, linestate changes are ignored as bus settles
91: 79	RW	10CBh	SUS	# of microseconds after entering U3, linestate changes are ignored as bus settles
78: 63	RW	D6D7h	SUS	# of microseconds for total reset duration
63: 50	RW	31h	SUS	# of microseconds of Chirp-K to register that a device is chirping

Bit	Access	Default Value	RST/PWR	Description
49: 37	RW	31h	SUS	# of microseconds of K/J in disconnected state to register connect has occurred.
36: 24	RW	31h	SUS	# of microseconds of SE0 in FS/LS mode to register disconnect had occurred.
23:21	RW	0h	SUS	Reserved
20	RW	1h	SUS	Mode for extended L1 Exit recovery delay: 0: 12us 1: 50us
19	RW	1h	SUS	Mode select for L1 Timeout increments: 0: time out increments are in 125us 1: L1 Timeout increments are in 256us. Refer to USB2 PORTHLPMC.L1 Timeout in XHCI Spec for additional details
18	RW	0h	SUS	Reserved
17	RW	0h	SUS	0: Detect minimal packet EOP. 1: Detect nominal packet EOP.
16	RW	0h	SUS	0: Normal 1: Force full speed on host ports (disable chirp response)
15	RW	0h	SUS	0: Enforce 192 byte limit on complete-split INs. Treat any packet > 192 as babble case. 1: Disable 192 byte limit check.
14	RW	0h	SUS	0: Internal FS/LS Disconnect from linestate[1:0] 1: External provided FS/LS Disconnect from hostdisconnect input
13:12	RW	0h	SUS	Select UTMI Reset Source (FRD UTMI Reset Only) 00: HCReset or Force PHY Reset or {internal reset after disconnect/suspend for restart} (default) 01,11: UTMI reset = ~UTMI suspendm 10: UTMI reset = ~UTMI suspendm & synchronization to port clk.
11	RW	0h	SUS	1: Enable HS Disconnect Window Function 0: Disable HS Disconnect Window Function
10	RW	0h	SUS	0: Enable Port Error Detection (default) 1: Disable Port Error Detection
9	RW	1h	SUS	0: Enable Peek function for ISO-OUT (default) 1: Disable Peek function for ISO-OUT
8	RW	1h	SUS	0: Drive Resume-K on parallel Interface 1: Drive Resume-K directly on FS/LS Serial Interface (default)
7	RW	1h	SUS	0: Disable Drop-Ping Function in USB2 Protocol (default) 1: Enable Drop-Ping Function in USB2 Protocol
6	RW	0h	SUS	0: Disable Force-Ping Function in USB2 Protocol (default) 1: Enable Force-Ping Function in USB2 Protocol
5	RW	1h	SUS	0: Disable Auto-Ping Function 1: Enable Auto-Ping Function in USB2 Protocol (default)
4	RW	0h	SUS	0: PHY is suspend=U3,U2,disconnect (default) 1: Disable PHY SuspendM in All States

Bit	Access	Default Value	RST/PWR	Description
3	RW	0h	SUS	0: Normal operation (internal clock gated in U2,U3,disconnect) 1: UTMI Internal Clock Gate Disable
2	RW	0h	SUS	0: PHY is suspendM=0 in Disconnect State (default) 1: Disable PHY SuspendM in Disconnect State
1	RW	0h	SUS	0: Normal Operation (default) 1: Force PHY Reset
0	RW	0h	SUS	0: Normal Operation (default – FPGA/ASIC) 1: USB2 Accelerated Simulation Timing (default – simulation)

Table 194. HOST_CTRL_BW_CTRL_REG - HOST CONTROLLER BW CONTROL REG

Address Offset:8100-8103h
Default Value:8008h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:22	RO	0h	Core	Reserved
23	RW	0b	Core	Disable Bandwidth Calculator Wrap 0: Bandwidth Calculator will not execute operations after the the number of Endpoints submitted to BW Calc exceeds the Context Cache Depth (wrap event). 1: (Chicken-bit operation): The Bandwidth Calculator will not behave differently after the Endpoint count wrap event. Note: This bit was created for COE HSD 1404204505
22		0b	Core	usl_mode_disable
21		0b	Core	Enable No Fairness mode for OUT
20		0b	Core	Enable No Fairness mode for IN
19		0b	Core	Disable Melt-to-Large function
18		0b	Core	Legacy Factored Sys
17		0b	Core	Legacy System OV
16		0h	Core	Legacy System Bandwidth Loss
15		1b	Core	bw_intel_en_reg
14		0b	Core	SuperSpeed Bandwidth Consumed Legacy Mode
13		0b	Core	Enable Attach SPD USBIF
12		0b	Core	SuperSpeed Bandwidth Consumed Bidirectional Disable
11:8		0h	Core	Bandwidth Carryover Enable Interval
7		0h	Core	Reserved
6		0h	Core	bw_2nd_dis_reg
5:3		001b	Core	Bandwidth DMI Factor
2		0b	Core	Bandwidth Debug Enable:
1		0h	Core	bwcal_debug_bus_en
0		0h	Core	force_melt_zero_en

Table 195. FPGA_REV_REG – FPGA Revision Register

Address Offset:8104-8107h
Access: RW;

Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31: 0	RO	11000000h	Core	FPGA Revision This field demarks the FPGA Revision Number. This is managed through the FPGA Revision Define.

Table 196. HOST_IF CTRL_REG - HOST_IF_CTRL_REG

Address Offset:8108-810Bh
Default Value:01h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31	RW	0h	Core	Enable SW update to HW Slot Table Setting this bit will unlock the HW Slot Table contents (like Slot Table, rd/wr pointers of Slot Table, and Slot En state array)
30	RW	0h	Core	Enable OUT Performance fix - Setting this bit enable the optimization that we have done to reduce the bubble in OUT data path to improve the OUT bandwidth to 900+MB/s when multiple USB3 ports are active.
29:2	RO	0h	Core	Rsvd1 (Rsvd1):
1	RW	0h	Core	HC Halt Timeout Enable Enables the HC halt flow to time-out after 15 ms.
0	RW	1h	Core	Host IF (HOSTIF):

Table 197. HOST_BW_OV_BURST_REG – BANDWIDTH OVERLOAD BURST

Address Offset:810C-810Fh
Default Value:00008020h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:24	RO	0h	Core	RESERVED
23:12	RW	08h	Core	BW calculation: Overhead per burst for system BW calculations. see white paper.
11:0	RW	20h	Core	BW calculation: Overhead per burst for SS BW calculations. see white paper.

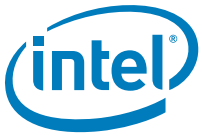
Table 198. HOST_CTRL_TRM_REG2 – Host Controller Transfer Manager Control 2

Address Offset:8110-8113h
Default Value:F0EC838Ch
Access: RW;
Size:32 bits
This register contains fields which control the behavior of the Transfer Manager in the XHC.
The functions controlled by this register are made available largely for debug/diagnostic purposes. This configurability is above and beyond that defined in the xHCI specification.

NOT for EDS

Bit	Access	Default Value	RST/PWR	Description
31	RW	1h	Core	This bit is added for bug FR2601. It is for cache invalidate case where xHC engine needs to insert wait states for completion engine when the completion has received a short packet before XFER engine has finished the TRB fetch for this packet at its packet boundary. 1: enables the feature 0: disabled
30	RW	1h	Core	This bit is added for bug FR2642. It is to delay the completion engine to generate an event due to internal error conditions that halted an EP until XFER engine has reached a packet boundary. 1: enabled 0: disabled
29	RW	1h	Core	This bit is added for bug FR2639. It enables the internal functions where xHC engine needs to immediately serve the EP again. 1: enabled 0: disabled
28	RW	1h	Core	This bit is added for bug FR2495. It enables that error completion code of the first error condition detected within an TD so that we can report the same error completion codes for all other TRBs within this TD. 1: enables the feature 0: disabled
27	RW	0h	Core	This bit disables a new feature where xHC engine will have an ODMA FIFO added for the commands between TRM and ODMA so that we can avoid the back-pressure situation due to the number of outstanding PCIe read limitation. This is for performance enhancement. 1: feature disabled 0: enabled
26	RW	0h	Core	This bit is added for bug FR2446. It is to enable TRM to only send one IN request for TTE 1st phase request even if it has not reached the packet boundary. 1: enabled 0: disabled
25	RW	0h	Core	This bit is added for bug FR2395. This disable the single IN EP for TTE function 1: only allow single IN EP per port for TTE 0: disabled
24	RW	0h	Core	This bit is added for bug FR2333 where the xHC engine has always ignored the credit returned from device for its OUT EP buffers when the EP is a periodic EP. 0: will enable the xHC engine to follow the flow control 1: will disable this feature
23	RW	1h	Core	This bit is added for bug FR2283. This is to ensure only 1 clear pulse generated when a completion has received. 1: enabled 0: disabled

Bit	Access	Default Value	RST/PWR	Description
22	RW	1h	Core	This bit enables a 2ms timeout for all TTE related EP stop endpoint command. The xHC engine will not check whether there is a pending response in context. It will only wait for 2ms and indicates that EP has been stopped. 1: enabled 0: disabled
21	RW	1h	Core	This bit enables xHC engine TRM to report the second or more events on an ISP flush on a second or more TRBs with ISP bit set that are flushed for a short packet response received. 1: enabled 0: disabled
20	RW	0h	Core	This bit enables a new feature where the completion engine of TRM can check the credit returned from remote device to not exceed its max burst size. If it does, we will keep the internal credits in the context to the max burst size so that xHC engine will not transmit more than max burst size. Note: CB has this bit default set to 0 PPT B0 and LPT will have this bit set to 1. 1: disabled 0: enabled
19	RW	1h	Core	Enable MSI_CNT update once we hit current interval during advancing. The new MSI_CNT value is calculated based on current uFrame w.r.t current Frame based on EP's SI. Disabling this will make controller to advance till either of below condition is met – MSI_CNT reaches to 0 Hit Isoc TD with FrameID for future frame/SI 1 – Enable MSI_CNT update 0 – Disable MSI_CNT update Note, this policy is only supported by the version of the controller that supports CFC=1 capability. Also, this policy should only be used when CFC=1 is enabled.
18	RW	1h	Core	This bit enables the xHC engine to fully support the non-0 control EP. This bit allows the xHC TRM to keep track of on non-0 control EP per port so that the responses can be routed to the correct DMA engine. 1: enabled 0: disabled
17	RW	0h	Core	This bit enables xHC engine to evaluate the next TRB even if the EP is at the end of a TD. 1: enables the feature 0: disables the feature
16	RW	0h	Core	Setting this bit to '1' will force xHC engine to ring internal doorbell on the EP that it has just received response for.



Bit	Access	Default Value	RST/PWR	Description
15	RW	1h	Core	This bit enables a feature where xHC engine will skip a service interval when an Interrupt EP has missed its service interval. 1: enables to skip a service interval 0: disables this feature
14	RW	0h	Core	New feature added to prevent the back-pressure from ODMA due to the fact that it ran out of ODMA timeout timer resources. This is for performance enhancement. We have put into the ODMA credit is part of resource calculation before TRM allows the next scheduling for OUT EP. 1: enables this feature 0: Disables this feature
13	RW	0h	Core	The xHC engine has a feature that can check with Receive Port Credit per root port to whether or not allowed the next schedule onto this port. This is for performance enhancement. This bit enables this feature 1: Feature enabled 0: Feature disabled
12	RW	0h	Core	1: Disable the error reporting for a received stream ID value of 0x0000. 0: Report received stream ID of 0x0000 as an error Note: only used when an endpoint is configured for stream operation.
11	RW	0h	Core	Enable the host to transfer to the prime-pipe state (and transmit a prime pipe) on each transfer back to the IDLE state. 1: Feature enabled 0: Feature disabled Note: only used when an endpoint is configured for stream operation.
10	RW	0h	Core	Reserved
9	RW	1h	Core	1: enable the XFER engine to auto detecting a missing service interval function when there is a long delay such that we missed a service interval due to the pending response. 0: disable this function in XFER engine.
8	RW	1h	Core	1: enable the function to support 0length TTE second phase request from TTE module. 0: disable this function.
7	RW	1h	Core	1: enable a packet pace function under a special condition. This is an internal feature to XFER engine. It is not expected to be used other than default. 0: disable this function.
6	RW	0h	Core	1: assert the sch_req_incomplete signal in XFER engine when a context FC is ON. This is an internal safety feature for XFER engine. 0: not to have this function
5	RW	0h	Core	1: enable the address device command to query a port credit before it is executed in ODMA engine. 0: Disable this function.

Bit	Access	Default Value	RST/PWR	Description
4	RW	0h	Core	1: Enable XFER engine to use context empty flag not assert as a way of identifying a TTE overlap condition. 0: Enable XFER engine to use a no-pending response flag as a way of identifying a TTE overlap condition
3	RW	1h	Core	1: enable the context storage for a flag to identify a DMA request as a 1st of TD DMA request. 0: disable the context storage.
2	RW	1h	Core	1: enable the credit redeem when a port is in NC state. 0: Disable the credit redeem
1	RW	0h	Core	1: enable the function where XFER engine uses the remaining burst count as an indication that the next TRB on the transfer ring for an ISO TD is either link TRB or event data TRB. 0: Disable this non DMA TRB detect function
0	RW	0h	Core	1: enable XFER engine to process a reserved TRB type as a NO-OP TRB 0: report TRB ERR for reserved TRB type.

Table 199. Sierra Back Door Registers

Address Offset:8114-8127h
Default Value:See below
Access: RW;
Size:160 bits (5 DW registers)

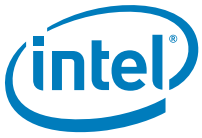
Table 200. HOST_CTRL_BW_MAX_REG – Max BW control Reg 4

Address Offset:8128-8133h
Default Value:See below
Access: RW;
Size:64 bits

Bit	Access	Default Value	RST/PWR	Description
95:84	RO	0h	Core	Reserved
83:72	RW	93Fh	Core	Max. Number of BW units for SSP ports. (denominator in 90% calculation)
71:60	RW	F42h	Core	Max. Number of OUT BW units for PCIe ports. (denominator in 90% calculation)
59:48	RW	F42h	Core	Max. Number IN of BW units for PCIe (system interface) (denominator in 90% calculation)
47:36	RW	528h	Core	Max. Number of BW units for TTs. (denominator in 90% calculation)
35:24	RW	505h	Core	Max. Number of BW units for FS/LS ports. (denominator in 90% calculation)
23:12	RW	647h	Core	Max. Number of BW units for HS ports. (denominator in 80% calculation)
11:0	RW	F42h	Core	Max. Number of BW units for SS ports. (denominator in 90% calculation)

Table 201. USB2_PROTOCOL_GAP_TIMER_LOW_REG – USB2 Protocol Gap Timer LOW

Address Offset:8134-8137h
Default Value:See below
Access: RW;



Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:24	RW	12d	Core	GAP time after FS 16.667 ns time units
23:16	RW	5d	Core	GAP time after HS RX 16.667 ns time units
15:8	RW	20d	Core	GAP time after HS TX SOF 16.667 ns time units
7:0	RW	12d	Core	GAP time HS TX Packet 16.667 ns time units

Table 202. USB2_PROTOCOL_GAP_TIMER_HIGH_REG – USB2 Protocol Gap Timer HIGH

Address Offset:8138-813Bh
Default Value:See below
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:24	RO	0	Core	Reserved
23:16	RW	12d	Core	GAP time after LS TX thru FS hub 16.667 ns time units
15:8	RW	60d	Core	GAP time after LS RX thru FS hub 16.667 ns time units
7:0	RW	100d	Core	GAP timer after LS 16.667 ns time units

Table 203. USB2_BTO_CTRL_REG – USB2 Bus Timeout Control

Address Offset:813C-813Fh
Default Value:8D4258B8
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description

31:22	RW	46A	Core	Bus timeout count for LS
				This value depended on whether this parameter USB2_PROTO_PROGRAMMBLE_DELAY is defined during synthesis.
				If USB2_PORT_CLK_60 is defined,
				{If USB2_PROTO_PPTLPT_DELAY is defined,
				Then the default value is : x46A,
				else x2DA,}
				Else
				{If USB2_PROTO_PPTLPT_DELAY is defined,
				Then the default value is : = x230
				else
				x172,}
				
				16.667 ns time units

Bit	Access	Default Value	RST/PWR	Description

21:11	RW	96	Core	Bus timeout count for FS
				This value depended on whether this parameter USB2_PROTO_PROGRAMMBLE_DELAY is defined during synthesis.
				If USB2_PORT_CLK_60 is defined,
				{If USB2_PROTO_PPTLPT_DELAY is defined,
				Then the default value is : x96,
				else
				x64,}
				Else
				{If USB2_PROTO_PPTLPT_DELAY is defined,
				Then the default value is : x50
				else
				x37}
				
				16.667 ns time units

10:0	RW	B8	Core	Bus timeout count for HS This value depended on whether this parameter USB2_PROTO_PROGRAMMBLE_DELAY is defined during synthesis. If USB2_PORT_CLK_60 is defined, 0xB8 Else 0x61 16.667 ns time units

Table 204. HOST_IF_PWR_CTRL_REG0 - Power Scheduler Control 0

Address Offset:8140-8143h
Default Value:0A019132h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:24	RW	Ah	Core	Engine Idle Hysteresis (EIH): This register controls the min. idle span that has to be observed from the engine idle indicators before the power state flags (xhc_*_idle) will indicate a 1 (TBD units)
23:12	RW	19h	Core	Fabric PLL Shutdown Advance Wake (FPSAW): This register controls the time before the next scheduled transaction where the Fabric PLL request will assert. Register Format: Bits [11:7] # of 125us uframes Bits [6:0] # of microseconds (0-124) Note this field shall be set to a minimum of 4 us.

Bit	Access	Default Value	RST/PWR	Description
11:0	RW	132h	Core	Fabric PLL Shutdown Min. Idle Duration (FPSMID): The sum of this register plus the FPSAdvance Wake form to a Total Idle time. When the next scheduled periodic transaction is after present time + Total Idle, the Fabric PLL request will de-assert, allowing the PLL to shutdown, based upon relevant enabled EP types (see Alarm bit definitions below). Register Format: Bits [11:7] # of 125us uframes Bits [6:0] # of microseconds (0-124)

Table 205. HOST_IF_PWR_CTRL_REG1 - Power Scheduler Control 1

Address Offset:8144-8147h
Default Value:0000033Fh
Access: RW;
Size:32 bits
These bit enable by EP type those EPs classes that are considered for determining next periodic active interval for pre-wake of the periodic_active signal. EP classes that are disabled may never be observed in setting of the periodic_active signal.

Bit	Access	Default Value	RST/PWR	Description
31:20	RW	0h	Core	Rsvd1 (Rsvd1):
19	RW	0h	Core	Enhanced Engine IDLE 0: HSD 375274 fix is enabled. “Engine IDLE” is deasserted if the Scheduler State Machine is performing the Periodic walk. 1: Revert to previous behavior
18:17	RW	0h	Core	Rsvd1 (Rsvd1):
17	RW	0b	Core	D0i2 Clear Alarm Fix Disable: 0: The D0i2 Alarm will self clear when the current time passes the D0i2 time, and the D0i2 Alarm will not clear at the beginning of every microframe. 1: The D0i2 will clear at the beginning of every microframe. Note: This bit was created for GEN2 HSD 1404805196.
16	RW	0b	Core	Disable HC Halt Clears Alarm: 0: The Host Controller Halt condition (hc_halt) will clear the LTR, PLL, and LPM alarms in the Power Scheduler. This prevents erroneous wakeups. 1: (Chicken-bit operation) Host Controller Halt condition does not clear the Power Scheduler alarms. Note: This bit was created for GEN2 HSD 1603947569.
15	RW	0h	Core	Disable BELT Latch: 1: The Power Scheduler’s interface to the LTR Manager signals BELT and No_Requirement are not latched with the Request signal and can change before Halt is deasserted. Asserting this bit will disable the fix from HSD LPTLP 375141. 0: The Power Scheduler’s interface to the LTR Manager signals BELT and No_Requirement are latched when the Request signal is asserted and will remain latched until Halt is deasserted.

Bit	Access	Default Value	RST/PWR	Description
14	RW	0h	Core	LPM Prewake Naked Interrupt Enable 0: Ignore the Naked INTR for LPM. 1: Do not ignore the Naked INTR for LPM.
13:12	RW	0h	Core	LPM Prewake Interrupt Enable 11: Disable interrupt prewake for LPM. 01: Enable interrupt OUT prewake for LPM. 10: Enable interrupt IN prewake for LPM. 00: Enable both interrupt IN/OUT prewake for LPM.
11:10	RW	0h	Core	Engine Idle Hysteresis Scale Controls the Engine Idle Hysteresis scale. 0 - clock 1 - 1 us 2 - 125 us
9	RW	1h	Core	HS Interrupt OUT Alarm (HSIO):
8	RW	1h	Core	HS Interrupt IN Alarm (HSII): Note: This is required to not be set to enable the functionality behind the PCICFG.HSCFG2.HSIIPAPC method of tracking HS Intr IN EP's for Periodic Active.
7	RW	0h	Core	SS Interrupt OUT Alarm (SSIO):
6	RW	0h	Core	SS Interrupt IN Alarm (SSII):
5	RW	1h	Core	SS Interrupt OUT and not in FC Frame Alarm (SSIO):
4	RW	1h	Core	SS Interrupt IN and not in FC Frame Alarm (SSII):
3	RW	1h	Core	HS ISO-OUT Alarm (SSOA):
2	RW	1h	Core	HS ISO-IN Alarm (SSIA):
1	RW	1h	Core	SS ISO-OUT Alarm (SSOA):
0	RW	1h	Core	SS ISO-IN Alarm (SSIA):

Table 206. AUX_CTRL_REG2 – (PM_MISC1_REG) Aux PM Control Register 2

Address Offset:8154-8157h
Default Value:81390206h
Access: RW;
Size:32 bits
Chassis Restore: S0iX (Regular)
Restore Group: VNNAON

Bit	Access	Default Value	RST/PWR	Description
31	RW	0h	SUS	This bit disables the dependency on Wake Enables defined in PORTSC for L1P2 exit when in D0
30:28	RW	0h	SUS	RESERVED
27:25	RW	0h	SUS	Reserved

Bit	Access	Default Value	RST/PWR	Description
24	RW	1h	SUS	This bit enables a L1 exit notification to SNPS PCIe core. There is a case where USB ports have waked up and AUX PM module has started the wakeup process. The AUX PM control state got into a wait for P0 state because it needs to wait until PCie core to signal powerdown state change. Due to the fact that the core is in D3Hot, there is no run_stop bit set such that no internal interrupt will be fired. This causes the LTSSM of PCIe stayed in L1 even though AUX PM has known that it needs an L1 exit. This bit works together with bit21 of this register. 1: enables this feature 0: disables this feature.
23	RW	0h	SUS	1: do not assert PLC for disconnection 0: assert PLC for disconnection
22	RW	0h	SUS	This bit enables a feature in PCie core LTSSM to treat IDLE received as TS2 when LTSSM is in wait for TS2 receive state. This is a function requested from PHY where it is possible to not able to receive TS2 without error. 1: treat Logic IDLE as TS2 received when in some PCIe LTSSM state. 0: disable this feature.
21	RW	1h	SUS	We added a feature where if PCIe core LTSSM enters L1 due to the D3hot, the aux PM control will not start a P2 overwrite function in anticipating for the next L23 enter. 1: disables p2 overwrite due to the D3HOT where PCIe core enters the L1. 0: enables P2 overwrite even if we are in D3Hot.
20	RW	1h	SUS	1: enables the port to enter U3 automatically when in U1/ U2 0: disables the port to enter U3 automatically when in U1/ U2
19	RW	1h	SUS	1: No linkdown reset is issue during low power state
18	RW	0h	SUS	This bit enables a feature in AUX PM module where if PCIe core LTSSM is in P0 for a duration of time, we will exit the deep sleep state. This is for failure control in case. 1: enables this feature 0: disable this feature
17	RW	0h	SUS	This bit selects U2 exit LFPS timer value 0: 320ns – 400ns in 25MHz domain 1: 240ns – 320ns in 25MHz domain
16	RW	1h	SUS	This bit enables a function that AUX PM module exits from the deep sleep state due to the USB ports wakeup level signal. We have added this feature where USB ports will generated a wakeup level signal to wakeup the AUX PM module if it is in deep sleep state and this level signal will be cleared if the change bits are updated by software. 1: enables this function 0: disables this function which means that a wakeup pulse generated from each USB PortSC event will wake up the AUX PM module from deep sleep if the D3 state is programmed.

Bit	Access	Default Value	RST/PWR	Description
15:14	RW	0h	SUS	This field defines the timeout value to enter P3 mode in U2. 00: 7us – 8us 01: 511us – 512us 10: disables the timer (0us) 11: disables the timer (0us)
13	RW	0h	SUS	1: enables PHY P3 mode in U2. 0: disables PHY P3 mode in U2.
12:11	RW	0h	SUS	Reserved
10	RW	0h	SUS	This bit enables a function that the SPNS PCIe core is controlled by xHCI engine internal periodic EP traffic conditions. 1: enables the xHC engine to request an exit of L1 when the service time has reached for an periodic EP. 0: disabled this function
9	RW	1h	SUS	This bit selects the port status change event generation mode. 1: port status change event is blocked until all status change bit are cleared. 0: port status change event is only blocked by the individual status change bit.
8:4	RW	0h	SUS	Reserved.
3	RW	0h	SUS	This bit enables the AUX PM module to automatically wakeup from deep power down when engine has detected non-idle condition. 1: feature enabled 0: feature disabled
2	RW	1h	SUS	This bit ensures the P1 drive during PERST#. 1: feature enabled 0: feature disabled
1	RW	1h	SUS	This bit enables PCIe PCLK isolation function when in two power domain. 1: feature enabled 0: feature disabled
0	RW	0h	SUS	This bit enables a feature where we can get P2 overwrite to automatically turned on when there is no pending traffic in the engine. Note: This bit may vary depending on the synthesis parameter selection. 1: feature enabled 0: feature disabled

Table 207. HOST_CTRL_SCH _REG - Host Control Scheduler 2

Address Offset:8160-8163h
Default Value:0h
Access: RW;

Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31	RW	0b	Core	Double Clear Disable for STOP Endpoint vs DB ring race condition 0: TBD 1: (Chicken-bit operation): The function is disabled. Note: This bit was created for COE HSD 1202394058.
30	RW	0b	Core	Maintain Out Interrupt on Flow Control 0: (Current mode of operation). A Flow Control will cause a SuperSpeed Out Interrupt Endpoint to be removed from the Schedule for the current Service Interval (Done bit is set) 1: A Flow Control will NOT cause a SuperSpeed Out Interrupt Endpoint to be removed from the Schedule for the current Service Interval. Note: This bit was created for COE HSD 1208391.
29	RW	0b	Core	Enable PRDC Credit Fix 0: PRDC Credit (All Credits) indication from the TRM for both OUT and IN are inaccurate and assert when there is at least 1 credit available. 1: PRDC Credit (All Credits) indication from the TRM for both OUT and IN are accurate and assert when all credits are available. Note: This bit was created for COE HSD 1011716755. Note: this bit should be removed for ICELAKE and forward.
28	RW	0b	Core	Enable Starvation Fix 0: Asynchronous Endpoint reservation system does not work for Control Endpoints. 1: Asynchronous Endpoint reservation system does work for Control Endpoints. Note: This bit was created for COE HSD 1403916447. Note: this bit should be removed for ICELAKE and forward.
27	RW	0h	Core	Disable Stream ID Clear 0: Current Stream ID and Last Current Stream ID area cleared duriing Stop Endpoint. 1: (Chicken-bit operation): Current Stream ID and Last Current Stream ID area not cleared during Stop Endpoint. Note: This bit was created for COE HSD 1403912459.
26:10	RW	0h	Core	Reserved
9	RW	0h	Core	Disable Doorbell Clear vs Request Race Condition 0: Race condition between the Stop Endpoint Command clearing the Doorbell vs the Scheduler requesting service on and Endpoint will not incorrectly divert to Late Frame logic. 1: (Chicken-bit operation): The Scheduler may incorrectly divert to Late Frame logic when a Stop Endpoint Command clears the Doorbell while the Scheduler is requesting service on that Endpoint. Note: This bit was created for COE HSD 1404494630.
8:7	RW	0h	Core	ASYNC Port Active Policy
6:5	RW	0h	Core	PRDC Port Active Policy
4	RW	0b	Core	ASYNC Port Active Disable

Bit	Access	Default Value	RST/PWR	Description
3	RW	0b	Core	PRDC Port Active Disable
2	RW	0b	Core	Always Reserve Disable
1	RW	0b	Core	Polling Reservation Disable
0	RW	0b	Core	Disable repeat scheduler service of usb2 periodic

Table 208. USB2PHYPM – USB2 Phy Power Management Control

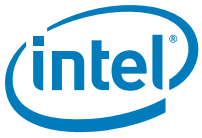
Address Offset:0x8164 – 0x8167
Default Value:0x0000_0000
Access: RW; RO
Size: 32bits

Bit	Access	Default Value	RST/PWR	Description
31:8	RO	0	NA	Reserved
7	RW	1	Core	Enable Command Manager Active indication for Tx/Rx Bias circuit HS Phy PM Policy
6	RW	1	Core	Enable TTE Active indication for Tx/Rx Bias circuit HS Phy PM Policy
5	RW	1	Core	Enable IDMA Active indication for Tx/Rx Bias circuit HS Phy PM Policy
4	RW	1	Core	Enable ODMA Active indication for Tx/Rx Bias circuit HS Phy PM Policy
3	RW	1	Core	Enable Transfer Manager Active indication for Tx/Rx Bias circuit HS Phy PM Policy
2	RW	1	Core	Enable Scheduler Active indication for Tx/Rx Bias circuit HS Phy PM Policy
1	RW	0	Core	Enable Rx Bias ckt disable When set enables the Rx bias ckt to be disabled when conditions met (as described by the HS phy PM policy bits)
0	RW	0	Core	Enable Tx Bias ckt disable When set enables the Tx bias ckt to be disabled when conditions met (as described by the HS phy PM policy bits)

Table 209. USB2PHYPM2 – USB2 Phy Power Management Control 2

Address Offset:0x8168 – 0x816B
Default Value:0x0002_82EE
Access: RW; RO
Size: 32bits

Bit	Access	Default Value	RST/PWR	Description
31:21	RO	0	Core	Reserved
20:15	RW	5h	Core	Tx/Rx Off Min Time: Minimum number of clocks (uclk60x) for which Tx/Rx shall be switched off. This is used to decide if bias circuits can be switched off in the current micro-frame ahead of the next Tx/Rx.
14:7	RW	5h	Core	Tx/Rx Off Wait time: Guardband time in number of clocks (uclk60x) before which Tx/Rx can be turned off when there is no activity



Bit	Access	Default Value	RST/PWR	Description
6:0	RW	6Eh	Core	Tx/Rx Pre Tx on time: This is the time (in uclk60 clock periods) when Tx/Rx Bias needs to be turned on ahead of Transmit or Receive. This is based on the AFE requirement when bias needs to be ON before the transmit/receive occurs on the bus.

Table 210. AUXCLKCTL - xHCI Aux Clock Control Register

Address Offset:0x816C – 0x816F
Default Value:0x0000_0400
Access: RW; RO
Size: 32bits
Chassis Restore: S0iX (Regular)
Restore Group: VNNAON

Bit	Access	Default Value	RST/PWR	Description
31:21	RO	0	NA	Reserved
20	RW	0	SUS	Port Reset Auto Complete when in Device Mode: This bit controls the release of warm rst_req_done immediately on reciept of req when in Device Mode 0: Auto Complete Port Reset 1: Wait for Port Reset on the wire for completion of Port Reset
19	RW	0	SUS	USB3 Partition Engine/Link trunk gating Enable When set to '1' enables gating of the SOSC trunk to the XHCI engine/link in the PARUSB3 partition.
18	RW	0	SUS	USB3 Partition Frame Timer trunk gating Enable When set to '1' enables gating of the SOSC trunk to the Frame Timer in the PARUSB3 partition.
17	RW	0	SUS	USB2 link partition clock gating enable When set to '1' enables gating of the SOSC trunk to the USB2 link and Phy logic in the PARUSB2 partition.
16	RW	0	SUS	USB2/USHIP 12.5 MHz partition clock gating enable When set to '1' enables gating of the 12.5 MHz SOSC trunk to the USB2 and USHIP logic in the PARUSB2 partition.
15	RO	0	SUS	Reserved
14	RW	0	SUS	USB3 Port Aux/Core clock gating enable When set, allows the aux_cclk clock into the USB3 port to be gated when conditions are met.
13:12	RW	0x0	SUS	Reserved
11:8	RW	0x4	SUS	Reserved
7	RW	0	SUS	Frame Timer Clock Gating Ports in U2 Enable (FTCGPU2E) This bit, when set, allows Host Controller to gate the clock to the Frame Timer when ports are in U2.
6	RW	0	SUS	USB2 port clock throttle enable When set, allows the Aux clock into the USB2 ports to be throttled when conditions allow.

Bit	Access	Default Value	RST/PWR	Description
5	RW	0	SUS	XHCI Engine Aux clock gating enable When set, allows the aux clock into the XHCI engine to be gated when idle.
4	RW	0	SUS	XHCI Aux PM block clock gating enable When set, allows the aux clock into the Aux PM block to be gated when idle.
3	RW	0	SUS	Reserved
2	RW	0	SUS	USB3 Port Aux/Port clock gating enable When set, allows the aux_pclk clock into the USB3 port to be gated when conditions are met.
1	RW	0	SUS	ModPHY port Aux clock gating enable in U2 When set, allows the aux clock into the ModPhy to be gated when Link is in U2 and pipe has been in PS3 for at least the time defined by U2 Residency Before ModPHY Clock Gating field.
0	RW	0	SUS	ModPHY port Aux clock gating enable in Disconnected, U3 or Disabled When set, allows the aux clock into the ModPHY to be gated when Link is in Disconnected, U3 or Disabled state.

Table 211. USB2LPM – USB LPM Parameters

Address Offset:0x8170 – 0x8173
Default Value:0x0009_0032
Access: RW; RO
Size: 32bits

Bit	Access	Default Value	RST/PWR	Description
31:22	RO	0	SUS	Reserved
21:19	RW	0b001	SUS	Min U3 Exit LFPS Duration This field defines the minimum duration of LFPS driven by Host Controller upon U3 exit LFPS handshake. Note that there's an uncertainty of +-16us in actual duration driven by the Host Controller. 0b000:96us 0b001:160us 0b010:224us 0b011:288us 0b100:352us 0b101:416us 0b110:480us 0b111:544us

Bit	Access	Default Value	RST/PWR	Description
18:16	RW	0b001	SUS	Min U2 Exit LFPS Duration This field defines the minimum duration of LFPS driven by Host Controller upon U2 exit LFPS handshake. Note that there's an uncertainty of +-16us in actual duration driven by the Host Controller. 0b000:96us 0b001:160us 0b010:224us 0b011:288us 0b100:352us 0b101:416us 0b110:480us 0b111:544us
15:10	RW	0	SUS	Reserved
9:0	RW	032h	SUS	xHCI BESL to HIRD Distance This field defines the gap between BESL and duration of Resume signalling from Host upon Host Initiated Resume from USB2.0 LPM. Default value of this register corresponds to xHCI spec defined 50us value. Value BESL to HIRD Distance 000h 0us 001h 1us 002h 2us : : : 3FFh 1023us

Table 212. XHCLTVCTL1 – XHCI Latency Tolerance Control 1

Address Offset:0x8174 – 0x8177
Default Value:0x0040_047D
Access: RW; RO
Size: 32bits

Bit	Access	Default Value	RST/PWR	Description
31	RW	0	Core	Disable scheduler direct transition from IDLE to NO requirement 0: (default) allow scheduler direct transition from IDLE to NO requirement 1: Disable scheduler direct transition from IDLE to NO requirement

Bit	Access	Default Value	RST/PWR	Description
30	RW	0b	Core	XHCI LTR Transition Policy (XLTRTP) When '0', the LTR messaging state machine transitions through High _ Med _ Low _ Active states assuming enough latency is available for each transition. When '1', LTR messaging state machine transitions from High, Medium, or Low LTR states to Active state upon the Alarm Timer timeout and stays in Active until the next service boundary.
29	RW	0b	Core	Include Scheduler First Round in Active Signal Disable 0: 'xHC Engine Idle' from the Power Scheduler will not assert if the Scheduler is performing its first round pass through periodic endpoints. 1: (Chicken bit) Revert to previous behavior. Scheduler's first round checks not included in 'xHC Engine Idle' equation.
28	RW	0b	Core	XHCI LTR Active Enable (XLTRAE) 0: The Power Scheduler will not request an LTR message on a transition to ACTIVE. 1: The Power Scheduler will request an LTR message on a transition to ACTIVE.
27	RW	0b	Core	Power Scheduler Local Clock Gating Enable (PWRLCGE) 0: Power Scheduler does not use local clock gating 1: Power Scheduler's local clock gating enabled. Note: This functionality is no longer required. This LCG existed previous to the inclusion of Aux clock gating.
26	RW	0b	Core	LTR EVM Hysteresis Max Count Power Scheduler's 'Periodic IDLE' residency before we assert 'Periodic Complete' 0: Hysteresis set to 127 clock ticks. (.64µs) 1: Hysteresis set to 31 clock ticks (.16µs)
25	RW	0b	Core	Reserved (for future ECO use).
24	RW	0b	Core	XHCI LTR Enable (XLTRE) This bit must be set to enable LTV messaging from XHCI to the PMC.
23:12	RW	400h	Core	Periodic Active LTV 23:22 Latency Scale 00b : Reserved 01b : Latency Value to be multiplied by 1024 10b : Latency Value to be multiplied by 32,768 11b : Latency Value to be multiplied by 1,048,576 21:12 Latency Value (ns) Defaults to 0µs

Bit	Access	Default Value	RST/PWR	Description
11:0	RW	47Dh	Core	USB2 Port L0 LTV 11:10 Latency Scale 00b : Reserved 01b : Latency Value to be multiplied by 1024 10b : Latency Value to be multiplied by 32,768 11b : Latency Value to be multiplied by 1,048,576 9:0 Latency Value (ns) Defaults to 128µs

Table 213. XHCLTVCTL2 – XHCI Latency Tolerance Control 2

Address Offset:0x8178 – 0x817B
Default Value:0x0000_17FF
Access: RW; RO
Size: 32bits

Bit	Access	Default Value	RST/PWR	Description
31:13	RO	0	NA	Reserved
12:0	RW	17FFh	Core	LTV Limit: This register defines a maximum LTR value that is allowed to be advertised to the PMC. This is meant to be used as a workaround or mitigation if issues are discovered with the LTR values generated by the XHC using the defined algorithms. If the LTR value of the XHC is larger than the value in this register field, the value in this field is sent to the PMC instead. Default value is the highest possible (101b) 12:10: Latency Multiplier Field 000b – Value times 1 ns 001b – Value times 32 ns 010b – Value times 1,024 ns 011b – Value times 32,768 ns 100b – Value times 1,048,576 ns 101b – Value times 33,554,432 ns 110b-111b – Not Permitted 9:0: Latency Value Default = 3FFh

Table 214. LTVHIT - xHC Latency Tolerance Parameters – High Idle Time Control

Address Offset:0x817C – 0x817F
Default Value:0x0000_0000
Access: RW; RO
Size: 32bits

Bit	Access	Default Value	RST/PWR	Description
31:29	RO	0	NA	Reserved

Bit	Access	Default Value	RST/PWR	Description
28:16	RW	0000h	Core	Minimum High Idle Time (MHIT) This is the minimum schedule idle time that must be available before a "High" LTR value can be indicated. This value must be larger than HIWL 12:7 – Time value in # of 125µs Bus Intervals (0 – 8ms) 6:0 – Fractional BI Time value in µs (0 – 124µs)
15:13	RO	0	NA	Reserved
12:0	RW	0000h	Core	High Idle Wake Latency (HIWL) This is the latency to access memory from the High Idle Latency state. This value must be larger than MIWL and LIWL 12:7 – Time value in # of 125µs Bus Intervals (0 – 8ms) 6:0 – Fractional BI Time value in µs (0 – 124µs)

Table 215. LTVMIT - xHC Latency Tolerance Parameters – Medium Idle Time Control

Address Offset:0x8180 – 0x8183
Default Value:0x0000_0000
Access: RW; RO
Size: 32bits

Bit	Access	Default Value	RST/PWR	Description
31:29	RO	0	NA	Reserved
28:16	RW	0000h	Core	Minimum Medium Idle Time (MMIT) This is the minimum schedule idle time that must be available before a "Medium" LTR value can be indicated. This value must be larger than MIWL 12:7 – Time value in # of 125µs Bus Intervals (0 – 8ms) 6:0 – Fractional BI Time value in µs (0 – 124µs)
15:13	RO	0	NA	Reserved
12:0	RW	0000h	Core	Medium Idle Wake Latency (MIWL) This is the latency to access memory from the Medium Idle Latency state. This value must be larger than LIWL 12:7 – Time value in # of 125µs Bus Intervals (0 – 8ms) 6:0 – Fractional BI Time value in µs (0 – 124µs)

Table 216. LTVLIT - xHC Latency Tolerance Parameters – Low Idle Time Control

Address Offset:0x8184 – 0x8187
Default Value:0x0000_0000
Access: RW; RO

Size: 32bits

Bit	Access	Default Value	RST/PWR	Description
31:29	RO	0	NA	Reserved
28:16	RW	0000h	Core	Minimum Low Idle Time (MLIT) This is the minimum schedule idle time that must be available before a "Low" LTR value can be indicated. This value must be larger than LIWL 12:7 – Time value in # of 125µs Bus Intervals (0 – 8ms) 6:0 – Fractional BI Time value in µs (0 – 124µs)
15:13	RO	0	NA	Reserved
12:0	RW	0000h	Core	Low Idle Wake Latency (LIWL) This is the latency to access memory from the Medium Idle Latency state. 12:7 – Time value in # of 125µs Bus Intervals (0 – 8ms) 6:0 – Fractional BI Time value in µs (0 – 124µs)

Table 217. XECP_CMDM_CTRL_REG1 - Command Manager Control 1

Address Offset:818Ch-818Fh
Default Value:3510AFFCh
Access: RW;
Size:32 bits
This register contains fields which control the behavior of the Command Manager in the xHC.
The functions controlled by this register are made available largely for debug/diagnostic purposes. This configurability is above and beyond that defined in the xHCI specification.
NOT for EDS

Bit	Access	Default Value	RST/PWR	Description
31:28	RW	3h	Core	Bandwidth calculation parameter: Default bandwidth for an Interrupt endpoint.
27:24	RW	5h	Core	Bandwidth calculation parameter: Default bandwidth for an Isoch. Endpoint.
23	RO	0h	Core	Reserved
22	RW	0h	Core	Determine if stream context needs to be saved/restored due to the retry flag. Note: This is only needed when we've switched streams mid-TRB and have partial length to maintain
21	RW	0h	Core	Setting this field will cause the Configure Endpoint command to lock slot context to avoid contention with other active Endpoints on that same slot
20	RW	0h	Core	Setting this field will enable cause a Configure Endpoint Command to fail if the number of active EPs post configuration exceeds the maximum number of EPs available in cache
19	RW	0h	Core	Setting this field will prohibit the bandwidth computation during the Get Port Bandwidth command
18	RW	0h	Core	Setting this field will mask the system bandwidth checks during the bandwidth calculations
17	RW	0h	Core	Setting this field will mask the primary and secondary bandwidth checks during the bandwidth calculations

Bit	Access	Default Value	RST/PWR	Description
16	RW	0h	Core	0: Disable clearing of split state if TSP=1. 1: Enable clearing of split state if TSP=1
15	RW	1h	Core	0: Disable clearing other context during a disable slot command. 1: Enable clearing other context during a disable slot command.
14	RW	0h	Core	0: Disable evaluating the endpoint state during an Evaluate Context command 1: Enable evaluating the endpoint state during an Evaluate Context command.
13	RW	1h	Core	When context preservation (bit-12) is enabled: 0: Do not modify the retry bits. 1: Force the retry bits of the TRM context to 1.
12	RW	0h	Core	0: Disable context preservation 1: Enable context preservation for all commands based on the state of the TSP bit.
11	RW	1h	Core	0: Disable clearing other context during a configure endpoint command. 1: Enable clearing other context during a configure endpoint command.
10	RW	1h	Core	0: Disable clearing other context during a reset device command. 1: Enable clearing other context during a reset device command.
9	RW	1h	Core	0: Disable clearing other context during a reset endpoint command. 1: Enable clearing other context during a reset endpoint command.
8	RW	1h	Core	0: Disable clearing other context during an enable slot command. 1: Enable clearing other context during an enable slot command.
7	RW	1h	Core	0: Disable clearing TRM, Scheduler, and DMA context during a configure endpoint command. 1: Enable clearing TRM, Scheduler, and DMA context during a configure endpoint command.
6	RW	1h	Core	0: Disable clearing TRM, Scheduler, and DMA context during an address device command. 1: Enable clearing TRM, Scheduler, and DMA context during an address device command.
5	RW	1h	Core	0: Disable clearing TRM, Scheduler, and DMA context during an enable slot command. 1: Enable clearing TRM, Scheduler, and DMA context during an enable slot command.
4	RW	1h	Core	0: Disable clearing TRM, Scheduler, and DMA context during a reset device command. 1: Enable clearing TRM, Scheduler, and DMA context during a reset device command.
3	RW	1h	Core	0: Address device does not return the error for this condition. 1: Address device command returns a context state error when the EP is in the default state and BSR=1
2	RW	1h	Core	0: Disable clearing TRM, Scheduler, and DMA context during a set TR DQ pointer command. 1: Enable clearing TRM, Scheduler, and DMA context during a set TR DQ pointer command.
1	RW	0h	Core	0: Bandwidth calculation handled normally. 1: Forces a failure in the endpoint bandwidth calculation.

Bit	Access	Default Value	RST/PWR	Description
0	RW	0h	Core	0: Disable generation of the completion event. 1: Enable the command manager to generate a completion event after processing an update endpoint command.

Table 218. XECP_CMDM_CTRL_REG2 - Command Manager Control 2

Address Offset:8190h-8193h
Default Value:06C60000h
Access: RW;
Size:32 bits
This register contains fields which control the behavior of the Command Manager in the xHC. The functions controlled by this register are made available largely for debug/diagnostic purposes.
This configurability is above and beyond that defined in the xHCI specification.
NOT for EDS

Bit	Access	Default Value	RST/PWR	Description
31	RW	0h	Core	Set this field to write all 5dw of output context
30	RW	0h	Core	Enable Stop EP 2ms Timeout
29	RW	0h	Core	Enable Slot ID Overwrite
28	RW	0h	Core	State Save Error Generator
27	RW	0h	Core	0: Turn ON the TTE clock. 1: Turn OFF the TTE clock.
26	RW	1h	Core	0: Disable clearing other context during a stop endpoint command. 1: Enable clearing other context during a stop endpoint command.
25	RW	1h	Core	0: Disable clearing other context during stall handling. 1: Enable clearing other context during stall handling.
24	RW	0h	Core	0: Mask the Error Event reporting occurred due to STOP EP 100ms timeout in TRM 1: Enables the Error reporting Event occurrence as a result of STOP EP 100ms timeout in TRM Old definition (Prior to KBPH) 0: The internal context write dq pointer is updated normally (based on previous wr dqpointer) 1: The internal context write dq pointer value will be set to the read dq pointer value when the command manager updates internal context.
23	RW	1h	Core	0: Disable clearing TRM, Scheduler, and DMA context during a reset endpoint command. 1: Enable clearing TRM, Scheduler, and DMA context during a reset endpoint command.
22	RW	1h	Core	0: Disable hardware bandwidth calculations. 1: Enable hardware bandwidth calculations.
21	RW	0h	Core	0: Delay processing command ring TRB while internal context requests are pending. 1: Process command ring TRBs normally.
20	RW	0h	Core	0: Disable clearing other context during a set dq pointer command. 1: Enable clearing other context during a set dq pointer command.
19	RW	0h	Core	0: Check the slot and endpoint state prior to processing a reset endpoint command. 1: Ignore the slot and endpoint state when processing a reset endpoint command.

Bit	Access	Default Value	RST/PWR	Description
18	RW	1h	Core	0: Disable sequence number preservation during set dq pointer command. 1: Enable sequence number to be preserved during set dq pointer command.
17	RW	1h	Core	0: Disable stop endpoint command interruption. 1: Enable stop endpoint command to be interrupt if the command is not completing normally.
16	RW	0h	Core	0: Pending commands have a higher priority than update endpoint processing. 1: Update endpoint processing in the command manager has a higher priority than pending commands. Note: Enabling this bit can prevent prolonged stall handling.
15	RW	0h	Core	0: Stall handling does clear the EP context fields. 1: Stall handling does not clear the EP context fields.
14	RW	0h	Core	0: Force the default burst size to be 1 when clearing context. 1: Force the default burst size to be the defined maximum burst size when clearing context.
13:0	RW	0h	Core	Clear state machine present state: Setting a bit in this field to 1, will reset the specified command manager state machine to the starting/idle state. bit-0: disable slot state machine bit-1: enable slot state machine bit-2: reset endpoint state machine bit-3: reset device state machine bit-4: command ring state machine bit-5: stop endpoint state machine bit-6: set dq pointer state machine bit-7: force header state machine bit-8: evaluate context state machine bit-9: update endpoint state machine bit-10: address device state machine bit-11: port bandwidth state machine bit-12: read output context state machine bit-13: configure endpoint state machine

Table 219. XECP_CMDM_CTRL_REG3 - Command Manager Control 3

Address Offset:8194h-8197h
Default Value:0020505Ah
Access: RW;
Size:32 bits
This register contains fields which control the behavior of the Command Manager in the xHC. The functions controlled by this register are made available largely for debug/diagnostic purposes.
This configurability is above and beyond that defined in the xHCI specification.
NOT for EDS

Bit	Access	Default Value	RST/PWR	Description
31	RW	0h	Core	RESERVED

Bit	Access	Default Value	RST/PWR	Description
30	RW	0h	Core	Default Control EP double counting Enable. When cleared, Control EP accounting is not enabled. If this feature is disabled, it implies that the Default Control EP accounting is comprehended through the BW Check, thus it has to be enabled via 805C[22], otherwise Default Ctrl EP's will not be accounted for. This allows for a usage where BW Check is disabled in HW while requiring HW to enforce EP resource check. This bit also controls ignore_hi_atomic_en functionality.
29:26	RW	0h	Core	RESERVED
25	RW	0h	Core	Setting this bit enables a mode to clear local LCStreamID as a part of StopEP cmd for StreamEP
24:22	RW	0h	Core	RESERVED
21	RW	1h	Core	stop_ep_clr_stream_st_en_reg
20	RW	0h	Core	Setting this field will prohibit the Command Manager from locking context during the execution of either Stop Endpoint, Reset Device, Disable Slot, Evaluate Context or Configure Endpoint commands
19	RW	0h	Core	Setting this field will cause both the IDMA & ODMA engines to stop their transaction timers when the Command Manager is executing a Stop Endpoint Command since they may be locked out of context
18	RW	0h	Core	Setting this field will enable DMA context to be cleared during a Disable Slot command
17:16	RW	0h	Core	This field determines the amount of wait time inserted at the end of a Disable Slot command prior to signaling a completion on the command ring. 0: Disabled 1: 100us 2: 9ms 3: 10ms
15:8	RW	50h	Core	Bandwidth calculation parameter: Default high speed bandwidth to advertise on each port.
7:0	RW	5Ah	Core	Bandwidth calculation parameter: Default bandwidth to advertise on each port.

Table 220. PDDIS – xHC Pull Down Disable Control

Address Offset: 8198h – 819Bh
Access: RO; RW
Size: 32b

Bit	Access	Default Value	RST/PWR	Description
31:NumUSB2	RO	00h	USB	Reserved

Bit	Access	Default Value	RST/PWR	Description
(NumUSB2-1):0	RW	0b	SUS	PDDISEN: Allow USB Pulldown disable Each bit corresponds to a USB2 port indexed by the bit number (zero based). Bit 0 = USB2 port 1 Bit 1 = USB2 port 2 Etc. When set, allow the pulldown on D+ or D- (as appropriate) to be disabled when the port is connected and in L2. This bit does not apply to eUSB2 ports, or shared USB2/ eUSB2 ports that are in eUSB2 mode.

Table 221. THROTT –XHCI Throttle Control

Address Offset: 819Ch – 819Fh
Access: RO; RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31	RW	0b	Core	Thermal Throttle TRM Advance 0: TRM will use a Thermal Throttle indication from the Scheduler to perform a "Thermal Throttle Advance" and generate a Missed Service Error. 1: (Chicken-bit operation) TRM will ignore Thermal Throttle signal from the Scheduler. Note: Asserting this bit will cause Thermal Throttling to be non-functional and should only be used if Thermal Throttling breaks normal operation
31:28	RO	00h	Core	Reserved
27	RW	0b	Core	Thermal Throttle Periodic Active LPM Masking 0: The "Periodic Active LPM" indication to USB2 ports is masked when the Thermal Throttle Powerdown is asserted 1: (Chicken-bit operation) "Periodic Active LPM" signal is not masked by the Thermal Throttle Powerdown signal.
26	RW	0b	Core	Thermal Throttle Command Manager IDLE Detection 0: Thermal Throttling indication to the ports will only assert if the Command Manager is IDLE. The deassertion of Command Manager IDLE during the "Off" portion of the Thermal Throttle window will not cause the Thermal Throttling indication to the ports to deassert. 1: (Chicken-bit operation) Thermal Throttle indication to the ports does not consider Command Manager IDLE.
25	RW	0b	Core	Thermal Throttle Backbone Clock Gate Detection 0: If the Backbone Clock used by the Scheduler is local clock gated when the Thermal Throttle window enter the "Off" portion, assert the Thermal Throttle indication to the ports. 1: (Chicken-bit operation) Thermal Throttle indication to the ports does not consider Backbone Clock gating.

Bit	Access	Default Value	RST/PWR	Description
24	RW	0b	Core	Thermal Throttle Fine/Coarse IDLE Duration 0: Thermal Throttle indication to the ports will assert when Thermal Throttle window is in the "Off" portion and all IDLE indications are asserted. 1: (Chicken-bit operation) Thermal Throttle indication to the ports will assert only at the BI boundary when the Thermal Throttle window enters the "Off" portion and all IDLE indications are asserted. For both settings, Thermal Throttle indication to the ports can only deassert at the BI boundary when the Thermal Throttle window enters the "On" portion.
23:21	RW	000b	Core	Reserved
20	RW	0b	Core	SSIC Thermal Throttle Ux Mapping Controls if U1 or U2 is forced upon the start of thermal throttle OFF period. 0 - Force ports into U2 during Thermal Throttle triggered Ux entry. 1 - Force ports into U1 during Thermal Throttle triggered Ux entry.
19:18	RW	0b	Core	USB3 Thermal Throttle Ux LGO delay Controls the delay enforced between LMP for FLPMA and LMP for Ux LGO. After sending LPMA ON , wait for pre-defined number of clocks to initiate LGO_U1/LGO_U2 00: 8 clocks 01: 32 clocks 10: 128 clocks 11: 0 clocks This field does not apply to ports that are not operating in the mode required to issue FLMA ON.
17	RW	0b	Core	Thermal Throttling Disable 0: Thermal throttling is enabled. 1: Thermal throtling is disabled. The host controller ignores the TT control inputs and does not throttle.
16	RW	0b	Core	USB3 Thermal Throttle Ux Mapping Controls if U1 or U2 is forced upon the start of thermal throttle OFF period. 0 - Force ports into U2 during Thermal Throttle triggered Ux entry. 1 - Force ports into U1 during Thermal Throttle triggered Ux entry.
15	RW	0b	Core	Throttle Priority Mode 0: "Off" period has priority: In this case, when the throttle signal is asserted, the host controller enters the "off" state on the next uframe boundary, and stays in the off state for the prescribed duration or until the end of the 16 uframe throttle period - whichever occurs first. On subsequent throttle periods, the off period occurs first and then the on period. 1: The "On" period has priority: In this case, when the throttle signal is asserted, the host controller completes the required On period first before entering the off period. If the required number of uFrames has already been executed in a 16 uframe throttle window, the controller enters the off period immediately.

Bit	Access	Default Value	RST/PWR	Description
14	RW	0b	Core	Disable Force L1 when throttled. 1: USB2 port will not force L1 entry on throttled ports. L1 entry will be based on the normal idle timeout 0: USB2 ports will attempt to enter L1 immediately after throttled ports are idle.
13	RW	0b	Core	Disable Interrupt Throttling 0: Interrupt traffic is throttled 1: Interrupt traffic is not throttled
12	RW	0b	Core	Disable Isochronous Throttling 0: Isochronous traffic is throttled 1: Isochronous traffic is not throttled
11:8	RW	0h	Core	T1 Action: # bus intervals to be idle for async traffic out of the 16 interval master period; from 0 to 15.
7:4	RW	0h	Core	T2 Action: # bus intervals to be idle for async traffic out of the 16 interval master period; from 0 to 15.
3:0	RW	0h	Core	T3 Action: # bus intervals to be idle for async traffic out of the 16 interval master period; from 0 to 15. Note: this value shall never bet set to exceed throttling of more than 14 uFrames. It implies that we will have at least 2 un-throttled micro frames.

Table 222. LFPSPM - LFPS PM Control

Address Offset:81A0h-81A3h
Default Value:0h
Access: RW;
Size:32 bits
This register is subject to HW save and restore.

Bit	Access	Default Value	RST/PWR	Description
31:NumUSB3	RO	0h	SUS	Reserved
(NumUSB3-1):0	RW	0h	SUS	LFPS Power Management in U3 Enable This field allows xHC to turn off LFPS Receiver when the port is in U3. This allows the Host Controller to save some extra power (about 200µW per port) in idle states if device connected on a port is not Resume capable or Resume enabled. This choice has to be done by BIOS and based on platform knowledge. For example, if an in-box device is not Resume Capable, BIOS could allow xHC to turn-off Rx LFPS when the port is in U3. Each bit represents a port. Bit [0] is for USB3.0 Port 1, Bit [1] is for USB3.0 Port 2 and so on. '0' in a bit position: LFPS Receiver shall be kept enabled when the port is in U3. '1' in a bit position: LFPS Receiver shall be disabled when the port is in U3.

Table 223. U2PDM –USB2 Port Disconnect Mask

Address Offset: 81A4h – 81A7h
Access: RO; RW;

Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:NumUSB2	RO	00h	SUS	Reserved
(NumUSB2-1):0	RW	0b	SUS	USB2 Port Disconnect Mask Per Port Control to allow for masking of port dis-connect events. 0: Do not mask Port Dis-Connect 1: Mask Port Dis-Connect by masking CSC from being set and suppressing PME due to the disconnect. PLS and CCS will reflect the true port state.

Table 224. U2PCM –USB2 Port Connect Mask

Address Offset: 81A8h – 81ABh
Access: RO; RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:NumUSB2	RO	00h	SUS	Reserved
(NumUSB2-1):0	RW	0b	SUS	USB2 Port Connect Mask Per Port Control to allow for masking of port connect events. 0: Do not mask Port Connect 1: Mask Port Connect by masking CSC from being set and suppressing PME due to the connect. PLS and CCS will reflect the true port state.

Table 225. U3PDM –USB3 Port Disconnect Mask

Address Offset: 81ACh – 81AFh
Access: RO; RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:NumUSB3	RO	00h	SUS	Reserved
(NumUSB3-1):0	RW	0b	SUS	USB3 Port Disconnect Mask Per Port Control to allow for masking of port dis-connect events. 0: Do not mask Port Dis-Connect 1: Mask Port Dis-Connect by masking CSC from being set and suppressing PME due to the disconnect. PLS and CCS will reflect the true port state.

Table 226. U3PCM –USB3 Port Connect Mask

Address Offset: 81B0h – 81B3h
Access: RO; RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:NumUSB3	RO	00h	SUS	Reserved

Bit	Access	Default Value	RST/PWR	Description
(NumUSB3-1):0	RW	0b	SUS	USB3 Port Connect Mask Per Port Control to allow for masking of port connect events. 0: Do not mask Port Connect 1: Mask Port Connect by masking CSC from being set and suppressing PME due to the connect. PLS and CCS will reflect the true port state.

Table 227. THROTT2 –XHCI Throttle Control2

Address Offset: 81B4h – 81B7h
Access: RO; RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:NumUSB3	RO	00h	Core	Reserved
(NumUSB3-1):0	RW	All 1's	Core	Thermal Throttle Force LPM Accept Enable Per Port Control to allow for enforcement to be based on device detection if certain devices do not support FLPMA. 0: Do not set FLPMA prior to Ux entry due to TT 1: Set FLPMA prior to Ux entry due to TT

Table 228. LFPSONCOUNT – LFPS On Count

Address Offset: 81B8h – 81BBh
Access: RW;

Bit	Access	Default Value	RST/PWR	Description
31:22	RW	0	SUS	RSVD
21	RW	0	SUS	RTLCLKGENOVERRIDE When set, it will keep RTC tick generation gated unconditionally. This will be used by software to disable the tick and CRO if WDE/WCE is disabled during D3.
20	RW	0	SUS	Chicken bit when set will allow Gated SS Link to send the LFPS even though AON owns the LFPS detection
19	RW	0	SUS	RSVD
18	RW	1h	SUS	RTCCLKGENCTRL 0 - Keep RTC tick generation and RxDetect enable for all the disconnected port. This can be used as a W/A to wake CRO at regular interval. 1 - Gate RTC tick generation when all the host controller ports are disconnected, port ownerships are not with XHCI. Ungate it if either one of the port ownership comes back to XHCI.

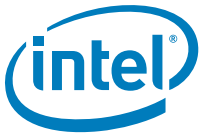
Bit	Access	Default Value	RST/PWR	Description
17:16	RW	0h	SUS	XU2P3LPSC (U2P3 LFPS Periodic Sampling Control) This field controls the OFF time for the LFPS periodic sampling for SS and SSIC ports in U2P3. If LFPSPM for a port is '1', it will override the OFF time and LFPS receiver will remain OFF permanently. For Fast Sim mode, 500us will be equivalent to 5us. 0x0 – Polling Disable. (RXDET Polling will become 100ms.) 0x1 – 500us OFF Time 0x2 – 1ms OFF Time 0x3 – 1.5ms OFF Time
15:10	RW	08h	SUS	XLFPSONCNTSSIC (LFPS ON Count for SSIC Ports) This time would describe the number of clocks SSIC LFPS will remain ON. SSIC LFPS detection operation may be carried out on using RTC clock or Oscillator clock. The value of this register should be adjusted accordingly. For RTC recommended value is 2. For Oscillator clock, recommended value is 8.
9:0	RW	0C8h	SUS	XLFPSONCNTSS (LFPS ON Count for SS Ports) This time would describe the number of clocks LFPS will remain ON. LFPS detection operation may be carried out on using RTC clock or Oscillator clock. The value of this register should be adjusted accordingly. For RTC recommended value is 2. For Oscillator clock, recommended value is 200.

Table 229. D0i2CTRL – D0i2 Control Register

Address Offset: 81BCh – 81BFh
Access: RO, RW;
Size:32 bits
Chassis Restore: S0iX (Regular)
Restore Group: VNNAON

Bit	Access	Default Value	RST/PWR	Description
31	RW	0h	SUS	USB2 Back to Back BTO Handling Enable When set enables handling of back to back Bus Time Out response generation by USB2 Port logic for Tx packets under conditions when packets cannot be sent on the link.
30	RW	0h	SUS	Reserved

Bit	Access	Default Value	RST/PWR	Description
29:26	RW	4h	SUS	D0i2 Entry Hysteresis Timer This field allows for a hysteresis timer to be implemented specifically for . This will allow for D0i2 entry to be controlled independently from the timer used for D0i3 and D3. 0h - Disabled 1h - 8 clocks 2h - 16 clocks 3h - 32 clocks 4h - 64 clocks 5h - 128 clocks 6h - 256 clocks 7h - 512 clocks
25:22	RW	2h	SUS	D0i2 Minimum Residency This field controls the minimum time that we must stay in to ensure that the entry sequence has settled before we attempt to exit. 0h - Disabled 1h - 8 clocks 2h - 16 clocks 3h - 32 clocks 4h - 128 clocks 5h - 256 clocks 6h - 512 clocks 7h - 1024 clocks
21	RW	0b	SUS	Active Periodic EP Disable This field allows the xHC to control how aggressive it enters D0i2 in the presence of active Periodic EP's. Setting this field will allow D0i2 only when there are no active Periodic EP's on the schedule. Either there are no active DB or any active Interrupt EP is flow controlled.
20:16	RW	2b	SUS	MSI D0i2 Pre Wake Time (MSID0I2PWT) This is the latency that is expected to be incurred to exit the D0i2 state. This wake latency is the latency to be added to the tracked D0i2 wake by the MSI module. Example: If while allowing D0i2 there is an MSI generation that will trigger in 250 us from now, the MSI module will trigger a D0i2 wake up 250 us – "MSI D0i2 Pre Wake Time". The D0I2WL is to ensure that the act of D0i2 exit does not impact the action(s) required by the alarm(s) that was enabled prior to D0i2. 3:0 – 250 ns ticks 0h – 0 ns 1h – 250 ns …. 1Fh – 3750 ns



Bit	Access	Default Value	RST/PWR	Description
15:4	RW	4Bh	SUS	MSI Idle Threshold This field allows the xHC to control how aggressive it enters D0i2 in the presence of pending MSI. This field is valid only if Pending MSI Disable is "0", allowing D0i2 in the presence of pending MSI's. D0i2 will be prevented if the amount of idle time between Event Ring being idle to the time an MSI will be generated does not exceed this time. Register Format: Bits [11:0] # 250 ns ticks
3	RW	0h	SUS	Pending MSI Disable This field allows the xHC to disable D0i2 when there are pending MSI's in the event manager. Setting this field will require all IMOD counters to be 0h and all MSI's delivered. Clearing this field will allow for D0i2 power gating while there are 1 or more IMOD counters decrementing which implies that an MSI is pending and will be generated once the corresponding IMOD counter reaches 0h.
2	RW	0h	SUS	Frame Timer Run Disable This field allows the xHC to disable D0i2 when the frame timer is running. Clearing this field will allow D0i2 when the frame timer is required as defined in the XHCI Spec. Setting this field will not allow D0i2 when the frame timer is required and will limit D0i2 for the condition where the frame timer is not required.
1	RW	0h	SUS	USB2 L1 Disable This field allows the xHC to disable D0i2 when USB2 ports are in L1. This implies that D0i2 will only be triggered when ports are in L2 or deeper.
0	RW	0h	SUS	USB3 U2 Disable This field allows the xHC to disable D0i2 when USB3 ports are in U2. This implies that D0i2 will only be triggered when ports are in U3 or deeper.

Table 230. D0i2SchAlarmCtrl – D0i2 Scheduler Alarm Control Register

Address Offset: 81C0h – 81C3h
Access: RO,RW;
Size:32 bits
Chassis Restore: S0iX (Regular)
Restore Group: VNNAON

Bit	Access	Default Value	RST/PWR	Description
31	RW	0b	SUS	Disable Active Async D0i2 Request During THT 0: The presence of an Active Asynchronous Endpoint while in a Thermal Throttling window will generate a request for the VNN domain clock to allow for Thermal Throttling counter to continue to increment. The presence of an Active Asynchronous Endpoint while not in a Thermal Throttling window will disable D0i2 entry. This will allow for D0i2 exit after the end of the Thermal Throttling window. 1: (Chicken-bit operation) The above two operations are disabled. Note: This bit was created for GEN2 HSD 1503900568.
30:29	RW	0h	SUS	Reserved
28:16	RW	0000h	SUS	D0i2 Idle Time (D0I2IT) This is the minimum schedule idle time that must be available before D0i2 can allowed. 12:7 – Time value in # of 125µs Bus Intervals (0 – 8ms) 6:0 – Fractional BI Time value in µs (0 – 124µs) This field controls how much scheduler idle time is required to trigger D0i2. The scheduler idle time is the same idle time that is used by other functions implementing alarm timers such as PLL shutdown, LTR and USB2 L1 override. If there is a need to require other alarm timers to have been set such as LTR has triggered a Low Idle time, then this field needs to be as aggressive as LTR Low Min Idle Time to ensure D0i2 is triggered once the scheduler has detected IDLE in the schedule. This is only to be used as alternate modes of operation or back up modes.
15:13	RW	000b	SUS	Reserved
12:0	RW	0000h	SUS	D0i2 Wake Latency (D0I2WL) This is the latency that is expected to be incurred to exit the D0i2 state. This wake latency is the latency to be added to the tracked D0i2 wake by the scheduler. Example: If while allowing D0i2 there is an alarm that will trigger in 250 us from now ,the scheduler will allow D0i2 and track this alarm with an adjustment to wake up 250ns – D0I2WL) from. The D0I2WL is to ensure that the act of D0i2 exit does not impact the action(s) required by the alarm(s) that was enabled prior to D0i2. 12:7 – Time value in # of 125µs Bus Intervals (0 – 8ms) 6:0 – Fractional BI Time value in µs (0 – 124µs)

Table 231. USB2PMCTRL – USB2 Power Management Control

Address Offset: 81C4h – 81C7h
Access: RW;

Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31	RW	0h	SUS	0 - Enable RF Power gating bug fix (Default) 1 - Disable RF Power gating bug fix
30:13	RW	0h	SUS	Reserved
12	RW	0h	SUS	USB2 HOST PHY UTMI Clock Gate Disable Policy This controls the policy for Host PHY UTMI Clock Gating. When Set HOST PHY UTMI Clock Gating is disabled else Host PHY UTMI Clock Gating is enable
11	RW	0h	SUS	USB2 PHY SUS Power Gate PORTSC Block Policy (U2PSPGPSCBP) This controls the policy for blocking PORTSC Updates while the USB2 PHY SUS Well is power gated. When set, the controller will block any updates to the PORTSC caused by port status change if the USB2 PHY SUS is power gated. 0 – Do not
10:8	RW	0h	SUS	USB2 PHY SUS Well Power Gate Entry Hysteresis Count (U2PSPGEHC) This controls the amount of hysteresis time the controller will enforce after detecting the USB2 PHY SUS Power Gate entry condition. 0h – 0 clocks 1h – 32 clocks 2h – 64 clocks 3h – 128 clocks 4h – 256 clocks 5h – 512 clocks 6h – 1024 clocks 7h – 2048 clocks
7:4	RW	0h	SUS	USB2 Common Lane Power Gate Latency (U2CLPGLAT) This field represents the worst case latency for the USB2 Common Lane to enter and exit its power gate state. This fields is required to be compared to a ports HIRD/HIRD value for the ports that have allowed L1 to L2 mapping to determine if the Common Lane can be allowed to power off. If the power gate entry/exit latency is greater than the HIRD/HIRDD then the common lane should not be allowed to power gate as this will result in a L1 exit violation. 0h – 100 us 1h – 200 us 2h – 300 us … Eh – 1500us Fh – 1600 us

Bit	Access	Default Value	RST/PWR	Description
3:2	RW	0h	SUS	USB2 PHY SUS Well Power Gate Policy (U2PSUSPGP) This field controls when to enable the USB2 PHY SUS Well Power Gating when the proper conditions are met. 00 – USB2 PHY SUS Power Gating is Disabled. 01 – NA 10 – USB2 PHY SUS Power Gating is Enabled in only in D3 and D0i3 11 – USB2 PHY SUS Power Gating is Enabled in D0/D0i2/D0i3/D3
1	RW	0h	SUS	USB2 Common Lane Power Gating Enable During L1 to L2 Mapping for USB2 PHY Power Gating (U2CLPGEL1L2) This field when set enables the controller to allow for the common lane power gating to be enabled when all ports are exposed as in L2 to the USB2 PHY while at least 1 port has been mapped to L2 from L1. This field alone does not guarantee power gating since the L1 HIRD/HIRDD Value must be compared with the PHY's power gate exit latency (U2CLPGLAT) held in this register to ensure that L1 exit is not violated. 0 – USB2 Common Lane Power Gating is disabled when any port has been mapped from L1 to L2. 1 – USB2 Common Lane Power Gating is allowed when any port has been mapped to L2 from L1 with the additional condition that the HIRD/HIRDD is greater than the PHY's Power Gate exit latency.
0	RW	0h	SUS	USB2 Data Lane L1 to L2 Mapping Enable for USB2 PHY Power Gating (U2DLL1L2ME) This field when set enables the controller to map an L1 entry directly to L2 to allow the USB2 PHY to trigger its Autonomous Power Gating. The USB2 PHY will trigger PG only when in L2 since it does not fully understand the requirements for L1. 0 – USB2 L1 to L2 mapping is disabled for all ports 1 – USB2 L1 to L2 mapping is enabled for all ports

Table 232. AUX_CTRL_REG3 - Aux PM Control Register 3

Address Offset:81C8-81CBh
Default: h
Access: RW;
Size:32 bits
Chassis Restore: S0iX (Regular)
Restore Group: VNNAON

Bit	Access	Default Value	RST/PWR	Description
31:28	RW	0h	SUS	RESERVED FOR FUTURE USE
10	RW	0h	SUS	ACCTRL based PG disable override Disable When cleared, will prevent D0i2/D0i3 PG'ing in the absence of ACCTRL being set by BIOS. When set, will D0i2/D0i3 PG'ing even in the absernce of ACCTRL being set by BIOS. Note that this doesn't affect/prevent D3, ForcePG, Function disable based PG'ing flow. Note that this will prevent subsequent D0i2 entry right after D3/ Sx exit (even though the D0i2 entry conditions are met) till driver initiated "restore" flow completes.
9:7	RW	0h	SUS	IP-Inaccessible Hysteresis Timer 000 : 50us 001 : 100us 010 : 150us 011 : 200us 000 : 250us 001 : 300us 010 : 350us 111 : 400us
6	RW	0h	SUS	Reset Prep Override Disable When cleared, will allow for reset prep to be ACK'ed regardless of the state of the controller i.e. controller may not have prepared for reset. When set, will require reset prep to be ACK'ed only when the controller has prepared for reset.
5:2	RW	3h	SUS	CDH Aggregation Minimum Wait Time This field controls the minimum time that we must wait for resets to propagate before allowing Power Up flow to complete. The Power Up flow requires special handling of clocks, reset and sleep signaling which requires the CDH to monitor reset propagation. This timer allow for flexibility on when we consider all resets propagated. 0h - Disabled 1h - 2 clocks 2h - 4 clocks 3h - 8 clocks 4h - 16 clocks 5h - 32 clocks 6h - 64 clocks 7h - 128 clocks

Bit	Access	Default Value	RST/PWR	Description
1	RW	0h	SUS	CDH Reset Propagation Aggregation Control This bit will indicate the mode of operation for the CDH Reset Propagation Aggregator. It allows for a mode where the aggregation will wait for an indication from each CDH before proceeding OR ignore the CDH indication before proceeding. Regardless of the mode, the aggregator will enforce the CDH Aggregation Mini Wait Time. 0 - Aggregate all the CDH indications before triggering the CDH Aggregation Mini Wait Time. Once the Min Wait Time is met a notification to the Power Sequencer/Control will be initiated 1 - Trigger the CDH Aggregation Mini Wait Time w/o waiting for CDH indication. Once the Min Wait time is met a notification to the Power Sequencer/Control will be initiated.
0	RW	0h	SUS	MMP_PFET_REQ_OVRD This bit will disable the MMP PFET request condition for PGCB control. 1 - MMP PFET Request Ignored 0 - Default

Table 233. AUX_CTRL_REG4 - Aux PM Control Register 4

Address Offset:81CC-81CFh
Default: 00000000h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:0	RW	0h	SUS	RESERVED FOR FUTURE USE

Table 234. TRB_PRF_CTRL_REG1 –TRB Prefetch Control Register 1

Address Offset:81D0-81D3h
Default: 0h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:26	RW	0h	Core	Reserved
25	RW	1b	Core	Disable LINK TRB fix related to sync'ing CPL Ptr with Xfer Ptr in TRB-$.
24	RW	0h	Core	Enable/disable DB vs EOR race condition where DB arrives little after the EOR is committed to TRM. When set, the fix for the race condition will be disabled and in that case we will have to set bit '23' of this register to avoid the race condition issue. Note that this change hasn't made into AR A0, A1 and B0 steppings.
23	RW	0b	Core	Enable/disable stale reporting of EOR to TRM Xfer Engine. When set, the TRB-$ will assert special indication to TRM Xfer engine while returning EOR TRB which indicates that the EOR is returned from Cache.

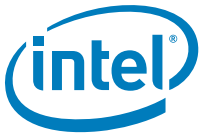
Bit	Access	Default Value	RST/PWR	Description
22	RW	0b	Core	Disable TRM to re-fetch EOR directly from system memory when TRB-$ returned EOR. 1 : Disable TRM to re-fetch EOR directly from memory when TRB-$ returned EOR 0 : Let TRM re-fetch EOR from memory every time EOR is returned by the TRB-$
21	RW	0b	Core	Enable descending order for cache replacement. 0 : Cache replacement follow Ascending order 1 : Cache replacement follow Descending order
20	RW	0b	Core	Disable the DB race condition fix - The race condition is DB ring arrive before TRB prefetch CPL which has Invalid TRB for which the DB is rung. Default is fix enable.
19	RW	0b	Core	Block prefetch until all outstanding TRB fetch CPLs come back when we detect DB race condition where SW DB ring arrives before the corresponding TRB that was read Invalid. This applies when we are enabled to issue multiple prefetches for same EP (i.e., bit 18 is set to '1').
18	RW	0b	Core	Unique TAG for each OS prefetch request (PCI mode): The field enables/disables the "Fix" vs "Unique TAG" mode for each OS prefetch request. As a PCI Endpoint, the controller shall be configured to use "Unique TAG" for each outstanding prefetch request. As an IOSF Endpoint, the controller can be configured to use "Fix" tagging mode for performance reasons. 0 : Use "Unique TAG" for each OS prefetch request 1 : Use "Fix" TAG for each OS prefetch request Note, this bit is NOT implemented in AR.
17:13	RW	0Fh	Core	Max OS prefetch request: This controls the number of outstanding TRB prefetch request that is allowed. This is zero based. 0Fh - Allow upto 16 OS prefetch requests 0Eh - Allow upto 15 OS prefetch requests …. 00h - Allow only 1 OS prefetch request This field is ONLY valid when bit-18 of this register is set to '0' (i.e., PCI mode TAG'ing is selected). When configured to use "Fix" Tag, the number of outstanding prefetch request is fixed to 16 and setting of this register becomes DON'T CARE.
12:9	RW	4h	Core	This allows to program minimum distance between two (2) Link TRBs that the cache supports without causing the entry invalidation. Setting to any value less than 4h will lead to undefined behavior.
8:6	RW	5h	Core	This allows to program number of past TRBs to be kept in the cache from the current Xfer pointer.
5	RW	0h	Core	Disable TRB-$ for CTRL EPs – Setting this bit disable TRB caching for control EPs. When set, all control EP's TRB request to TRB-$ will take bypass path. 0 : Enable TRB-$ for CTRL EPs 1 : Disable TRB-$ for CTRL EPs

Bit	Access	Default Value	RST/PWR	Description
4	RW	0h	Core	Disable multiple Outstanding prefetch request per EP When set, it disables issuing multiple prefetch requests and serializes the prefetch for a given EP. In other word, there will be only one prefetch request outstanding per EP. 0 : Enable multiple prefetches per EP. 1 : Disable multiple Outstanding prefetch requests per EP
3	RW	0h	Core	Disable TRB cache's "Defer" response generation capability. When set, TRB Cache will not return "Defer" response to TRM Xfer engine's TRB request upon cache miss or when the requested TRB is not available in cache to serve. 0 : TRB Cache will generate "Defer" response if the requested TRB is not available in the cache 1: Disable "Defer" response generation capability. In this case, the TRB cache will generate response back when the TRB is available.
2	RW	0b	Core	Enable Cache Bypass for Cache Full : This mode enables TRB Cache bypass path when the cache is full and no entry is in the state that can be flushed/replaced. In that case, this mode will allow TRM to make progress on this new EP who's TRB fetch request resulted in cache miss and no cache resource available for allocation. 0 : Disable the bypass path. In this mode, the cache always waits for the state where one entry is available to be flushed/replaced. 1: Enable the bypass path.
1	RW	0b	Core	Disable Link TRB Traversal : The field enables/disable TRB Prefetcher to prefetch/traverse beyond the Link TRB. 0 : Enable prefetching beyond Link TRB 1 : Disable prefetching beyond Link TRB
0	RW	0b	Core	TRB Prefetcher Enable : This field enables/disables the TRB Prefetch feature. 0: Disable TRB Prefetcher 1: Enable TRB Prefetcher

Table 235. TRB_PRF_CTRL_REG2 –TRB Prefetch Control Register-2

Address Offset:81D4-81D7h
Default: 20100410h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:30	RW	0h	Core	Reserved



Bit	Access	Default Value	RST/PWR	Description
29:24	RW	20h	Core	Max Prefetch (TRB) EPs Cache depth This controls the number of EPs whose TRBs can be cached. Setting it to smaller than the actual cache depth will effectively reduce the cache depth and impact the performance.
23:21	RW	0h	Core	Reserved These ones are spare bits for future scalability
20:16	RW	10h	Core	Max TRB prefetch (per EP) – This allows us to control number of TRBs that can be prefetched and cached at a given time for EPs. The value set in this field is in term of number of TRB.
15:13	RW	0h	Core	Reserved These ones are spare bits for future scalability
12:8	RW	4h	Core	Min TRBs per prefetch read – This allows us to control Min number of TRBs that is required to be fetched as a part of single prefetch read request to avoid smaller size prefetches. This is mainly to efficiently use the read credit on IOSF/Backbone. The value set in this field is in term of number of TRBs. Note that, each TRB is 16B wide. Note that, the behavior will be undefined if set to 0. Make sure to set this value smaller than "Max TRBs per prefetch read" field. The behavior will be undefined if it is not followed.
7:5	RW	0h	Core	Reserved These ones are spare bits for future scalability of "Max TRB per prefetch read" field due to cache size increase.
4:0	RW	10h	Core	Max TRBs per prefetch read – This allows to control Max number of TRBs that can be fetched in single prefetch read request. The value set in this field is in term of number of TRBs. Note that, each TRB is 16B wide. Note that, the behavior will be undefined if set to 0. Also, the value in this field should be chosen such so the controller doesn't violate the MaxRdReqSize setting. Formula – Max number of TRBs per read <= (MaxRdReqSize / 16)

Table 236. TRB_PRF_CACHEINV_REG – TRB Prefetch Cache Invalidation Register

Address Offset:81D8-81DBh
Default: 0h
Access: RW;

Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31	RW1S	0h	Core	Invalidate/Flush the entire TRB Cache. When this is set, the Slot ID and EP ID fields of the register is don't care. SW sets this bit to trigger a Cache wide entry invalidation. HW will clear this bit once the Cache invalidation is complete.
30	RW1S	0h	Core	Invalidate/Flush TRB Cache for EP specified by Slot ID and EP ID fields of the register. SW sets this bit to trigger a specific entry invalidation. HW will clear this bit once the Cache invalidation is complete.
29:24	RW	0h	Core	Reserved
23	RW	0h	Core	Enable TRB-$ flushing for Disable Slot command. 0 : Disable flushing of TRB-$ for Disable Slot. 1 : Enable flushing of TRB-$ for Disable Slot. Always set it to 0 if TRB PRF Cache feature is disabled or not supported.
22	RW	0h	Core	Enable TRB-$ flushing for Stop EndPoint command. 0 : Disable flushing of TRB-$ for Stop Endpoint. 1 : Enable flushing of TRB-$ for Stop Endpoint. Always set it to 0 if TRB PRF Cache feature is disabled or not supported.
21	RW	0h	Core	Enable TRB-$ flushing for SetTRDQPointer Command. 0 : Disable flushing of TRB-$ for SetTRDQPointer. 1 : Enable flushing of TRB-$ for SetTRDQPointer. Always set it to 0 if TRB PRF Cache feature is disabled or not supported.
20	RW	0h	Core	Enable TRB-$ flushing for Update EndPoint (cases that triggers EP state change and stream switch etc). 0 : Disable flushing of TRB-$ for Update EndPoint. 1 : Enable flushing of TRB-$ for Update EndPoint. Always set it to 0 if TRB PRF Cache feature is disabled or not supported.
19	RW	0h	Core	Enable TRB-$ flushing for Reset EndPoint command. 0 : Disable flushing of TRB-$ for Reset Endpoint. 1 : Enable flushing of TRB-$ for Reset Endpoint. Always set it to 0 if TRB PRF Cache feature is disabled or not supported.

Bit	Access	Default Value	RST/PWR	Description
18	RW	0h	Core	Enable TRB-$ flushing for Reset Device command. 0 : Disable flushing of TRB-$ for Reset Device. 1 : Enable flushing of TRB-$ for Reset Device. Always set it to 0 if TRB PRF Cache feature is disabled or not supported.
17	RW	0h	Core	Enable TRB-$ flushing for Config EndPoint command. 0 : Disable flushing of TRB-$ for Config EndPoint. 1 : Enable flushing of TRB-$ for Config EndPoint. Always set it to 0 if TRB PRF Cache feature is disabled or not supported.
16	RW	0h	Core	Enable/Disable full handshake for TRB-$ flush. 0 : Enable full handshake 1 : Disable full handshake Always set it to 1 if TRB PRF Cache feature is disabled or not supported.
15:13	RW	0h	Core	Reserved
12:8	RW	0h	Core	EP ID : EP Id (in DCI format) of EP that is requested to be invalidated
7:0	RW	0h	Core	Slot ID : Slot ID of EP that is requested to be invalidated

Table 237. TRB_PRF_CACHE_STATUS_REG1 – TRB Prefetch Cache Status Register-1

Address Offset:81DC-81DFh
Default: 0h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:27	RO	0h	Core	Prefetch TRB Address (bits 8:4 of TRB Address)
26:22	RO	0h	Core	Prefetch pointer
21	RO	0h	Core	Link TRB Stop prefetch flag
20	RO	0h	Core	“Invalidate pending” flag
19:15	RO	0h	Core	EP/DCI the Way ID provided by SW is allocated to.
14:9	RO	0h	Core	Device/Slot the Way ID provided by SW is allocated to.
8	RO	0h	Core	Way ID Valid : Indicates whether the way is allocated and is “valid” for the Way ID provided by SW.

Bit	Access	Default Value	RST/PWR	Description
7:0	RW	0h	Core	TRB-$ way ID : TRB-$ way ID that we want to read out the status of.

Table 238. TRB_PRF_CACHE_STATUS_REG2 – TRB Prefetch Cache Status Register-2

Address Offset:81E0-81E3h
Default: 0h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:30	RO	0h	Core	Reserved
30	RO	0h	Core	Multiple Link Invalidation
29:28	RO	0h	Core	Last Link TRB Distant (in terms of TRB count)
27	RO	0h	Core	Last Link TRB Distant Valid
26:25	RO	0h	Core	EOR state
24:20	RO	0h	Core	CPL TRB Address
19:15	RO	0h	Core	CPL Pointer
14:10	RO	0h	Core	Xfer TRB Address
9:5	RO	0h	Core	Xfer Pointer
4:0	RO	0h	Core	Write Pointer

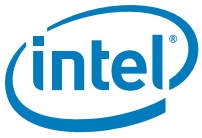
Table 239. HOST_BW_OV_SSP_REG – Super Speed Bandwidth Overload

Address Offset: 81F0h – 81F3h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:24	RO	0h	Core	Reserved
23:12	RW	02h	Core	BW calculation: Overhead per packet for SSP BW calculations. see white paper.
11:0	RW	08h	Core	BW calculation: Overhead per burst for SSP BW calculations. see white paper.

Table 240. HOST_CTRL_LINK_PORT_SPEED_REG

Address Offset:81F4 - 81F7h
Default Value:0h
Access: RW;



Size:32 bits

Bit	Access	Default Value	RST/ PWR	Description
[31:USB3_PORTS]	RO	0	Core	RESERVED
[USB3_PORTS-1:0]	RW	0	Core	PORT_SPEED_MODE 0: PORT Speed field in the PortSC will reflect the speed value based on the connected device as SSP, SS or SSIC with correct rate. 1: PORT Speed filed will reflect SS (with USB3.0 Capability) as the only speed when device is connected.

Table 241. HOST_CTRL_SUS_LINK_PORT_REG

Address Offset: 81F8-81FBh
Default Value:0h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/ PWR	Description
31:13	RW		AON	RESERVED
12	RW	0	AON	REQ_GEN1_2_PIPE_CLK_SIMULTANEOUS When set, XHCI will request for both Gen1 and Gen2 PIPE clock if either one of the clock is required by any agent.
11:9	R	000	AON	USB3_PORT_DISC_WATCHDOG This watch dog timer will be set when DAP deassert the request, once expired it will unconditionally return back the handshake to DAP. In this case controller will rely on its internal watchdog timers to get to disconnected state. When "000", watchdog timer will be disabled, else it will be multiple of RTC tick generation.
8:7	RW	2	AON	USB3_U2_EXIT_DET_TIME The time for the Gated logic to detect LFPS based on rxelecidle for U2 and U1 exit 0 = 256ns 1 = 384ns 2 = 512ns 3 = 1.024us
6:4	RW	3	AON	USB3_U3_EXIT_DET_TIME The time for the Gated logic to detect LFPS based on rxelecidle for U3 exit 0 = Immediate 1 = 128ns 2 = 256ns 3 = 512ns 4 = 1.024us 5 = 2.048us 6 = 4.096us 7 = 8.192us

Bit	Access	Default Value	RST/ PWR	Description
3	RW	1	AON	USB3_PORTEN_FORCE DISC When set treat Port Disable due to Fuse, soft strap, SSPE, PDO as a condition to force the AUX PM to go to P3 Disconnected state.
2	RW	0	AON	USB3_FORCE_PORT_DISC When set treat Port Disable due to Fuse, soft strap, SSPE, PDO (USB3_PORTEN_FORCE_DISC) and DAP request deassertion (based on USB3_HOST_ALLOC_FORCE_DISC) as a condition to force the AUX PM to go to P3 Disconnected state.
1	RW	0	AON	USB3_HOST_ALLOC_FORCE DISC Configuration to enable the force disconnect for SS port if DAP is requesting for the port ownership and Port is not in RXDET P3 state.
0	RW	0	AON	USB3_LFPS_POLLING_MODE 0: Wait for BIOS programming done before proceeding. This also implies that for D3 exit, restore from the scratch pad is complete. 1: Don't wait for the BIOS programming done and make forward progress based on the default values. BIOS should not update the LFPS default values if this bit set to 1.

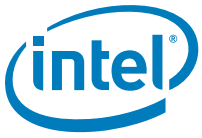
Note:
There exists a DEFINE to track the last register that need to be saved/restored as part of the register save/restore to scratchpad that needs to be updated. This is what it needs to be based on the defined registers above.
`define LAST_CHICKEN_BITS_OFS (`XECP_HOST_ADDR_OFS+16'd396) // OFFSET x81F4

Note: DFT Register uses from Address Offset 83A0h, refer to section contain all DFT Registers

Table 242. HOST CTRL EARLY DBG REG

Address Offset:81FC-81FFh
Default Value:0h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:2	RW	0	AON	Reserved
1	RW	0	AON	HW Triggered HCRST (HWTHCRST): 1: When set, HW HCRST will trigger when BootPrep is received and USB2DBCEN is set on exit from Warm/ Cold Reset cycle. Once HCRST completes, BootPrepAck will be returned. If USB2DBCEN is cleared, no HW HCRST will be triggered and BootPrepAck will be returned unconditionally. 0: When cleared, no HW HCRST will be triggered, independent of USB2DBCEN set or cleared. The SS link selects it's reset using this bit. When 1'b0, DebugResetFlag will always reset the link, else HW HCRST is used.



Bit	Access	Default Value	RST/PWR	Description
0	RW	0	AON	Wait on SW HCRST (WTONSWHCRST): 1: When set and xHCI Engine's context is NOT saved when ResetPrep (Sx, Warm/Cold) is received, upstream non-debug transactions will be blocked until a SW HCRST is seen upon an S0 re-entry. If xHCI Engine's context is saved, upstream non-debug transactions will be unblocked as soon as BootPrepAck is returned. 0: When cleared, upstream non-debug transactions will be unblocked as soon as BootPrepAck is returned. xHCI Engine context saved implies that SW wrote the USBCMD.CSS bit to 1'b1 while USBSTS.HCH bit is 1'b1

Table 243. PMREQ Control Register

Address Offset:83D0-83D3h
Default Value:600C_0033h
Access: RO; RW; RW/1S;
Size:32 bits
Chassis Restore: S0iX (Regular)
Restore Group: VNNAON

Bit	Access	Default Value	RST/PWR	Description
31	RW/1S/V	1'h0	AON	Move Controller to "unblock" state (CTRL_UNBLK): When set to '1', the controller will transition to un-block state if it is in blocked state. The read will return the status of the operation. HW will clear the bit once the requested operation is over. This is added as survivability mode.
30	RO/V	Varies	AON	PM Block Status (CTRL_BLKST) - Indicates the present state of the PM "block" flag. 0 - Controller is in un-block state and can issue upstream posted/non-posted memory accesses (Default state of PCH version of USB xHC). 1 - Controller is in block state and can't issue upstream posted/non-posted memory accesses (Default state of CPU version of USB xHC).
29	RO	1'h1	AON	No Active Slot Present - 1 - No Active Device Slot is present on xHC 0 - One or more device Slots are active on xHC. This is derived purely based on driver enabling/ disabling the device slot and doesn't factor in the actual connection status on the USB pin.
28:21	RW	9'h0	AON	Reserved (RSVD2)

Bit	Access	Default Value	RST/PWR	Description
20:18	RW	3'h3	AON	PMREQ IDLE timer (PMREQ_IDLE_TIMER): This timer is to allow PMREQ Sequencer programmable amount of time to wait for controller "idle" state such so it can accept the block request. It is only applicable during Unblock to Block transition request. Also, it doesn't guarantee that block request will always be accepted when this timer is enabled. The timer gets loaded upon PMREQ request when the controller is not idle. The timer continue to run until either it expires or controller idle state is detected during count down phase. If the controller idle state is detected during count down phase then the PMREQ sequence will move ahead with blocking flow. If the controller idle state is not detected before the timer expired then upon timer expiry, the PMREQ sequencer will go to reject state and return PMRSP(unblock) handshake. 000: Disabled 001: 128 bb_cclk 010: 256 bb_cclk 011: 512 bb_cclk 100: 1024 bb_cclk 101: 2048 bb_cclk 110: 4096 bb_cclk 111: 8192 bb_cclk
17	RW	1'b0	AON	Prevent D3/D0i3/D0i2 based PowerGating when IP wake wire to request for unblock is asserted (IP_WAKE_DIS_PG) - 1 - IP wake prevents D3/D0i3/D0i2 based PG'ing 0 - IP wake doesn't prevent PG'ing Note that, this policy mode doesn't block ForcePowerGatePOK and SW based PG'ing requests.
16	RW	1'b0	AON	Use xHC "Engine Idle" indication instead of L1TCG to accept/reject the PMREQ (EngineIdle_x_L1tcg_b) - 1 - xHC "Engine Idle" is used to accept/reject the PMREQ 0 - L1TCG is used to accept/reject the PMREQ
15	RW	1'b0	AON	Wait for VPL in L0 to service PMREQ (PMREQ_W4_VPL_L0) - 1 - Enable a mode where PMREQ SB widget will request and wait for VPL to be in L0 before proceeding PMREQ msg 0 - PMREQ SB widget will NOT wait for VPL to be in L0
14:13	RO	2'h0	AON	NDE Multiplier (NDE_MULTP): 00b: Value times 10 usec 01b: Value times 13.33 usec (not supported for ICL) 10b: Reserved 11b: Reserved Note: Added this field for future use. Only supported value is 00b in ICL.

Bit	Access	Default Value	RST/PWR	Description
12	RW	1'h0	AON	Enable feeding Periodic Scheduler Idle time into LTR (PWRSCH_IT_IN_LTR): When set, the Periodic Scheduler LTR will be included into final LTR to PMC. This is fall back mode to be able to go back to legacy LTR behavior.
11	RW	1'b0	AON	"IP wake" assertion policy for LTR Update (LTR_IPWAKE_POLICY) : 0 : Any LTR change in "block" state result into IP wake 1 : Assert IP wake only when new LTR is lower than last advertised LTR.
10:8	RW	3'h0	AON	Fabric Clock Req -> Ack assertion Timeout Timer (BBCLKACK_TIMEOUT): Timer triggers when Fabric clock "req" is asserted and starts counting until the clock "ack" assert or timeout. When the timer times out, the controller will assert the IP wake wire to indicate the clock request. This can happen when CPU system enters into deeper C-State (based on large LTR/NDE provided by controller) and shutdown Fabric PLLs. When it enters into that state, the only way to get the clock is via the assertion of IP wake wire. This timer should only be enabled in CPU version of USB controller. Value decoding (in aux_clk) : 000: Disabled (Timer is disabled) 001: 8 clocks 010: 64 clocks 011: 128 clocks 100: 256 clocks 101: 512 clocks 110: 1024 clocks 111: 2048 clocks Note that when the timer is disabled, it will also disable the assertion of IP wake wire due to clock req -> ack delay.
7	RW	1'h0	AON	Reject PM Block request when Downstream Completions pending (DSCPEND_BLKREJT) When set, the PMREQ block request will be rejected if there are one or more downstream completions pending when the block request is arrived. When clear, the PMREQ block request will be accepted even if there are one or more downstream completions pending when the block request is arrived if other criteria are met.

Bit	Access	Default Value	RST/PWR	Description
6	RW	1'h0	AON	Policy mode to provide NDE (if available) as a part of PMREQ NACK response (INCLD_NDE): When set/enabled, PMREQ Handler will trigger NDE calculation and return the NDE if available (i.e., periodic scheduler is IDLE). When clear/disabled, indicate NDE "not valid" when we NACK the PMREQ block request.
5	RW	1'h1	AON	Wait to comprehend all active LTR sources before generating PMRSP (WTONALL_LTRSRCS) : When set/enabled, the LTR reported in PMRSP will include all the active LTR sources, if present, instead of reporting out previously calculated value. When clear/disabled, LTR reported in PMRSP will be purely based on the accumulated value at the time when the PMRSP is received and HW will not wait for any on-going LTR computation to complete.
4	RW	1'h1	AON	Reject PMREQ "block" request in presence of active Debug Session (ACTVDBC_BLKREJT) (i.e., Debug is enable and Debug Host is attached) : When set to '1', the PMREQ "block" will be NACK/ rejected when Debug session is active (i.e., debug activity in-progress independent). When clear to 0, the PMREQ "block" is much more aggressive and will only be rejected if debug activity is in-progress.
3	RW	1'h0	AON	Disable D0i3/D3 PMREQ policy (DIS_D3_POLICY): By default (i.e., when this bit is cleared), certain contributors like L1TCG and run125 to PMREQ response/wake decision making criteria are excluded during D3/D0i3 state. But when this policy is set, it doesn't exclude those from PMREQ response/wake criteria. 0 : Exclude L1TCG and run125 from PMREQ response/ wake decision making criteria during D3/D0i3 state 1 : Disable the exclusion of L1TCG and run125 from PMREQ response/wake decision making criteria during D3/D0i3 state.
2:0	RW	3'h3	AON	PMRSP Timeout Timer (RSP_TIMEOUT): If programmed to non-zero, it allows a wait period for controller to establish the block on various upstream master interface from the point where it receives PMREQ request before timing out and return PMRSP response. 000: Disabled 001: 512 bb_cclk 010: 1024 bb_cclk 011: 2048 bb_cclk 100: 4096 bb_cclk 101: 8192 bb_cclk 110: 16384 bb_cclk 111: 131072 bb_cclk

Table 244. USB2_LINESTATE - Port Line State USB2

Address Offset:83F4-83F7h
Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:(NumUSB2*2)	RO	0h	Core	RESERVED
(NumUSB2*2-1) : (NumUSB2*2-2)	RO	0h	Core	Port N UTMI Linestate

Table 245. ECC Parity Error Log Register

Address Offset:83F8-83FBh
Access: RW, RW1C, RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31	RW1C	0x0	Core	Command Parity Error detected on received IOSF transaction
30	RW1C	0x0	Core	Data Parity Error detected on received IOSF transaction
29	RW1C	0x0	Core	Error Present detected on received IOSF transaction
28:26	RO	0x0	Core	Reserved
25:21	RW1C	0x0	Core	Correctable ECC Error RF Info When set indicates the specific RF the ECC Error was detected on. This is used along with the ECC Source, and Port Info to determine the specific RF on which Correctable ECC Error was seen on. USB2 Port RF: 00000: Reserved 00001: Async. TX Payload 00010: Periodic TX Payload 00011: RX Payload 00100: TTE Periodic TX Payload 00101: TTE RX Payload Others: Reserved USB3 Port RF: 00000: Reserved 00001: Async TX Payload 00010: Periodic TX Payload 00011: RX Payload Others: Reserved XHCI Engine RF: 00000: Reserved 00001: TTE Context 00010: TRM Context 00011: XHCI Completion Collect 00100: Debug Device Completion Collect 00101: DBC-EXI Trace Data

Bit	Access	Default Value	RST/ PWR	Description
20:15	RW1C	0x0	Core	Correctable ECC Error Source Port Info When set indicates the Port# if the ECC Error was detected on any of the USB2/USB3 Port RFs. This is valid only when bit[1:0] != 00
14:13	RW1C	0x0	Core	Correctable ECC Error Source Log When an Correctable ECC is detected for an RF, the corresponding bit is set to '1' 11: Detected Uncorrectable ECC Error on USB3 RFs 10 : Detected Uncorrectable ECC Error on USB2 RFs 01: Detected Uncorrectable ECC Error on XHCI Engine RFs 00 : No Error Note: On detection of first Uncorrectable ECC Error HW shall lock the Correctable log registers (Source, Port, RF) until SW clears the ECC Error log or cleared by reset.
12:8	RW1C	0x0	Core	Uncorrectable ECC Error RF Info When set indicates the specific RF the ECC Error was detected on. This is used along with the ECC Source, and Port Info to determine the specific RF on which uncorrectable ECC Error was seen on. USB2 Port RF: 00000: Reserved 00001: Async. TX Payload 00010: Periodic TX Payload 00011: RX Payload 00100: TTE Periodic TX Payload 00101: TTE RX Payload Others: Reserved USB3 Port RF: 00000: Reserved 00001: Async TX Payload 00010: Periodic TX Payload 00011: RX Payload Others: Reserved XHCI Engine RF: 00000: Reserved 00001: TTE Context 00010: TRM Context 00011: XHCI Completion Collect 00100: Debug Device Completion Collect 00101: DBC-EXI Trace Data

Bit	Access	Default Value	RST/ PWR	Description
7:2	RW1C	0x0	Core	Uncorrectable ECC Error Source Port Info When set indicates the Port# if the ECC Error was detected on any of the USB2/USB3 Port RFs. This is valid only when bit[1:0] != 00
1:0	RW1C	0x0	Core	Uncorrectable ECC Error Source Log When an uncorrectable ECC is detected for an RF, the corresponding bit is set to '1' 11: Detected Uncorrectable ECC Error on USB3 RFs 10 : Detected Uncorrectable ECC Error on USB2 RFs 01: Detected Uncorrectable ECC Error on XHCI Engine RFs 00 : No Error Note: On detection of first Uncorrectable ECC Error HW shall lock the Uncorrectable log registers (Source, Port, RF) until SW clears the ECC Error log or cleared by reset.

Table 246. ECC Poisining Control Register

Address Offset:83FC-83FFh
Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:23	RW	0x0	Core	XHCI Engine RFs ECC Poisoning Inversion bits for the 64b or 128bit (based on RF width)
22:14	RW	0x0	Core	USB3 RFs ECC Poisoning Inversion bits for the 64b or 128bit (based on RF width)
13:5	RW	0x0	Core	USB2 RFs ECC Poisoning Inversion bits for the 64b or 128bit (based on RF width)
4:3	RO		Core	Reserved
2	RW	0x0	Core	Enable ECC Poisoning for XHCI Engine related RFs that support ECC
1	RW	0x0	Core	Enable ECC Poisoning for USB3 Port related RFs that support ECC. Setting this bit enables poisoning of USB2 Port related RFs. This applies to all USB3 ports
0	RW	0x0	Core	Enable ECC Poisoning for USB2 Port related RFs that support ECC. Setting this bit enables poisoning of USB2 Port related RFs. This applies to all USB2 ports

Table 247. USB2/HSIC Port State Register

Address Offset:8400-8407h
Access: RO;

Size:64 bits

Bit	Access	Default Value	RST/PWR	Description
63:N	RO	0h	SUS	RSVD
N:0	RO	0h	SUS	USB2/HSIC Port State Per USB2/HSIC Port State Register indicating the following states 0x0 – Disconnected (PLS=5h) 0x1 – Suspended (PLS=3h) 0x2 – Disabled (PLS=7h) 0x3 – Reserved (PLS=all others) This register is Read Only and will reflect the state of the ports. Status can change at any time and any usage of this information must be done with care and under specific flows where port state change race conditions are properly handled. Note: The expectation is that this register is consumed when the controller is power gated which implies that valid values exposed should be 0x, 0x1 or 0x2. A value of 0x3 is not expected when in power gated state and implies there is an error.

Note: N = (2 * USB2/HSIC Port Count)

Table 248. USB3/SSIC Port State Register

Address Offset:8408-840Fh
Access: RO;
Size:64 bits

Bit	Access	Default Value	RST/PWR	Description
63:N	RO	0h	SUS	RSVD

Bit	Access	Default Value	RST/PWR	Description
N:0	RO	0h	SUS	USB3/SSIC Port State Per USB3/SSIC Port State Register indicating the following states 0x0 – Disconnected (PLS=5h) 0x1 – Suspended (PLS=3h) 0x2 – Disabled (PLS=4h) 0x3 – Reserved (PLS=all others) This register is Read Only and will reflect the state of the ports. Status can change at any time and any usage of this information must be done with care and under specific flows where port state change race conditions are properly handled. Note: The expectation is that this register is consumed when the controller is power gated which implies that valid values exposed will be 0x, 0x1 or 0x2. A value of 0x3 is not expected when in power gated state and implies there is an error.

Note: N = (2 * USB3/SSIC Port Count)

Table 249. FUSE1 : Miscellaneous Fuses

Address Offset:8410h-8413h
Access: RW;
Size:32 bits
This register is NOT subject to HW save and restore.

Bit	Access	Default Value	RST/PWR	Description
31	RO/V		SUS	XHCI Frame Timer Clock Frequency Select: Specifies the frequency of the Frame Timer clock used by XHCI for the frame timer block 0 : 19.2 MHz (default) 1 : 24 MHz This field is not a reflection of a FUSE since this information is exposed to the host controller as a physical wire instead of a fuse. We treat this like a FUSE hence we are shadowing the value of the wire into this register.
30:21	RO	0h	Core	Reserved
20:18	RO/V	0b	SUS	XHCI Device ID Provides a fuse over-ride for the lower 3 bits of device ID.
17	RO	0b	SUS	Reserved
16	RO/V	0b	SUS	USBr Disable (USBRDIS) : 0: USBr enabled 1: USBr disabled
15	RO/V	0b	SUS	XHCI Function Disable (XHCFD) : When asserted, it indicates the XHCI is fused to function disabled.

Bit	Access	Default Value	RST/PWR	Description
14:10	RO/V	00h	SUS	USB2 Port Count 0x0 = MAX USB2 Ports enabled 0x1 = "Max USB2 Ports -1" enabled 0x1F = All ports disabled
9:5	RO/V	00h	SUS	USB3 Port Count 0x0 = MAX USB3 Ports enabled 0x1 = "Max USB3 Ports -1" enabled 0x1F = All ports disabled
4:0	RO	0b	SUS	Reserved

Table 250. FUSE2/3: Port Map Fuses1/2 (Ports 1 to 32)

Address Offset:8414h-841Bh
Access: RW;
Size: 2 32 bit registers
This register is NOT subject to HW save and restore.

Bit	Access	Default Value	RST/PWR	Description
63: (NumUSB3*2)	RO	0h	Core	Reserved If 32 ports are defined there will not be any reserved fields. Reserved fields should result in Fuses not required to avoid having additional fuses being held by this unused field.
((NumUSB3*2)-1): ((NumUSB3*2)-2)	RO	0h	Core	Specifies XHIC port ownership for up to 32 ports. If less than 32 ports are defined, the unused bits are reserved (see next field). 00 - Flex-IO 01 - PortN is owned by XHCI operating as USB3+ 10 - PortN is owned by XHCI operating as SSIC 11 - PortN is Not owned by XHCI Ports not owned by XHCI are owned by PCIe or CSI. FLEX-IO refers to IO ownership determined by the Soft Strap. NumUSB3 = Number of SS Ports 1:0 - Port 1 3:2 - Port 2 5:4 - Port 3 … 31:30 - Port 16

Table 251. FUSE4: USB3 Port Speed Capability

Address Offset:841Ch-841Fh
Access: RW;
Size:32 bits
This register is NOT subject to HW save and restore.

Bit	Access	Default Value	RST/PWR	Description
31: (NumUSB)	RO	0h	Core	Reserved

Bit	Access	Default Value	RST/PWR	Description
NumUSB3-1:0	RO	0h	SUS	Specifies USB3.1 speed capability for up to 32 ports. 1= Port is operational as USB3.0 0= Port is operational as USB3.1 This FUSE is NA if - FUSE2/3 preclude USB 3+ mode. - FUSE2/3 dictate Flex-IO and STRAP1/2 preclude USB3+ mode.

Table 252. STRAP1: Flex IO Straps

Address Offset:8420h-8423h
Access: RW;
Size:32 bits
This register is NOT subject to HW save and restore.

Bit	Access	Default Value	RST/PWR	Description
31: (NumUSB)	RO	0h	Core	Reserved
NumUSB3-1:0	RO	0h	SUS	FlexIO mapping Each bit corresponds to the appropriately numbered USB3 port (zero based) Bit 0 = port 1, bit 1 = port 2 etc. 0: Port is owned by XHCI 1: Port is not owned by XHCI Ports not owned by XHCI are owned another controller(by PCIe/CSI/GBE/SATA)

Table 253. STRAP2: USB3 Mode Strap

Address Offset:8424h-8427h
Access: RW;
Size:32 bits
This register is NOT subject to HW save and restore.

Bit	Access	Default Value	RST/PWR	Description
31: (NumUSB)	RO	0h	Core	Reserved
NumUSB3-1:0	RO	0h	SUS	USB3+/SSIC Mode Each bit corresponds to the appropriately numbered USB3 port (zero based) Bit 0 = port 1, bit 1 = port 2 etc. 0: Port is operated in USB3/3.1 mode 1: Port is operated in SSIC mode

Table 254. STRAP3: USB3 Port Speed Capability

Address Offset:8428h-842Bh
Access: RW;
Size:32 bits
This register is NOT subject to HW save and restore.

Bit	Access	Default Value	RST/PWR	Description
31: (NumUSB)	RO	0h	Core	Reserved

Bit	Access	Default Value	RST/PWR	Description
NumUSB3-1:0	RO	0h	SUS	Specifies USB3.1 speed capability for up to 32 ports. 0= Port is operation as USB3.0 if DW0/1 indicate this port is operational under USB3/3.1 protocol. 1= Port is operation as USB3.1 if DW0/1 indicate this port is operational under USB3/3.1 protocol.

Table 255. STRAP4: Initial Port Speed Select

Address Offset:842Ch-842Fh
Access: RW;
Size:32 bits
This register is NOT subject to HW save and restore.

Bit	Access	Default Value	RST/PWR	Description
31:0	RO/V	NA	Core	Specifies forced port speed select for up to 32 ports. If less than 32 ports are defined, the unused bits are reserved (see next field). 0= Port will boot up as USB3.0 Port (5Gbps) and will carry on LBPM if USB3.1 is operational. 1= Port will boot up as USB3.1 Port (10Gbps) and skip LBPM.

Table 256. DFT1: DFT Register1

Address Offset:8430h-8433h
Access: RW;
Size:32 bits
This register is NOT subject to HW save and restore.

Bit	Access	Default Value	RST/PWR	Description
31:16	R0	FFFFh	Core	SS/SSIC DFT CRC (SSDFTCRC): These register bits contain the value of SS DFT CRC
15:12	RW	0h	Core	Rsvd1 (Rsvd1):
11	RW	0h	Core	This bit is set to bypass link training state in HBP mode. This bit is applicable only in HBP mode, and need to be set before HBP Enable bit is set.
10	RW	0h	Core	Super Speed DFT LFPS Mode Select (SSDFTLMSEL): This bit selects the Super Speed DFT LFPS mode, and will only take effect when Super Speed HBP mode is enabled. 0b: HBP logic will internally loopback TX LFPS as RX LFPS and AFE RX LFPS path to the controller is disconnected. (DFTLFPSSEL should be set) 1b: RX LFPS path works normally driven from GPIO pin

Bit	Access	Default Value	RST/PWR	Description
9:6	RW	0h	Core	SS/SSIC DFT CRC Select (SSDFTCRCSEL): These bits select which Super Speed DFT CRC value is reflected in SSDFTCRC bits. In addition, these bits also select which SuperSpeed DFT CRC MSB value is sent to GPIO monitor pin, i.e. sata3gp_gp37 to aid silicon debug. Live version of selected CRC's MSB will be- sent to GPIO monitor pin, i.e. sata3gp_gp37. 0h (default): No SuperSpeed DFT CRC is selected. 1h: Data Payload CRC 2h: Link Management Packet CRC 3h: Transaction Packet CRC 4h: Isochronous Timestamp Packet CRC 5h: Data Packet Header CRC 6h: Link Command Packet CRC 7h: RRAP Packet CRC 8h: Tx/Rx Cfg CRC Others: Reserved Note : CRC types 7 and 8 are only applicable if Port is SSIC Port
5	RO	0h	Core	Port Loopback MISR Clear (MISR_CLEAR) [Applicable only for DFx Port Loopback mode] Clear function equivalent to hbp_crc_rst signal. This will clear both Host and Device CRC and DP_COUNT registers. This register need to be explicitly set and cleared with 2us delay. 0 - Default 1 - Clear DP_COUNT, SS MISRs and HS/FS MISRs
4:0	RW	0h	Core	SS/SSIC DFT CRC Port Select (SSICDFTCPS): One CRC per packet type is shared for all the Super Speed ports. These bits select the Super Speed port for which CRC data will be updated. 000b: (default) No SuperSpeed Port is selected 001b: SS/SSIC Port 0 010b: SS/SSIC Port 1 011b: SS/SSIC Port 2 100b: SS/SSIC Port 3 101b: SS/SSIC PORT4 110b :SS/SSIC Port 5 others : Rsvd

Table 257. DFT2: DFT Register2

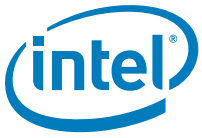
Address Offset:8434h-8437h
Access: RW;
Size:32 bits
This register is NOT subject to HW save and restore.

Bit	Access	Default Value	RST/PWR	Description
31:16	RO	FFFFh	Core	HS/HSIC TX CRC (TXCRC): These register bits contain the value of TX CRC. This TX CRC is placed right after the 480MHz XCLKQ.

Bit	Access	Default Value	RST/PWR	Description
15:11	RW	0h	Core	HSIC/UTMI+ DFT Port Select (UTMIDFTPS): One CRC is shared for all the UTMI+ ports. These bits select the UTMI+ port for which CRC data will be updated and loopback status reflected in UTMILPBKSTS. 0h: (default) No UTMI+ Port is selected 1h: UTMI+ Port 0 2h: UTMI+ Port 1 3h: UTMI+ Port 2 4h: UTMI+ Port 3 5h: UTMI+ Port 4 6h: UTMI+ Port 5 7h: UTMI+ Port 6 8h: UTMI+ Port 7 9h: UTMI+ Port 8 Ah: UTMI+ Port 9 Bh: UTMI+ Port 10 Ch: UTMI+ Port 11 Dh: UTMI+ Port 12 Eh: UTMI+ Port 13 Others: Reserved
10:7	RW	0h	Core	Reserved
6:5	RW	0h	Core	Operational Mode (UTMIOPMODE_1_0): Operational Mode in test mode. These signals select between various operational modes: 00b: Normal Operation 01b: Non-Driving 10b: Disable Bit Stuffing and NRZI encoding 11b: Reserved
4	RW	0h	Core	Termination Select (UTMITERMSEL): Termination Select in test mode. This signal selects between the FS and HS terminations: 0b: HS termination enabled 1b: FS termination enabled
3:2	RW	0h	Core	Transceiver Select (UTMIXCVRSELECT_1_0): Transceiver Select in test mode. This signal selects between the LS, FS and HS transceivers: 00b: HS transceiver enabled 01b: FS transceiver enabled 10b: LS transceiver enabled 11b: Reserved
1:0	RW	0h	Core	Reserved

Table 258. DFT3: DFT Register3

Address Offset:8438h-843Bh
Access: RW;
Size:32 bits



This register is NOT subject to HW save and restore.

Bit	Access	Default Value	RST/PWR	Description
31:24	RO	0	Core	Error Count Error count tracks the number of grey count cycle that had errors. This count increments once for every cycle with error, and waits for next sequence to start with 8'hFF. The counter does not roll over on reaching the max count. Can be reset by disabling the UTMI Loopback Enable.
23:16	RO	0h	Core	Number of consecutive LFSR cycle Good pattern increment on every cycle 8'hFF The counter does not roll over on reaching the max count. This counter stops incrementing after first error. Can be reset by disabling the UTMI Loopback Enable.
15:0	RW	0h	Core	Reserved

Table 259. DFT4: DFT Register4

Address Offset:843Ch-843Fh
Access: RW;
Size:32 bits
Reads to this register will return 0 unless HBP mode is enabled allowing for the HBP clock to run.
This register is NOT subject to HW save and restore.

Bit	Access	Default Value	RST/PWR	Description
31:NumUSB2	RO	0h	Core	Reserved
(NumUSB2-1):0	RW	0h	Core	Loopback Lane Select (UTMILPBKSEL): Port is selected if the corresponding bit (zero based) is selected Bit 0 = Port 1 Bit 1 = Port 2 Etc.

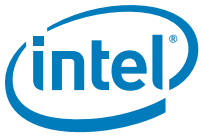
Table 260. DFT5: DFT Register5

Address Offset:8440h-8443h
Access: RW;
Size:32 bits
Reads to this register will return 0 unless HBP mode is enabled allowing for the HBP clock to run.
This register is NOT subject to HW save and restore.

Bit	Access	Default Value	RST/PWR	Description
31:28	RW/L	0h	Core	High Speed Bypass Enable 0000 - Disable all HBP 0001 - Enable SS HBP 0010 - Enable HS HBP 0011 - Enable HSIC HBP 0100 - Enable SSIC HBP 0101 - Enable SSP HBP Others - Reserved Access is controlled by the "Access Control" lock bit in config space.

Bit	Access	Default Value	RST/PWR	Description
27	RW	0h	Core	DFTIDPINSEL Select Between Device and Host Controller in HBP mode 0h : Host Controller is selected 1h : Device Controller is selected
26	RO	0b	Core	Reserved
25	RW/L	0h	Core	Loopback Enable (UTMILPBKEN): Enable loopback test mode. If asserted, loopback test mode is enabled UTMI loopback is supported for XHCI & XDCI via DFTIDPINSEL.
24:11	RW	0h	Core	Rsvd
10	RW	0h	Core	HBP_DISCONNECT_CONTROL XHCI: In HBP mode this bit enables host_disconnect control. This eliminates the need for tester to control the PHY disconnect signaling on D+/- lines. 0h: XHCI HBP uses host_disconnect signal from USB2 PHY 1h: XHCI HBP uses ftc_data[10] signal to control the host_disconnect signal XDCI: In HBP mode this bit enables bvalid control from USB2 PHY. This eliminates the need for tester to maintain the VBUS voltage input to PHY. 0h: XDCI HBP uses bvalid signal from USB2 PHY 1h: XDCI HBP uses ftc_data[10] signal to control the bvalid signal
9	RW	0h	Core	DIS_GPIO LINESTATE_CONTROL_XHCI Disable GPIO UTMI Linestate Control for XHCI By default UTMI Linestate are controlled via GPIO pins. Set this register to disable the GPIO control, XHCI will internal HS Chirp bypass. 0h : Linestate controlled via GPIO 1h : HS Chirp bypassed
8	RW	0h	Core	DIS_GPIO LINESTATE_CONTROL_XDCI Disable GPIO UTMI Linestate Control for XDCI By default UTMI Linestate are controlled via GPIO pins. Set this register to disable the GPIO control, XDCI will using the Linestate from USB2 PHY, HVM tester need to synthesize the Linestate by driving the D+/-. 0h : Linestate controlled via GPIO 1h : Linestate controlled via PHY input
7:0	RO	0h	Core	DFT5[7:0]: HBP TX DP COUNT This field captures the TX DP packet count captured in TX DP MISR. This field is applicable to current HBP test for either USB3.x or SSIC interface. The counter freezes when reaches the limit and does not roll over. The clear can be performed by HBP crc reset signal.

Table 261. DFT6: DFT Register6



Note: The start Address Offset for DFT6 register and beyond is different, not contiguous from previous DFT5 register.

Address Offset:83A0h-83A3h
Access: RW;
Size:32 bits
This register is NOT subject to HW save and restore.

Bit	Access	Default Value	RST/PWR	Description
31:28	RW	0h	Core	DFx Port Loopback Interface Select 0000 - Reserved 0001 - Self Loopback* (same port at PIPE interface) 0010 - SSP Loopback 0011 - SS Loopback 0100 - UTMI Loopback Others - Reserved
27	RW	0h	Core	DFx Port Loopback Device Select 0 - Use XDCI for Device 1 - Use DBC for Device
26:22	RW	0h	Core	DFx Port Loopback Host Port Select XHCI Port number to select Host mode connection. 0 - Port 0 1 - Port 1 N - max (NumUSB2, NumUSB3) - 1 Others - Reserved
21:17	RW	0h	Core	DFx Port Loopback Port Select XHCI Port number to select Device mode connection, applicable in both XHCI and DBC mode. This register should match the DAP register for Device port select. 0 - Port 0 1 - Port 1 N - max (NumUSB2, NumUSB3) - 1 Others - Reserved
16	RW/L	0h	Core	DFx USB3 Persistence Mode Enable 0 - Disabled 1 - Enabled This enable bit is common for all ports. Disabling this mode requires this bit to be cleared, and port is directed to Disable state. Access is controlled by the "Access Control" lock bit in config space.
15:14	RO	0h	Core	Reserved
13	RW	0h	Core	DFx Port Loopback CRC Override Override mode is to enable MISR calculation on every clock in DFx Port Loopback mode. Test can read any of DFT CRC MISRs after sequence completes. TX_DP_COUNT is invalid when override is enabled. Typical usage is to observe MSB of CRC (16th) in Visa. 0 - Normal 1 - CRC Override enable on every clock

Bit	Access	Default Value	RST/PWR	Description
12	RW/L	0h	Core	DFx Port Loopback Enable This field enables the start of DFx Port Loopback mode. Test need to ensure that this is set last in init sequence, and other dft register are valid. Test shall clear this register at the end of the sequence, this will ensure the HBP CRC register are not updated further. Access is controlled by the "Access Control" lock bit in config space.
11:4	RO	0h	Core	Device HBP TX DP COUNT [Applicable only for DFx Port Loopback mode, for both XDCI & DBC] This field captures the TX DP packet count captured in TX DP MISR. This field is applicable to current HBP test for USB3.0 interface. The counter freezes when reaches the limit and does not roll over. The clear can be performed by HBP crc reset signal.
3:0	RW	0h	Core	Device SS DFT CRC Select (XDCI SSDFTCRCSEL): [Applicable only for DFx Port Loopback mode, for both XDCI & DBC] These bits select which Super Speed DFT CRC value is reflected in SSDFTCRC bits. In addition, these bits also select which SuperSpeed DFT CRC MSB value is sent to GPIO monitor pin, i.e. sata3gp_gp37 to aid silicon debug. Live version of selected CRC's MSB will be- sent to GPIO monitor pin, i.e. sata3gp_gp37. 0h (default): No SuperSpeed DFT CRC is selected. 1h: Data Payload CRC 2h: Link Management Packet CRC 3h: Transaction Packet CRC 4h: Reserved (ITP NA for Device) 5h: Data Packet Header CRC 6h: Link Command Packet CRC Others: Reserved

Table 262. DFT7: DFT Register7

Address Offset:83A4h-83A7h
Access: RW;
Size:32 bits
This register is NOT subject to HW save and restore.

Bit	Access	Default Value	RST/PWR	Description
31:16	RO	FFFFh	Core	Device SS DFT CRC (XDCI_SSDFTCRC): [Applicable only for DFx Port Loopback mode, for both XDCI & DBC] These register bits contain the value of SS DFT CRC. This CRC is selected by DFT6.XDCI_SSDFTCRCSEL.

Bit	Access	Default Value	RST/PWR	Description
15:0	RO	FFFFh	Core	Device USB2 TX CRC (XDCI TXCRC): [Applicable only for DFx Port Loopback mode, for both XDCI & DBC] These register bits contain the value of USB2 TX CRC. This TX CRC is placed right after the 480MHz XCLKQ.

Table 263. STS_CTRL_REG - STATUS CONTROL REGISTER

Address Offset:8444h-8447h
Default Value:0h
Access: RW;
Size:32 bits
This register is not subject to HW save and restore.

Bit	Access	Default Value	RST/PWR	Description
31:3	RW	0h	Core	Reserved
2:0	RW	0h	Core	DAP STRAP SELECT This field is used to select the DAP STRAP register to read out at STRAP5_12 REG 0h - STRAP5 1h - STRAP6 2h - STRAP7 3h - STRAP8 4h - STRAP9 5h - STRAP10 6h - STRAP11 7h - STRAP12

Table 264. XECP_CMDM_STS0 - XECP_CMDM_STS0

Address Offset:8448h-844Bh
Default Value:00000CC1h
Access: RO;
Size:32 bits
This register is not subject to HW save and restore.

Bit	Access	Default Value	RST/PWR	Description
31	RO	0h	Core	Indicates that IDMA module currently owns the context access :
30	RO	0h	Core	Indicates that ODMA module currently owns currently the context access
29	RO	0h	Core	Indicates that TRM modules owns the context access currently
28	RO	0h	Core	Indicates that Command Manager has requested a context lock
27	RO	0h	Core	Indicates that Command Ring stop command is in progress
26	RO	0h	Core	Indicates that clearing an EP out of schedule is in progress
25	RO	0h	Core	Indicates that current address device command is done by ODMA
24	RO	0h	Core	Indicates that ODMA has an address device command in progress
23	RO	0h	Core	Indicates that updating of EP state is in progress
22	RO	0h	Core	Indicates that doorbell manager is issuing and EP update due to a doorbell ring on an EP that is in stop state
21	RO	0h	Core	Indicates that transfer ring manager is issuing and EP update due to an EP error condition detected

Bit	Access	Default Value	RST/PWR	Description
20	RO	0h	Core	Indicates that transfer ring manager is issuing and EP state update due to stall received
19	RO	0h	Core	Reserved
18	RO	0h	Core	Indicates that a STOP on the Command Ring is in progress
17	RO	0h	Core	Indicates that command ring has a doorbell pending
16	RO	0h	Core	Indicates that the commend ring is running
15:8	RO	0Ch	Core	Command next capability offset
7:0	RO	C1h	Core	Vendor defined capability ID

Table 265. XECP_CMDM_STS1 - XECP_CMDM_STS1

Address Offset:844Ch-844Fh
Default Value:03FC0000h
Access: RO;
Size:32 bits
This register is not subject to HW save and restore.

Bit	Access	Default Value	RST/PWR	Description
31:0	RO	03FC0000h	Core	Internal xhci engine status bits: {6'b0,evtm_pcs[7:0], trb_count[96:91], trb_count[83:78], trb_count[70:65]}

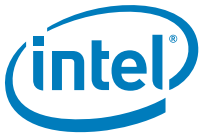
Table 266. XECP_CMDM_STS2 - XECP_CMDM_STS2

Address Offset:8450h-8453h
Default Value:00000000h
Access: RO;
Size:32 bits
This register is not subject to HW save and restore.

Bit	Access	Default Value	RST/PWR	Description
31:0	RO	0h	Core	Internal command manager status bits: { 3'b0, reset_endpt_pst, // 5 bits 29-bits total force_header_pst, // 3 bits reset_device_pst, // 5 bits stop_endpt_pst, // 4 bits update_endpt_pst, // 4 bits set_tr_dequeue_ptr_pst, // 4 bits get_port_bw_pst }; // 4 bits

Table 267. XECP_CMDM_STS3 - XECP_CMDM_STS3

Address Offset:8454h-8457h
Default Value:00000000h
Access: RO;
Size:32 bits



This register is not subject to HW save and restore.

Bit	Access	Default Value	RST/PWR	Description
31:0	RO	0h	Core	Internal command manager status bits: 8'b0, 1'b0, ep_state, // 3 bits slot_en_ary, 1'b0, slot_state, //2 2'b0, ep_id, // 5 bits internal_cmd_slot_id_extended }; // 8 bits

Table 268. XECP_CMDM_STS4 - XECP_CMDM_STS4

Address Offset:8458h-845Bh
Default Value:00000000h
Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:0	RO	0h	Core	Internal command manager status bits: cmd_ring_pointer[31:4], 3'b0, cmd_ccs

Table 269. XECP_CMDM_STS5 - XECP_CMDM_STS5

Address Offset:845Ch-845Fh
Default Value:00000000h
Access: RO;
Size:32 bits
This register is not subject to HW save and restore.

Bit	Access	Default Value	RST/PWR	Description
31:0	RO	0h	Core	Internal command manager status bits: cmd_ring_pointer[63:32]

Table 270. UPORTS_PON_RST_REG - AUX Power PHY Reset

Address Offset:8460-8463h
Default Value:00000000h
Access: WO;
Size:32 bits
This register is not subject to HW save and restore.

Bit	Access	Default Value	RST/PWR	Description
31:6	RO	0h	Core	RESERVED
3:0	WO	0h	Core	Allow a USB PHY reset being issued by software. Writing to this register with bit set to 1 will reset the USB PHY that is connected to the port. Bit3:0 indicates the port number of the USB PHY

Table 271. HOST_IF_LAT_TOL_CTRL_REG0 - Latency Tolerance Control 0

Address Offset:8464-8467h
Default Value:0h
Access: RW;
Size:32 bits
The Latency Tolerance Control Register is used by SW to control which BELT is returned when this register is read. SW shall write to this register to program a Slot-ID, Port-ID and BELT Select to determine which BELT is selected. When this register is read the selected BELT is returned.

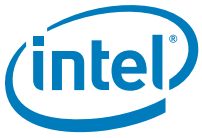
This register is not subject to HW save and restore.

Bit	Access	Default Value	RST/PWR	Description
31:30	WO	0h	Core	BELT Select (): This field determines what value will be selected to read back from SW when reading this register 0: Returns the SW programmed Latency Tolerance Value 1: Returns the Lowest BELT in the Host 2: Returns the BELT for the requested Slot-ID (Slot Select) 3: Returns the BELT for the requested Port-ID (Port Select)
29:20	RO	0h	Core	Rsvd1 (Rsvd1):
19:16	WO	0h	Core	Port Select (): Used to select the BELT for a given Port # when the BELT Select is programmed to select the Port-ID (this field is 0 based)
15:12	RO	0h	Core	Rsvd1 (Rsvd1):
11:5	RO	0h	Core	BELT Value (BELTV) [11:5]: Value of selected BELT is return in this field
4:0	RW	0h	Core	Reads will return: BELT Value (BELTV) [4:0]: Value of selected BELT is return in this field Writes will control : Slot Select (): Used to select the BELT for a given Slot # when the BELT Select is programmed to select the Slot-ID (this field is zero based)

Table 272. PMCTRL2-Power Management Control

Address Offset:8468-846Bh
Default Value:5Eh
Enabling per port Power Gating requires following sequence,
- Update any register for RF configuration except PORT_RF_PG_EN (PMCTRL[7:1])
- Set PORT_RF_PG_EN
- Set USB_SRAM_PG_EN. (This can be set without setting PORT_RF_PG_EN to enable D0i1 without per port RF power gating)

Bit	Access	Default Value	RST/PWR	Description
31:30	RW	0	SUS	Reserved
29:26	RW	4	SUS	ISOL_TO_PWRGATE_LTNCY Latency in aux clock count from Isolation to Power Gate assertion for RF Per Port PG
25:22	RW	2	SUS	ISOL_TO_DEISOL_LTNCY Latency in aux clock count from Isolation to Deisolation if flow breaks in the middle for RF Per Port PG
21:18	RW	2	SUS	PWRGATE_TO_PWRUNGATE_LTNCY Minimum residency time in power gating state in aux clock count for RF Per Port PG
17:14	RW	2	SUS	PWRUNGATE_TO_PWRGATE_LTNCY Minimum residency time in power ungating gating state in aux clock count for RF Per Port PG



Bit	Access	Default Value	RST/PWR	Description
13:10	RW	4	SUS	PWRUNGATE_TO_DEISOL_LTNCY Latency in aux clock count from Power Ungating to removing isolation for RF Per Port PG
9:6	RW	1	SUS	DEISOL_TO_PWRSTABLE_LTNCY Latency in aux clock count from removing isolation to allowing RF access for RF Per Port PG
5	RW	0	SUS	PORT_RF_PG_EN When set, it will enable per port Power gating for RF. This will not impact D0I1 flow which will be controlled by USB SRAM PG config bit. If enabling Per port RF Power Gating, this bit must be set before setting USB_SRAM_PG_EN bit.
4	RW	1	SUS	PORT_RF_PG_USB2_DIS_DISC_EN When set, it will enable the Per Port RF power gating for USB2 ports which are Disconnected / Disabled or Power Off This bit should be set/clear before setting USB_SRAM_PG_EN bit.
3	RW	1	SUS	PORT_RF_PG_USB2_U3_EN When set, it will enable the Per Port RF power gating for USB2 ports which are in U3 This bit should be set/clear before setting USB_SRAM_PG_EN bit.
2	RW	1	SUS	PORT_RF_PG_USB3_DIS_DISC_EN When set, it will enable the Per Port RF power gating for USB3 ports which are Disconnected / Disabled or Power Off. This bit should be set/clear before setting USB_SRAM_PG_EN bit.
1	RW	1	SUS	PORT_RF_PG_USB3_U3_EN When set, it will enable the Per Port RF power gating for USB3 ports which are in U3. This bit should be set/clear before setting USB_SRAM_PG_EN bit.
0	RW	0	SUS	PORT_RF_USB3_DECODE_MODE 1: It will use the PLS as the indication for the port status. 0: Port pipe power down signal will be used for state decoding. This bit should be set/clear before setting USB_SRAM_PG_EN bit.

4.4.4.3 Legacy Support Extended Capability

Base Offset of this capability from MBAR is 846Ch

Table 273. USBLEGSUP - USB Legacy Support Capability

Address Offset:846C-846Fh
Default Value:00000001h
Access: RO; RW;
Size:32 bits
Chassis Restore: S0iX (Regular)
Restore Group: VNNAON

This register is modified and maintained by BIOS

Bit	Access	Default Value	RST/PWR	Description
31:25	RO	0h	Core	Rsvd2 (Rsvd2):
24	RW	0h	SUS	HC OS Owned Semaphore (HCOSOS):
23:17	RO	0h	Core	Rsvd1 (Rsvd1):
16	RW	0h	SUS	HC BIOS Owned Semaphore (HCBIOSOS):
15:8	RW/L	22h / 25h See Note	SUS	Next Capability Pointer (NextCP):
7:0	RO	1h	SUS	Capability ID (CID):

Note:

Note: If PDOCapability = 0, Next Capability Pointer = 25h

Table 274. USBLEGCTLSTS - USB Legacy Support Control Status

Address Offset:8470-8473h
Default Value:00000000h
Access: RO; RW; RW1C;
Size:32 bits
Chassis Restore: S0iX (Regular)
Restore Group: VNNAON

Bit	Access	Default Value	RST/PWR	Description
31	RW1C	0h	SUS	SMI on BAR (SMIBAR):
30	RW1C	0h	SUS	SMI on PCI Command (SMIPCIC):
29	RW1C	0h	SUS	SMI on OS Ownership Change (SMIOSOC):
28:21	RO	0h	Core	Rsvd4 (Rsvd4):
20	RO	0h	SUS	SMI on Host System Error (SMIHSE):
19:17	RO	0h	Core	Rsvd3 (Rsvd3):
16	RO	0h	SUS	SMI on Event Interrupt (SMIEI):
15	RW	0h	SUS	SMI on BAR Enable (SMIBARE):
14	RW	0h	SUS	SMI on PCI Command Enable (SMIPCICE):
13	RW	0h	SUS	SMI on OS Ownership Enable (SMIOSOE):
12:5	RO	0h	Core	Rsvd2 (Rsvd2):
4	RW	0h	SUS	SMI on Host System Error Enable (SMIHSEE):
3:1	RO	0h	Core	Rsvd1 (Rsvd1):
0	RW	0h	SUS	USB SMI Enable (USBSMIE):

4.4.4.4 Port Disable Override Capability

If this Extended Capability exists, it must be located in the Always ON power well to retain the “Write Once” attribute – which is necessary to maintain the integrity of the Port Disable setting.

Base Offset = 84F4h

Table 275. Capability Register

Address Offset: 00 - 03

Bit	Access	Default Value	RST/PWR	Description
31:16	RO	0h	NA	Reserved
15:8	RW/L	3h	Core	Next Capability Pointer

Bit	Access	Default Value	RST/PWR	Description
7:0	RW/L	C6h	Core	Capability ID

Table 276. USB2 – Port Disable Override

Address Offset: 04 – 07h

Bit	Access	Default Value	RST/PWR	Description
31: NumUSB2	RO	0h	Core	Rsvd1 (Rsvd1) :
(NumUSB2-1):0	RWO	0h	Core	USB2 Port Disable Override (USB2PDO) : A '1' in a bit position prevents the corresponding USB2 port from reporting a Device Connection to the XHC. This applies across all USB2 protocol ports

Table 277. USB3 Port Disable Override

Address Offset: 08 – 0Bh

Bit	Access	Default Value	RST/PWR	Description
31: NumUSB3	RO	0h	Core	Rsvd1 (Rsvd1) :
(NumUSB3 -1):0	RWO	0h	SUS	USB3 Port Disable Override (USB3PDO) : A '1' in a bit position prevents the corresponding USB3 port from reporting a Device Connection to the XHC. This applies across all USB3 protocol ports

4.4.4.5 HW State Access Capability

This memory range is reserved for use by the Host Controller HW to assist in save and restore of HW state. This memory range is not intended to be read or written by SW.

Base Offset = 8500h
This capability starts at offset 8500h from MBAR.

Table 278. Capability ID register

Address Offset: 00 – 03h

Bit	Access	Default Value	RST/PWR	Description
31:24	RO	00h	Core	Reserved
23:16	RO	Variable	Core	Save Length Indicates the number of DWords in this capability starting at offset 04h, that need to be saved and restored
15:8	RO	40h	Core	Next Capability Pointer
7:0	RO	C7h	Core	Supported Protocol ID

Note: The save length is a f() of various RTL parameters. Any HW consumer of this field shall also consume the same value derived be these parameters.

Table 279. SOCHWSTSAVE1 - SOC HW State Save 1 Register

Address Offset: 04-07h
Access: RW;
Size:32 bits
Chassis Restore: S0iX (Regular)
Restore Group: VNNAON

Bit	Access	Default Value	RST/PWR	Description
31	RW	0h	SUS	Update the cmd_ssv flag which indicates that context is saved or not.
30:8	RW	0h	SUS	Reserved
7:0	RW	0h	SUS	save_retore_enable_reg This field reflects the current value of save_restore_enable flag.

Table 280. HWST1 - HW State 1

Address Offset 14- 17h

Bit	Access	Default Value	RST/PWR	Description
31:00	RW	X	Core	Implementation defined HW state: SW must not access this register.

Table 281. HWST2 - HW State 2

Address Offset 18- 1Bh

Bit	Access	Default Value	RST/PWR	Description
31:00	RW	X	Core	Implementation defined HW state: SW must not access this register.

Table 282. HWST3 - HW State 3

Address Offset 1C- 1Fh

Bit	Access	Default Value	RST/PWR	Description
31:00	RW	X	Core	Implementation defined HW state: SW must not access this register.

Table 283. HWST4 - HW State 4

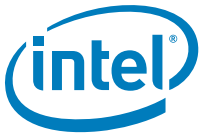
Address Offset 20- 23h

Bit	Access	Default Value	RST/PWR	Description
31:00	RW	X	Core	Implementation defined HW state: SW must not access this register.

4.4.4.6 Config Space Register Mirror

Base Offset: 8600h

Table 284. Capability Register



Address Offset: 00 – 03 (from the base offset)

Bit	Access	Default Value	RST/PWR	Description
31:16	RO	0h	NA	Reserved
15:8	RW/L	40h*	Core	Next Capability Pointer See Note below on configurability
7:0	RW/L	C2h	Core	Capability ID

Note: Next Capability Pointer=80h if XHCIDbC = False, but NumSSICports>0.

Note: Next Capability Pointer=00h if XHCIDbC = False and NumSSICports=0.

Table 285. XHCC1 - XHC System Bus Configuration 1

Address Offset: 40-43h

Table 286. XHCC2 - XHC System Bus Configuration 2

Address Offset: 44-47h

Table 287. XHCLKGTEN - Clock Gating

Address Offset: 50-53h

Table 288. AUDSYNC - Audio Time Synchronization

Address Offset: 58-5Bh

Table 289. FSLSPS – FS/LS Port Staggering Control

Address Offset: 98-9Ch

Table 290. HSCFG1 - High Speed Configuration 1
Address Offset: A0-A3h

Table 291. HSCFG2 - High Speed Configuration 2
Address Offset: A4-A7h

Table 292. SSCFG1 - SuperSpeed Configuration 1
Address Offset: A8-ABh

Table 293. U2OCM<N> - XHCI USB2 Overcurrent Pin N Mapping
Address Offset: B0-B3h, ... (B0h+(NumOC-1)*4) to (B3h+(NumOC–1)*4) <upto C7h>

Table 294. U3OCM<N> - XHCI USB3 Overcurrent Pin N Mapping
Address Offset: D0-D3h, ... (D0h+(NumOC-1)*4) to (D3h+(NumOC–1)*4) <upto E7h>

Table 295. MANID - Manufacturing Process ID
Address Offset: F8-FBh

4.4.4.7 XHCI Debug Capability

Base Offset = 8700h

Table 296. Debug Capability ID Register (DCID)

Memory Mapped IO Space
Address Offset:00-03h
Access: RO; RW/S;
Size:32 bits
This register is modified and maintained by BIOS

Bit	Access	Default Value	RST/PWR	Description
31:21	RW	0h	NA	Reserved
20:16	RW/L	05h	Core	Debug Capability Event Ring Segment Table Max (DCERST Max)
15:8	RW/L	10h	Core	Next Capability Pointer
7:0	RW/L	0Ah	Core	Capability ID

Table 297. Debug Capability Doorbell Register (DCDB)

Memory Mapped IO Space
Address Offset:04h-07h
See xHCI spec for details

Table 298. Debug Capability Event Ring Segment Table Size Register (DCERSTSZ)

Memory Mapped IO Space
Address Offset:08h-0Bh
See xHCI spec for details

Table 299. Debug Capability Event Ring Segment Table Base Address Register (DCERSTBA)

Memory Mapped IO Space
Address Offset:10-17h
See xHCI spec for details

Table 300. Debug Capability Event Ring Dequeue Pointer Register (DCERDP)

Memory Mapped IO Space
Address Offset:18-1Fh
See xHCI spec for details

Table 301. Debug Capability Control Register (DCCTRL)

Memory Mapped IO Space
Address Offset:20-23h
Default Value:0005_000Ah
Access: RO; RW1C; RW1S; RW
Size:32 bits

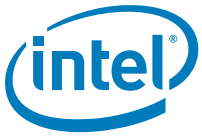
Bit	Access	Default Value	RST/PWR	Description
31	RW	0h	Core	Debug Capability Enable (DCE)
30:24	RO	00h	Core	Device Address
23:16	RO	00h	Core	Debug Max Burst Size: LPT-LP USB Debug Device does not support bursting.
15:5	RO	000h	NA	Reserved
4	RW1C	0	Core	DbC Run Change (DRC)
3	RW1S	0	Core	Halt IN TR (HIT)
2	RW1S	0	Core	Halt OUT TR (HOT)
1	RW	0	Core	Link Status Event Enable (LSE)
0	RO	0	Core	DbC Run (DCR)

Table 302. Debug Capability Status Register (DCST)

Memory Mapped IO Space
Address Offset:24-27h
See xHCI spec for details

Table 303. Debug Capability Port Status and Control Register (DCPORTSC)

Memory Mapped IO Space



Address Offset:28-2Bh

Note: Note:The DCPORTSC definition has been updated to reflect USB 2.0 only operation. When operating in USB 3.0 mode, the xHCI specification defined behavior shall be followed

Bit	Access	Default Value	RST/PWR	Description
31:24	RO	0		Reserved
23	RW1C	0		Reserved for USB2 Debug Capability. Note: This bit shall never be set when operating in USB2 Debug Capability mode.
22	RW1C	0	SUS	Port Link Status Change (PLC): This flag is set to '1' due to the following PLS transitions: Transition Condition U0 -> U3 Suspend signaling detected from Debug Host U3 -> U0 Resume complete Software shall clear this bit by writing a '1' to it. This field is '0' if (DCE and USBDCIEN) is '0'.
21	RW1C	0	SUS	Port Reset Change (PRC): Default = '0'. This bit is set when reset processing on this port is complete (i.e. a '1' to '0' transition of PR). '0' = No change. '1' = Reset complete. Software shall clear this bit by writing a '1' to it. This field is '0' if (DCE and USBDCIEN) is '0'.
20:18	RO	0		Reserved
17	RW1C	0	SUS	Connect Status Change (CSC): '1' = Change in Current Connect Status. '0' = No change. Indicates a change has occurred in the port's Current Connect Status. The xHC sets this bit to '1' for all changes to the Debug Device connect status, even if system software has not cleared an existing DbC Connect Status Change. For example, the insertion status changes twice before system software has cleared the changed condition, hardware will be "setting" an already-set bit (i.e., the bit will remain '1'). Software shall clear this bit by writing a '1' to it. This field is '0' if (DCE and USBDCIEN) is '0'.
16:14	RO	0		Reserved
13:10	RO	0	SUS	Port Speed (Port Speed): This field identifies the speed of the port. This field is only relevant when a Debug Host is attached (PED = '1') in all other cases this field shall indicate Undefined Speed. Value Meaning 0 Undefined Speed 1-15 Protocol Speed ID (PSI) Note: The USB2 Debug Capability does not support LS operation.
9	RO	0		Reserved

Bit	Access	Default Value	RST/PWR	Description
8:5	RO	4'h4	SUS	Port Link State (PLS): This field reflects its current link state. This field is only relevant when a Debug Host is attached. Link == USB2 Port State since there is no notion of link states on USB2. Value Meaning 0 Link is in the U0 State 1 Reserved 2 Link is in the U2 State (Device L1 suspended) 3 Link is in the U3 State (Device Suspended) 4 Link is in the Powered Off State 5 Reserved 6 Reserved 7 Link is in the Disabled State 8:11 Reserved 12 Link is in Port Reset State 13:14 Reserved 15: Resume Note: Transitions between different states are not reflected until the transition is complete
4	RO	0	SUS	Port Reset (PR): '1' = Port is in Reset. '0' = Port is not in Reset. This bit is set to '1' when the bus reset sequence as defined in the USB 2.0 Specification is detected on the port assigned to the Debug capability. It is cleared when the bus reset sequence is completed by the Debug Host, and the DbC shall transition to the USB Default state. A '0' to '1' transition of this bit shall clear DCPORTSC PED ('0'). This field is '0' if (DCE and USBDCIEN) or CCS are '0'.
3:2	RO	0		Reserved

Bit	Access	Default Value	RST/PWR	Description
1	RW	0	SUS	Port Enabled/Disabled (PED): '1' = Enabled. '0' = Disabled. This flag shall be set to '1' on a '1' to '0' transition of the PR. PED will transition from '1' to '0' due to the as-sertion of PR. This flag may be used by software to enable or disable the operation of the USB2 Debug Capability. The USB2 Debug Capa-bility operation may be disabled by a disconnect event, the assertion of DCPORTSC PR, or by software. 0 = USB2 Debug Capability port is disabled. 1 = USB2 Debug Capability port is enabled. When the port is disabled (PED = '0') the port's link shall be disabled and remain there until PED is reasserted ('1') or (DCE or USBDCIEN) is negated ('0'). When PED is reasserted ('1'), it will not be reflected immediately, but shall be set to '1' only after a '1' to '0' transition of the PR. Note that the port is remains mapped to Debug Capability while PED = '0'. While PED = '0' the USB2 Debug Capability will appear to be disconnected to the Debug Host. This field is '0' if (DCE and USBDCIEN) or CCS are '0'.
0	RO	0	SUS	Current Connect Status (CCS): '1' = A Root Hub port is connected to a Debug Host and assigned to the Debug Capability. '0' = No Debug Host is present. This value reflects the current state of the port, and may not correspond to the value reported by the Connect Status Change (CSC) field in the Port Status Change Event that was generated by a '0' to '1' transition of this bit. This flag is '0' if Debug Capability Enable (DCE) and USB DCI Enable (USBDCIEN) bits are '0'.

Table 304. Debug Capability Context Pointer Register (DCCP)

Memory Mapped IO Space
Address Offset:30-37h
See xHCI spec for details

Table 305. Debug Capability Device Descriptor Info Register 1 (DCDDI1)

Memory Mapped IO Space
Address Offset:38-3Bh
See xHCI spec for details

Table 306. Debug Capability Device Descriptor Info Register 2 (DCDDI2)

Memory Mapped IO Space
Address Offset:3C-3Fh
See xHCI spec for details

4.4.4.8 Vendor Defined Debug Capability Config Registers

This section describes configuration bits that provide proprietary control for USB Debug Device.
Note: bU1DevExitLat and bU2DevExitLat fields returned in BOS Descriptor read will be taken from the corresponding fields from the Host Controller space.

Base Offset = 8740h

Table 307. Debug Capability Descriptor Parameters

Memory Mapped IO Space
Address Offset:00-03h
Default Value:0000_0000h
Access: RO; RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:24	RO	0h	NA	Reserved
23:16	RW	00h	Core	Max Power Field This field will be used by USB Debug Device to report maximum power consumption when the device is fully operational. This value is returned by bMaxPower field in response to Configuration Descriptor read from the debug device.
15:8	RW/L	30h*	Core	Next Capability Pointer See Note below for configurability
7:0	RW/L	C3h	Core	Capability ID

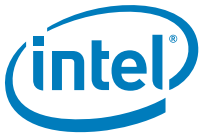
Note: Next Capability pointer = 00h if NumSSICPorts = 0

Table 308. DBGDEV_CTRL_TRM_REG1 – Debug Device Control Transfer Manager (TRM)

Memory Mapped IO Space
Address Offset:04-07h
Default Value:0C20 1103h
Access: RW;
Size:32 bits
This register contains fields which control the behavior of the Transfer Manager in the Debug Device logic implemented in DbC.
The functions controlled by this register are made available largely for debug/diagnostic purposes. This configurability is above and beyond that defined in the xHCI specification.
NOT for EDS

Bit	Access	Default Value	RST/PWR	Description
31	RW	0h	Core	Reserved. It must set to 0 .
30:28	RO	0h	Core	RESERVED
27	RW	1h	Core	This bit has been modified for its usage since PPTA0. It is used to allow NO-OP TRB to be treated in a same way as link TRB. In other words, it will update the internal context when it is fetched while the internal context cache TRB FIFO is empty. 1: enabled the cache function 0: disable the function
26	RW	1h	Core	This is a special internal condition enable for CPL engine which it enables all EP halt conditions detected to cause the proper actions in a response. 1: enabled 0: disabled Note: only default condition of 1 is validated.
25	RO	0h	Core	RESERVED
24	RW	0h	Core	This is a special internal branch condition control in XFER engine which does the EP transfer ring process. When this bit is set, the XFER will not continue even if the next TRB is identified as a non DMA TRB. The engine will then wait for the next scheduled request for this EP. 1: enabled the branch condition 0: disabled.

Bit	Access	Default Value	RST/PWR	Description
23	RW	0h	Core	When ERDP register is updated by software, it is expected as an atomic function since this is a 64bit register. It is expected that the ERDP (64bits register) is updated together when ERDP high 32 is written. We have this bit designed to ignore the atomic operation required from software for ERDP low 32bits. When this bit is set to 1, it will update the ERDP low 32bits when software issues a CPU write to the ERDP low 32 bit. 1: ignore atomic operation 0: not ignore.
22	RW	0h	Core	Setting this bit to 1 will force an internal doorbell ring on the EP that it has received a response.
21	RO	0h	Core	RESERVED
20	RW	1h	Core	0: Disable timeout of TRB error processing. 1: Enable timeout of a TRB processing in few critical states that possibly have a deadlock for unexpected reason. A vendor defined completion code is generated in the event of a timeout during TRB processing.
19	RO	0h	Core	RESERVED
18	RW	0h	Core	This bit is modified to enable the NOOP TRB as a TD when Missing Service Interval Error has encountered. This is only for PPT B0, LPT and CB. 1: enabled 0: disabled
17:14	RO	0h	Core	RESERVED
13	RW	0h	Core	0: Bulk and interrupt endpoints use burst size defined by endpoint context. 1: Force the Bulk and Interrupt endpoints use a burst size of 1.
12	RW	1h	Core	0: ENT bit is ignored. 1: ENT bit is processed. The transfer engine will service the next TRB.
11	RW	0h	Core	Setting this bit to 1 will force the transfer engine to set the packet boundary flag. This flag is an important flag which may cause a deadlock. This is a safety feature that we pluged in.
10	RO	0h	Core	RESERVED
9	RW	0h	Core	Setting this bit to 1 will force the transfer engine state machine to exit the CPL_WAIT state. This is designed to avoid unexpected deadlock in CPL_WAIT state.
8	RW	1h	Core	0: Disable internal TRB cache invalidation. 1: Enable internal TRB cache invalidation auto detect function This will allow engine to handle more than 4TRBs per packet.
7:6	RO	0h	Core	RESERVED
5	RW	0h	Core	Enable a function which we can clear mask of an EP on any response of that EP. 0: Clear the scheduler mask normally. 1: Clear the scheduler mask on each received packet.



Bit	Access	Default Value	RST/PWR	Description
4	RW	0h	Core	This bit is designed to allow XFER engine to do a transfer without checking against the available port credit. 0: Advertises accurate buffer credit information to the scheduler. 1: Advertises non-zero buffer credits to the scheduler. (e.g. never backpressure back on buffer credit information)
3	RO	0h	Core	RESERVED
2	RW	1h	Core	Generation of Completion Code for LINK/NOOP TRB
1	RO	0h	Core	RESERVED
0	RW	1h	Core	0: Disable TD pacing for IN endpoint. 1: Enable TD pacing for IN endpoints.

Table 309. DBGDEV_CTRL_ODMA_REG – Debug Device Control ODMA

Memory Mapped IO Space
Address Offset: 08- 0Bh
Default Value:0004 2000 h
Access: RO; RW;
Size:32 bits
This register contains a number of fields that provide a specific level of configurability for the OUT DMA that is part of Debug Device logic.
This configurability is above and beyond that defined in the xHCI specification.

Bit	Access	Default Value	RST/PWR	Description
31:19	RO	0h	Core	RESERVED
18	RW	1h	Core	Setting this field will enable ACK FIFO credit accounting. ODMA will ensure that ample room exists in the ACK FIFO for expected device responses prior to initiating a given DP
17:14	RO	0h	Core	RESERVED
13	RW	1h	Core	Setting this field will enable ACK FIFO individual credit accounting mechanisms for Async vs. Periodic Endpoints. ODMA will ensure that ample room exists in the ACK FIFO for expected device responses prior to initiating a given DP
12:9	RO	0h	Core	RESERVED
8	RW	0h	Core	Setting this field generates a pulse that clears the ownership of the context semaphore that is shared between the Out DMA Response and Completion Finite State Machines
7	RW	0h	Core	Setting this field generates a pulse that implicitly returns all of the Out DMA ACK credits on all ports
6	RO	0h	Core	RESERVED
5	RW	0h	Core	Setting this field generates a pulse that returns the Out DMA Completion Finite State Machine into the IDLE state
4	RW	0h	Core	Setting this field generates a pulse that returns the Out DMA Response Finite State Machine into the IDLE state
3	RW	0h	Core	Setting this field generates a pulse that returns the Out DMA Read Finite State Machine into the IDLE state
2:0	RO	0h	Core	RESERVED

Table 310. DBGDEV_CTRL_IDMA_REG – Debug Device Control IDMA

Memory Mapped IO Space
Address Offset: 0C- 0Fh
Default Value:0000 0000h
Access: RW;
Size:32 bits

This register contains a number of fields that provide a specific level of configurability for the IN DMA in the Debug Device logic.
This configurability is above and beyond that defined in the xHCI specification.
NOT for EDS

Bit	Access	Default Value	RST/PWR	Description
31	RO	0h	Core	RESERVED
30	RW	0h	Core	Setting this field will allow the Event Manager to treat either Transfer Manger (when 1) or Completion Engine (when 0) Event requests with higher priority. This bit is used by Event Manager
29	RW	0h	Core	Setting this field will allow the Doorbell Manager to post events on a given transfer ring
28:25	RO	0h	Core	RESERVED
24	RW	0h	Core	0: Flush the Asynchronous Address FIFO when bit[18] is strobed 1: Flush the Periodic Address FIFO when bit[18] is strobed
23:19	RO	0h	Core	RESERVED
18	RW	0h	Core	Setting this field will generate a strobe causing a give Periodic or Asynchronous Address FIFO to flush. FIFO flushed is a function of bits [25:19]
17	RO	0h	Core	RESERVED
16	RW	0h	Core	0: Default IDMA Pointer Buffer Room to a default value of 8. Requires a strobe of bit[3] to take effect. 1: Default IDMA Pointer Buffer Room to a default value of 4. Requires a strobe of bit[3] to take effect.
15	RW	0h	Core	Setting this field will prohibit IDMA from automatically dropping received DPs when a given endpoint currently has no outstanding transactions
14	RW	0h	Core	Setting this field will prohibit IDMA from automatically dropping received DPs when a given endpoint is currently in a flow controlled state
13:8	RO	0h	Core	RESERVED
7	RW	0h	Core	Setting this field generates a pulse that clears the ownership of the context semaphore that is shared between the IN DMA Acknowledge and Data Mover Finite State Machines
6	RW	0h	Core	Setting this field generates a pulse that returns the IN DMA Data Mover Finite State Machine into the IDLE state
5	RW	0h	Core	Setting this field generates a pulse that returns the IN DMA Acknowledge Finite State Machine into the IDLE state
4	RW	0h	Core	Setting this field generates a pulse that implicitly returns all of the IN DMA Data Packet credits on all ports
3	RW	0h	Core	Setting this field generates a pulse that clears all the Read and Write Pointers associated with the various DMA Address FIFOs causing them to appear empty
2:0	RO	0h	Core	RESERVED

Table 311. DGGDEV_CTRL_TRM_REG2 – Debug Device Control Transfer Manager (TRM)

Memory Mapped IO Space
Address Offset: 10- 13h
Default Value:F080 0084h
Access: RW;

Size:32 bits
This register contains fields which control the behavior of the Transfer Manager in the Debug Device logic.
The functions controlled by this register are made available largely for debug/diagnostic purposes.
This configurability is above and beyond that defined in the xHCI specification.
NOT for EDS

Bit	Access	Default Value	RST/PWR	Description
31	RW	1h	Core	This bit is added for bug FR2601. It is for cache invalidate case where xHC engine needs to insert wait states for completion engine when the completion has received a short packet before XFER engine has finished the TRB fetch for this packet at its packet boundary. 1: enables the feature 0: disabled
30	RW	1h	Core	This bit is added for bug FR2642. It is to delay the completion engine to generate an event due to internal error conditions that halted an EP until XFER engine has reached a packet boundary. 1: enabled 0: disabled
29	RW	1h	Core	This bit is added for bug FR2639. It enables the internal functions where xHC engine needs to immediately serve the EP again. 1: enabled 0: disabled
28	RW	1h	Core	This bit is added for bug FR2495. It enables that error completion code of the first error condition detected within an TD so that we can report the same error completion codes for all other TRBs within this TD. 1: enables the feature 0: disabled
27	RW	0h	Core	This bit disables a new feature where xHC engine will have an ODMA FIFO added for the commands between TRM and ODMA so that we can avoid the back-pressure situation due to the number of outstanding PCIe read limitation. This is for performance enhancement. 1: feature disabled 0: enabled
26:24	RO	0h	Core	RESERVED
23	RW	1h	Core	This bit is added for bug FR2283. This is to ensure only 1 clear pulse generated when a completion has received. 1: enabled 0: disabled
22:21	RO	0h	Core	RESERVED
20	RW	0h	Core	This bit enables a new feature where the completion engine of TRM can check the credit returned from remote device to not exceed its max burst size. If it does, we will keep the internal credits in the context to the max burst size so that xHC engine will not transmit more than max burst size. Note: CB has this bit default set to 0 PPT B0 and LPT will have this bit set to 1. 1: enabled 0: disabled

Bit	Access	Default Value	RST/PWR	Description
19	RW	1h	Core	This bit enables an internally detected deadlock situation being treated as an TRB_ERR when reports the event. This is an internal debug function. 1: enabled 0: disabled
18	RO	0h	Core	RESERVED
17	RW	0h	Core	This bit enables xHC engine to evaluate the next TRB even if the EP is at the end of a TD. 1: enables the feature 0: disables the feature
16:15	RO	0h	Core	RESERVED
14	RW	0h	Core	New feature added to prevent the back-pressure from ODMA due to the fact that it ran out of ODMA timeout timer resources. This is for performance enhancement. We have put into the ODMA credit is part of resource calculation before TRM allows the next scheduling for OUT EP. 1: enables this feature 0: Disables this feature
13	RW	0h	Core	The xHC engine has a feature that can check with Receive Port Credit per root port to whether or not allowed the next schedule onto this port. This is for performance enhancement. This bit enables this feature 1: Feature enabled 0: Feature disabled
12:8	RO	0h	Core	RESERVED
7	RW	1h	Core	1: enable a packet pace function under a special condition. This is an internal feature to XFER engine. It is not expected to be used other than default. 0: disable this function.
6:4	RO	0h	Core	RESERVED
3	RW	0h	Core	1: enable the address device command to query a port credit before it is executed in ODMA engine. 0: Disable this function.
2	RW	1h	Core	1: enable the credit redeem when a port is in NC state. 0: Disable the credit redeem
1	RO	0h	Core	RESERVED
0	RW	0h	Core	1: enable XFER engine to process a reserved TRB type as a NO-OP TRB 0: report TRB ERR for reserved TRB type.

Table 312. DBGDEV_CTRL_REG1 – Debug Device Control Register 1

Memory Mapped IO Space
Address Offset: 14- 17h
Default Value:0000 000Ch
Access: RW;
Size:32 bits
This register contains fields which control the behavior of the Debug Device logic.
The functions controlled by this register are made available largely for debug/diagnostic purposes. This configurability is above and beyond that defined in the xHCI specification.
NOT for EDS

Bit	Access	Default Value	RST/PWR	Description
31:16	RW	0h	Core	Per SS Port masking of Debug Capability. When a bit is set, the corresponding SS port will not attempt training as a Debug Device Capable upstream device. When a bit is not set, the corresponding SS port will train as Debug Device capable upstream port when DCE = 1
15: 4	RW	0h	Core	Reserved
3	RW	1h	Core	1: enable setting of Halt flag on TD Babble error. TD Babble will trigger Stall event. 0: disable setting of Halt flag on Babble error. TD Babble will not trigger a Stall event
2	RW	1h	Core	1: enable setting of Halt flag on TRB Error event. TRB error will trigger Stall event 0: disable setting of Halt flag on TRB Error. TRB error will not trigger Stall event
1	RW	0h	Core	1: enable generation of STALL event for vendor defined errors. Vendor defined errors are treated as halt condition. 0: Disable generation of STALL event for vendor defined errors. Vendor defined errors are not treated as halt conditions
0	RW	0h	Core	1: disable handling of TD Babble as a fatal error 0: TD Babble is handled as fatal error, and EP is stalled.

Table 313. DGGDEV_CTRL_TRM_REG3- Debug Device Control Transfer Manager3 (TRM)

Memory Mapped IO Space
Address Offset: 18- 1Bh
Default Value:0000 0000h
Access: RW;
Size:32 bits
This register contains fields which control the behavior of the Debug Device logic
The functions controlled by this register are made available largely for debug/diagnostic purposes. This configurability is above and beyond that defined in the xHCI specification.
NOT for EDS

Bit	Access	Default Value	RST/PWR	Description
31:6	RW	0h	Core	Reserved
5	RW	0h	Core	Clear Active IN EP This register is used to clear the internal valid IN EP array that TRM stored in order to guarantee one IN EP per port. This register allows software to clear the valid bit of each port IN EP.
4	RW	0h	Core	Write 1 to force XFER Manager state to Idle
3	RW	0h	Core	Write 1 to force CPL Manager state to Idle
2	RW	0h	Core	Allow software to add once credit back to credit control unit
1	RW	0h	Core	Allow software to subtract one credit back to credit control unit.
0	RW	0h	Core	Update credit count thru chicken mode. allow software to subtract one credit back to Tx/Rx FIFO

Table 314. DBGDEV_ECOPOLICY - DbC ECO Policy Register

MMIO Space
Address Offset : 1C - 1Fh

Default Value:0000 0000h
Access: RW;
Size:32 bits
This register contains fields which control the behavior of the Debug Device logic
The functions controlled by this register are made available largely for debug/diagnostic purposes. This configurability is above and beyond that defined in the xHCI specification.
NOT for EDS

Bit	Access	Default Value	RST/PWR	Description
31:02	RW	0h	Core	Reserved 32-bit Chicken bit register for ECO/Future use

Table 315. DBCCTL – DbC Control

MMIO Space
Address Offset : 20– 23h

Bit	Access	Default Value	RST/PWR	Description
31:8	RO	0h	Core	Reserved
7	RW	0h	Core	SW DCE Select When set, selects DCE that is visible to SW. Default is DCCTRL.DCE.
6:2	RW	0h	Core	Soft Disconnect RX Detect Count Indicates the count of Rx detect durations to force soft disconnect
1	RW	0b	Core	Force DCE Mode 0: When DCE is set, the DbC switches to Mode 2 1: When DCE is set, the DbC switches to Mode 3
0	RW	0b	Core	Force Disconnect upon DCE : If this bit is set by BIOS, the DbC will temporarily Disconnect from the remote host if the DCE is set, and shortly thereafter re-connect. This allows the DbC to switch from Mode1 to Mode2 or Mode 3 operation upon DCE being set.

4.4.4.9 SSIC Policy and Implementation Specific Registers

Chicken bits and Policy bits associated with SSIC.
This capability starts at offset 8800h from MBAR.

Table 316. Capability ID Register

Address Offset: 00 – 03h

Bit	Access	Default Value	RST/PWR	Description
31:16	RO	00h	Core	Reserved
15:8	RO	40h	Core	Next Capability Pointer
7:0	RO	C4h	Core	Supported Protocol ID

Table 317. SSIC Global Configuration Control

Address Offset:04h – 07h,

Bit	Access	Default Value	RST/PWR	Description
31:18	RO	0h	NA	Reserved

Bit	Access	Default Value	RST/PWR	Description
17:16	RW	See Description	Core	T_ACT_H8_MARGIN Specifies the margin time added to the tActivate spec time of 100us in T_ACT_H8_TIME. 11: Reserved 10: 50us 01: 20us (default for ModPHY) 00: 10us (default for MIPI MPHY)
15:4	RO	0h	NA	Reserved
3	RW	See Description	Core	BB_PLL_OVRD_DURING_PWM Override BB PLL clock gating during PWM mode. 1: Keep BB PLL up during PWM mode (default for ModPHY) 0: No override (default for MIPI MPHY)
2	RW	0h	Core	CMN_LANE_PWRGATE_DIS This will disable the MPHY common lane power gate.
1	RW	0h	Core	HS_CLK_GATE_DIS This will disable the HS Clock gate request from XHCI to MIPI PLL.
0	RW	0h	Core	PWM_CLK_GATE_DIS This will disable the PWM Clock gate request from XHCI to MIPI PLL.

Table 318. SSIC Configuration Register 1

Address Offset: 08h-0bh
Port 1 ... N : 08h, 38h, ... ,(08h + (NumSSICPorts-1)*30h)
Up to a maximum of 4 SSIC Ports

Bit	Access	Default Value	RST/PWR	Description
31:30	RW	2/h	Core	NUM_RRAP_ATTEMPT Specify the number of RRAP access attempt if there was tRRAPInitiatorResponse timeout.
29:22	RW	08h	Core	TX_MIN_STALL (TX_Min_STALL_NoConfig_Time_Capability in MIPI PHY Spec). PA will ensure TX_MIN_STALL time in STALL before entering HS-BURST or HIBERN8. Specifies minimum time in SI in STALL state.
21:17	RW	0Bh	Core	PWM_EXIT_TIME This will be max of RX_Min_ActivateTime_Capability and TX_Min_SAVE_Config_Time_Capability in MIPI PHY Specs) Specifies minimum activate time needed in 10us steps. PA will wait PWM_EXIT_TIME time after exiting PWM to start HS-BURST. SSIC spec requires it to be at 100us. 0000 – 10us 0001 – 20us …… 1110 – 150us 1111 – 1ms For speedup mode this time would be in 1us steps.

Bit	Access	Default Value	RST/PWR	Description
16	RW	0		DSP_DISC_BURST_CLOSE_RRAP Send BURST Closure RRAP for DSP Disconnect Don’t send Burst Closure RRAP for DSP Disconnect. For device PWM exit would be indication for DSP Disconnect.
15:13	RW	03h	Core	TX_MIN_ACTIVATE_DEFAULT (TX_Min_ActivateTime in MIPI PHY Spec) Specifies minimum activate time pwm_exit_timeneeded in 500us steps. PA will wait TX_MIN_ACTIVATE time after DISABLE H8 exit to start of PWM Burst. 000 – 0.5ms 001 – 1ms …… 111 – 3.5ms SSIC spec requires it to be at 1.5ms. For speedup mode this time would be 50us to 350us in steps of 50us.
12	RW	0h	Core	RRAP_BYPASS Enables DFx Loopback test mode where RRAP command / response is bypassed for HS_CONFIG and PWM_BURST_CLOSURE. Host will still perform initial enter and exit PWM mode with no RRAP transfers.
11			Core	Reserved
10:8	RW	0h	Core	T_ACT_H8_EXIT Specifies minimum time in 100us steps for T_ACTIVATE_TIME to exit H8 , with margin added from register T_ACT_H8_MARGIN based on PHY characteristic. Val: Si Time / Fast Sim Time 000: 110us / 10us 001: 210us / 20us … 110: 710us / 70us 111: 5ms / 500us Spec required timing is 100us.
7:5	RW	0h	Core	MIN_HIBERN8_TIME Minimum time in HIBERN8 state Val: Si Time / Fast Sim Time 000 – 110us / 10us 001 – 210us / 20us ….. 110 – 710us / 70us 111 – 5ms / 500us PA will ensure MIN_HIBERN8_TIME in its TX HIBERN8. For speedup mode this time will be from 10us to 80us in steps of 10us.
4	RW	0b/1b SPT uses ‘1b’	Core	SSICRATE 1 – A Series (default for ModPHY) 0 – B Series (default for MIPI MPHY)

Bit	Access	Default Value	RST/PWR	Description
3:2	RW	0h	Core	HSGEAR 0=HS-G1 1=HS-G2 2=HS-G3 HS Gear information will be latched for controller use once program done is asserted and later when PWM is done.
1:0	RW	0h	Core	SSICLANE 0=Single lane 1=Bi-lane 2=Quad-lane

Table 319. SSIC Configuration Register 2

Address Offset: 0Ch-0Fh
Port 1 ... N : 0Ch, 3Ch, ... ,(0Ch + (NumSSICPorts-1)*30h)
Up to a maximum of 4 SSIC Ports

Bit	Access	Default Value	RST/PWR	Description
31	RW	0	Core	SSIC_PORT_UNUSED This indicates that no SSIC device is connected to the port and PORTSC register would always reflect DISCONNECTED. Once PROG_DONE is set, this bit cannot be changed.
30	RW	0	Core	PROG_DONE BIOS will program this bit once SSIC profile programming is done. SSIC will enable the MPHY and local PLL once this bit is set.
29:26	RW	1h	Core	NUM_OF_MK0 Number of MK0 which transmitter will send before sending any data. . This field is multiple of 4. e.g. 0000 – 4 MK0 0001 – 8 MK0 ….. 1111 – 64 MK0
25	RW	0h	Core	DISABLE_SCRAMBLING This bit will disable scrambling in HS-BURST. The Driver should program DISABLE_SCRABLING on the remote side through profile.
24:21	RW	4h	Core	RETRAIN_TIME Corresponds to time in 10us to detect improper training of the local and remote M-RX as part of HS-BURST entry. 0000 – Disabled 0001 – 10us 1110 – 140us …… 1111 – 1ms SSIC Spec specific 40 to 50us
20:16	RW	1h	Core	PHY_RESET_TIME Corresponds to time in 100ns, PA will drive PHY RESET for MIPI PHY. This is the minimum time PA will ensure PHY reset is asserted.

Bit	Access	Default Value	RST/PWR	Description
15:8	RW	1Fh	Core	LRST_TIME Corresponds to time in 100us PA will drive DIF-P for line reset. MIPI PHY specifies 3.1 ms Minimum. When this time is changed the corresponding tx line reset timer MPHY registers need to be matched. 0x00 - 100us 0x01 - 200us … 0x1E - 3.1ms … 0xFE - 25.5ms 0xFF - 100ms For speedup mode this time will be in steps of 5us.
7:0	RW	46h	Core	ACTIVATE_LRST_TIME (Corresponds to tResetDIFN) Specifies in step of 1ms period of time a DSP is required to drive a DIF-N prior to a LINE-RESET. SSIC spec defined range is 60-80ms. For speedup mode this time will be from 5us to 400us in steps of 5us.

Table 320. SSIC Configuration Register 3

Address Offset: 10h-13h
Port 1 ... N : 10h, 40h, ... ,(10h + (NumSSICPorts-1)*30h)
Upto a maximum of 4 SSIC Ports

Bit	Access	Default Value	RST/PWR	Description
31:28	RW	4h	Core	U0_STALL_TO Time in 2^[U-STALL_TO] clock for U0 STALL entry. If there is no packet in arbiter for U0_STALL_TO time, PA will enable U0 STALL if DISABLE_U0_STALL is not set. 0000 – 0011 (Not recommended) 0100 – 16 SSIC HS CLK …. 1111 – 32768 SSIC HS CLK
27	RW	0h	Core	MPHY TEST_MODE_EN When this bit is set, controller would not initiate any PWM once it enters PWM Mode. It will wait for tester to send Loopback RRAP Command.
26	RW	0h	Core	DL_PWR_GATE_DIS This will disable the MPHY data lane power gate. This will be effective in DISBALED, U3 and U2 state and it will override SSIC_PG_U3_DIS and SSIC_PG_U2_DIS.
25:21	RW	2h	Core	HIBERN8_ENTER_TX The time PA will drive DIF-N after last bit of Line-CFG before entering H8. In steps of 27ns for Rate A and 32ns for Rate B. Legal range is 50 to 1000ns.

Bit	Access	Default Value	RST/PWR	Description
20:19	RW	1h	Core	LUP_LDN_TIMER_MAX 00: 10 us 01: 250 us 10: 1000us /1ms 11: (Timer is disable and don't transmit LDN)
18:3	RO	0	Core	Reserved
2	RW	0h	Core	DISABLE_U0_STALL This bit will disable the STALL entry in U0
1	RW	0	Core	SSIC_PG_U3_DIS This disables MPHY DL PG during U3. For S0IX, this bit should remain cleared.
0	RW	0	Core	SSIC_PG_U2_DIS This disables MPHY DL PG during U2.

Table 321. SSIC Configuration Register 4

Address Offset: 14h-17h
Port 1 ... N : 14h, 44h, ... ,(14h + (NumSSICPorts-1)*30h)
Upto a maximum of 4 SSIC Ports

Bit	Access	Default Value	RST/PWR	Description
31:24	RW	64h	Core	LC_MAX_TIMER In steps of 1us. Default 100us
23:16	RW	64h	Core	ENTRY_TIMER_MAX In steps of 1us. Default 100us
15:8	RW	64h	Core	HP_PEND_TIMER_MAX In steps of 1us. Default 100us
7:0	RW	64h	Core	CRD_PEND_TIMER_MAX In steps of 1us. Default 100us

Table 322. SSIC Loopback Config Register

Address Offset: 18h-1Bh
Port 1 ... N : 18h, 48h, ... ,(18h + (NumSSICPorts-1)*30h)
Upto a maximum of 4 SSIC Ports

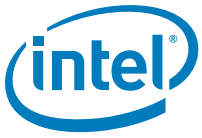
Bit	Access	Default Value	RST/PWR	Description
32:8			Core	RESERVED

Bit	Access	Default Value	RST/PWR	Description
7:4	RO	0h	Core	LOOPBACK_EN This Register is used to enable Conformance Loopback in the Target in the specified PAIR.. Bit [0]: • Writing 1'b1 enables the loopback mode in PAIR0. • Writing 1'b0 shall have no effect. Bit [1]: • Writing 1'b1 enables the loopback mode in PAIR1. • Writing 1'b0 shall have no effect. Bit [2]: • Writing 1'b1 enables the loopback mode in PAIR2. • Writing 1'b0 shall have no effect. Bit [3]: • Writing 1'b1 enables the loopback mode in PAIR3. • Writing 1'b0 shall have no effect.
3:0	RO	0h	Core	RX LOOPBACK CNTR RESET Reset RX_BURST_COUNT and RX_ERR_COUNT, write only, self-clearing. Bit [0] for PAIR0 Bit [1] for PAIR1 Bit [2] for PAIR2 Bit [3] for PAIR3

Table 323. SSIC Loopback Burst Count Register

Address Offset: 1Ch-1Fh
Port 1 ... N : 1Ch, 4Ch, ... ,(1Ch + (NumSSICPorts-1)*30h)
Upto a maximum of 4 SSIC Ports

Bit	Access	Default Value	RST/PWR	Description
31:24	RO	00h	Core	RX_BURST_COUNT_LANE3 RX_BURST_COUNT shall increment each time the M-RX of the PAIR under test detects a prepare time DIF-P. This shall be reset when the DUT receives a Write Command with rx_count_reset set to one. These counters shall not be reset when the DUT receives a LINE-RESET.
23:16	RO	00h	Core	RX_BURST_COUNT_LANE2 RX_BURST_COUNT shall increment each time the M-RX of the PAIR under test detects a prepare time DIF-P. This shall be reset when the DUT receives a Write Command with rx_count_reset set to one. These counters shall not be reset when the DUT receives a LINE-RESET.



Bit	Access	Default Value	RST/PWR	Description
15:8	RO	00h	Core	RX_BURST_COUNT_LANE1 RX_BURST_COUNT shall increment each time the M-RX of the PAIR under test detects a prepare time DIF-P. This shall be reset when the DUT receives a Write Command with rx_count_reset set to one. These counters shall not be reset when the DUT receives a LINE-RESET.
7:0	RO	00h	Core	RX_BURST_COUNT_LANE0 RX_BURST_COUNT shall increment each time the M-RX of the PAIR under test detects a prepare time DIF-P. This shall be reset when the DUT receives a Write Command with rx_count_reset set to one. These counters shall not be reset when the DUT receives a LINE-RESET.

Table 324. SSIC Loopback Error Count Register

Address Offset: 20h-23h
Port 1 ... N : 20h, 50h, ... ,(20h + (NumSSICPorts-1)*30h)
Upto a maximum of 16 SSIC Ports

Bit	Access	Default Value	RST/PWR	Description
32:24	RO	00h	Core	RX_ERR_COUNT_LANE3 RX_BURST_COUNT shall increment each time the M-RX of the PAIR under test detects a prepare time DIF-P. This shall be reset when the DUT receives a Write Command with rx_count_reset set to one. These counters shall not be reset when the DUT receives a LINE-RESET.
23:16	RO	00h	Core	RX_ERR_COUNT_LANE2 RX_BURST_COUNT shall increment each time the M-RX of the PAIR under test detects a prepare time DIF-P. This shall be reset when the DUT receives a Write Command with rx_count_reset set to one. These counters shall not be reset when the DUT receives a LINE-RESET.
15:8	RO	00h	Core	RX_ERR_COUNT_LANE1 RX_BURST_COUNT shall increment each time the M-RX of the PAIR under test detects a prepare time DIF-P. This shall be reset when the DUT receives a Write Command with rx_count_reset set to one. These counters shall not be reset when the DUT receives a LINE-RESET.
7:0	RO	00h	Core	RX_ERR_COUNT_LANE0 RX_BURST_COUNT shall increment each time the M-RX of the PAIR under test detects a prepare time DIF-P. This shall be reset when the DUT receives a Write Command with rx_count_reset set to one. These counters shall not be reset when the DUT receives a LINE-RESET.

4.4.4.10 SSIC Local and Remote Profile Registers

This capability starts at offset 8900h from MBAR.

Table 325. SSIC Capability Register

Address Offset: 00h - 03h

Bit	Access	Default Value	RST/PWR	Description
31:16	RO	0h	NA	Reserved
15:8	RW/L	FFh*	Core	Next Capability Pointer See Note below
7:0	RW/L	C5h	Core	Capability ID

Note: The next capability pointer is 00h if EPPortLock = False

Table 326. SSIC Port N Register Access Control

Address Offset:04h – 07h,
Port 1 ... N : 04h, 114h, 224h
Port N = 04h + (NumSSIClanes-1)* 110h
Upto a maximum of 3 SSIC ports

Bit	Access	Default Value	RST/PWR	Description
31:26	RO	0h	Core	Reserved
25	RW	0b	Core	Register Bank Valid 0 = No valid Commands in the Lane N register bank. Host Controller can close the PWM burst once commands from this register are completed. 1 = Valid commands present in the Lane N register bank. Host controller must complete commands from the register bank before closing the burst.
24	RW	0b	Core	Target Phy: 0 = Remote Phy 1 = Local Phy Setting this bit to '1' allows the use of this command mechanism to write to local Phy profile and AFE tuning registers – Primarily as a back up option.
23	RW	1b	Core	HS_Config: When this bit is set to '1' the host controller will issue an RRAP write with HS_Config=1 once it sees "Command Phase Done" = 1
22	RW	1b	Core	Command Phase Done When set to '1', this indicates that SW has completed performing RRAP cycles through the command register. SW can set this bit initially to indicate auto mode for Local and Remote MIPI MPHY registers. For Remote MIPI MPHY auto mode SW should ensure that CONFIG_FOR_HS is executed via HS_Config or through command.
21	RW	0b	Core	Command Valid: When written to '1' indicates that the Attribute ID and Attribute Data (for writes) fields are valid. This is set by SW and cleared by HW once command operation is done. SW should only program the next read/ write operation after that.
20	RW	0b	Core	Read_Write 0 = Write 1= Read
19:8	RW	000h	Core	Attribute ID Attribute ID that is being written or read

Bit	Access	Default Value	RST/PWR	Description
7:0	RW	00h	Core	Attribute Write Data Data byte that is required to be written to either the local phy or the remote phy

Table 327. SSIC Port N Register Access Status

Address Offset: 08h-0Bh
Port 1 ... N : 08h, 118h, 228h
Port N = 08h + (NumSSIClanes-1)* 110h
Upto a maximum of 3 SSIC Ports

Bit	Access	Default Value	RST/PWR	Description
31:10	RO	0h	Core	Reserved
9:8	RW	0b	Core	Command Completion Status 00 = Command not complete 01 = Command complete with Success 10 = Command complete with Error These bits must be cleared before a new command is initiated.
7:0	RO	00h	Core	Read Data Data read as a result of the RRAP operation

Table 328. Profile Attributes: Port 1 ... N

Address Offsets:0Ch – 0Fh, upto 108h – 10Bh (for Port 1)
Default Value:00h
Access: RW;
Size:32 bits
64 Dwords per Port, upto a max. of 3 Ports.

Port 1: 0Ch,10h,...,108h

Port 2: 11Ch, 120h, … , 218h

Port 3: 22Ch, 230h, … , 328h

Repeat for NumSSIClanes ports,
Port N = 0Ch + (N-1)* 110h to 108h+(N-1)*110h
(where N = NumSSIClanes)

This bank of registers provides 64 Dwords per port to be used to store attributes that need to be written into the local and remote phy every time the link enters the PWM state.

Bit	Access	Default Value	RST/PWR	Description
31:28	RO	0h	Core	Reserved
27:16	RW	00h	Core	Attribute ID {Upper Address [3:0], Lower Address [7:0]}
15	RW	0b	Core	Valid When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	RW	0b	Core	Target Phy 0 = Remote Phy 1 = Local Phy
13:8	RO	0h	Core	Reserved
7:0	RW	0h	Core	Attribute Value

Table 329. Reserved Addresses: Ports 1 ... N

Address Offsets:10Ch – 113Fh, upto 32Ch – 333h
Default Value:00h

Access: RO;
Size:32 bits
2 Dwords per Port,
Port 1: 10Ch, 110h
Port 2: 21Ch, 220h
Port 3: 32Ch, 330h
Repeat for NumSSIClanes
Port N = 10Ch + (N-1)* 110h to 110h+(N-1)*110h
Where N = 1 to 3
Upto a max. of 3 ports

These two DWORDs are left reserved per Port.

4.4.4.11 EP Type Based Port Lock

Base Offset = 8CFCh

Table 330. EP Type Based Port Lock Capability Register
Address Offset: 00h - 03h

Bit	Access	Default Value	RST/PWR	Description
31:16	RO	0h	NA	Reserved
15:8	RW/L	45h	Core	Next Capability Pointer
7:0	RW/L	C8h	Core	Capability ID

Note: The next capability pointer is 00h if TimeSync = False

Table 331. EP Type Lock Policy 1
Address Offsets:04h - 07h
Default Value:00h
Access: RW/L; (this register can be written until the access control is set)
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:8	RO	0h	NA	Reserved
7	RW/L	0	Core	Interrupt IN EP Type: 0 - Interrupt IN EP is allowed 1 - Interrupt IN EP is not allowed
6	RW/L	0	Core	Bulk IN EP Type 0 - Bulk IN EP is allowed 1 - Bulk IN EP is not allowed
5	RW/L	0	Core	Isochronous IN EP Type 0 - Isoch IN EP is allowed 1 - Isoch IN EP is not allowed
4	RW/L	0	Core	Control EP Type 0 - Control EP is allowed 1 - Control IN EP is not allowed
3	RW/L	0	Core	Interrupt OUT EP Type 0 - Interrupt OUT EP is allowed 1 - Interrupt OUT EP is not allowed

Bit	Access	Default Value	RST/PWR	Description
2	RW/L	0	Core	Bulk OUT EP Type 0 - Bulk OUT EP is allowed 1 - Bulk OUT EP is not allowed
1	RW/L	0	Core	Isochronous OUT EP Type 0 - Isoch OUT EP is allowed 1 - Isoch OUT EP is not allowed
0	RW/L	0	Core	Policy 1 Enable When set, enables Policy #1 to be globally enabled.

Table 332. EP Type Lock Policy 2

Address Offsets:08h - 0Bh
Default Value:00h
Access: RW/L; (this register can be written until the access control is set)
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:8	RO	0h	NA	Reserved
7	RW/L	0	Core	Interrupt IN EP Type: 0 - Interrupt IN EP is allowed 1 - Interrupt IN EP is not allowed
6	RW/L	0	Core	Bulk IN EP Type 0 - Bulk IN EP is allowed 1 - Bulk IN EP is not allowed
5	RW/L	0	Core	Isochronous IN EP Type 0 - Isoch IN EP is allowed 1 - Isoch IN EP is not allowed
4	RW/L	0	Core	Control EP Type 0 - Control EP is allowed 1 - Control IN EP is not allowed
3	RW/L	0	Core	Interrupt OUT EP Type 0 - Interrupt OUT EP is allowed 1 - Interrupt OUT EP is not allowed
2	RW/L	0	Core	Bulk OUT EP Type 0 - Bulk OUT EP is allowed 1 - Bulk OUT EP is not allowed
1	RW/L	0	Core	Isochronous OUT EP Type 0 - Isoch OUT EP is allowed 1 - Isoch OUT EP is not allowed
0	RW/L	0	Core	Policy 2 Enable When set, enables Policy #1 to be globally enabled.

Table 333. EP Type Lock Policy 3

Address Offsets:0Ch - 0Fh
Default Value:00h
Access: RW/L; (this register can be written until the access control is set)
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:8	RO	0h	NA	Reserved
7	RW/L	0	Core	Interrupt IN EP Type: 0 - Interrupt IN EP is allowed 1 - Interrupt IN EP is not allowed
6	RW/L	0	Core	Bulk IN EP Type 0 - Bulk IN EP is allowed 1 - Bulk IN EP is not allowed
5	RW/L	0	Core	Isochronous IN EP Type 0 - Isoch IN EP is allowed 1 - Isoch IN EP is not allowed
4	RW/L	0	Core	Control EP Type 0 - Control EP is allowed 1 - Control IN EP is not allowed
3	RW/L	0	Core	Interrupt OUT EP Type 0 - Interrupt OUT EP is allowed 1 - Interrupt OUT EP is not allowed
2	RW/L	0	Core	Bulk OUT EP Type 0 - Bulk OUT EP is allowed 1 - Bulk OUT EP is not allowed
1	RW/L	0	Core	Isochronous OUT EP Type 0 - Isoch OUT EP is allowed 1 - Isoch OUT EP is not allowed
0	RW/L	0	Core	Policy 3 Enable When set, enables Policy #1 to be globally enabled.

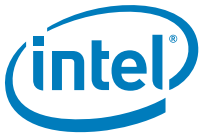
Table 334. Port Lock Control - Port 1 … N

Address Offsets:10h, 14h, … extend to Maxports count.
Default Value:00h
Access: RW/L; (this register can be written until the access control is set)
Size:32 bits
Repeat Maxports times
Addresses:
Port 1 = 10h,
Port 2 = 14h,
Port 3 = 18h …
Port (Maxports) = 10+(Maxports - 1) * 4
Maxports is no more than 64

Bit	Access	Default Value	RST/PWR	Description
31:8	RO	0h	NA	Reserved
7	RW/L	0	Core	Enable USB Lock Policy on root port number N: 00h - Port lock not enabled on port N 01h - Policy 1 enabled on port N 02h - Policy 2 enabled on port N 03h - policy 3 enabled on port N 4h to FFh - Reserved

Table 335. Private - EP Type Lock Policy 2 (18h)

Address Offsets:18h - 1Bh
Default Value:00h



Access: RW/L; (this register can be written until the access control is set)
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:8	RO	0h	NA	Reserved
7	RW/L	0	Core	Interrupt IN EP Type: 0 - Interrupt IN EP is allowed 1 - Interrupt IN EP is not allowed
6	RW/L	0	Core	Bulk IN EP Type 0 - Bulk IN EP is allowed 1 - Bulk IN EP is not allowed
5	RW/L	0	Core	Isochronous IN EP Type 0 - Isoch IN EP is allowed 1 - Isoch IN EP is not allowed
4	RW/L	0	Core	Control EP Type 0 - Control EP is allowed 1 - Control IN EP is not allowed
3	RW/L	0	Core	Interrupt OUT EP Type 0 - Interrupt OUT EP is allowed 1 - Interrupt OUT EP is not allowed
2	RW/L	0	Core	Bulk OUT EP Type 0 - Bulk OUT EP is allowed 1 - Bulk OUT EP is not allowed
1	RW/L	0	Core	Isochronous OUT EP Type 0 - Isoch OUT EP is allowed 1 - Isoch OUT EP is not allowed
0	RW/L	0	Core	Policy 2 Enable When set, enables Policy #1 to be globally enabled.

4.4.4.12 Global Time Synchronization

Base Offset = 8E10h

Table 336. Global Time Sync Capability Register

Address Offset: 00h - 03h
Default Value:00h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:16	RO	0h	NA	Reserved
15:8	RW/L	06h	Core	Next Capability Pointer
7:0	RW/L	C9h	Core	Capability ID

Table 337. Global Time Sync Control Register

Address Offset: 04 - 07h
Default Value:00h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:01	RO	0h	Core	Reserved
0	RW1S	0b	Core	Time Stamp Counter Capture Initiate SW sets this bit to initiate a time capture. Once the time capture is complete and the time values are valid in the Local and Global time capture registers, HW clears the bit.

Table 338. MicroFrame Time (Local Time)

Address Offset: 08 - 0Bh
Default Value:00h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:30	RO	0h	Core	Reserved
29:16	RO	0h	Core	Captured Frame List Current Index/Frame Number (CMFI) : The value in this register is updated in response to sample_now signal. Bits [29:16] reflect state of bits [13:0] of FRINDEX
15:13	RO	0h	Core	Reserved
12:0	RO	0h	Core	Captured Micro-frame BLIF (CMFB): The value is updated in response to sample_now signal and provides information about offset within micro-frame. Captured value represents number of 8 high-speed bit time units from start of micro-frame. At the beginning of micro-frame captured value will be 0 and increase to maximum value at the end. Default maximum value is 7499 but it may be changed as result of adjustment done via Bus Interval Adjust (BIA).

Table 339. Global Time (Low)

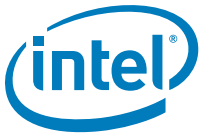
Address Offset: 10 - 13h
Default Value:00h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:0	RO	0h	Core	Global Time Value (Low): Lower Dword of the Global time value captured based on the time sync initiated by SW.

Table 340. Global Time (High)

Address Offset: 14 - 17h
Default Value:00h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:0	RO	0h	Core	Global Time Value (High): Upper Dword of the Global time value captured based on the time sync initiated by SW.



4.4.4.13 USB3.1 Policies

Base Offset = 8E58h

All registers under this capability will be saved and restored expect HOST_CTRL_USB3_DEBUG_REG1/2/3.

Table 341. USB3p1 Policies Capability Register

Address Offset: 00h - 03h
Default Value:00h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:16	RO	0h	NA	Reserved
15:8	RW/L	00h	Core	Next Capability Pointer
7:0	RW/L	CAh	Core	Capability ID

Table 342. HOST_CTRL_SSP_LINK_PORT_REG1

Address Offset: 04 – 07h
Default Value:00h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
[31:USB3_PORTS]	RO	0	PGD	Reserved
[SSP-PORTS-1:0]	RW	0	PGD	GEN2_ENABLE 0: LBPM will advertise Gen2 Speed by default 1: LBPM will advertise Gen1 Speed by default

Table 343. HOST_CTRL_SSP_LINK_PORT_REG2

Address Offset: 08 – 0Bh
Default Value:00h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
[31:USB3_PORTS]	RO	0	PGD	RESERVED
[SSP-PORTS-1:0]	RW	0	PGD	SSP_LPBK_REPEATER: This will set the local loopback in repeater bit (Bit 4) set in Symbol 5 of TS1/TS2. (Bit2 and Bit3 will be controlled by HOST_CTRL_PORT_LINK_REG)

Table 344. HOST_CTRL_SSP_LINK_REG1

Address Offset: 0C – 0Fh
Access: RW;

Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31	RW	0	PGD	RXDTVAL_DEASSERT_EBEMPTY_DIS When set, XHCI will disable the support for the RxDataValid Deassertion because of EB Empty during a data block for SSP. In this case the recommended setting for the PHY is Half Full.
30	RW	0	PGD	LFPS_BYPASS Setting this to 1 will force the LTSSM to bypass LFPS Polling and LBPM altogether. This will be used only for HBP, FPGA or simulation.
29	RW	0	PGD	PORT_SPEED_SEL Setting this bit to 1 will force the port to switch to Gen2 mode unconditionally without SCD detection.
28	RW	0	PGD	TSEQ_OS_PHY_SIM_COUNT When set, link will send around 45us of TSEQ for Gen1 / Gen2 overriding TSEQ_OS_COUNT register. This is simulation mode only to give enough time for PHY to train. For Gen1, it will send 3000 TSEQ and for Gen2 it will send 3600 TSEQ.
27	RW	0	PGD	FORCE_COMP Set by software to switch to compliance pattern defined by FORCE_COMP_PATTERN instead of waiting for the Ping.LFPS. This is self-clearing bit set by software and cleared by hardware when switching is complete.
26:22	RW	0	PGD	FORCE_COMP_PATTERN Compliance pattern to be forced when FORCE_COMP is set.
21:17	RW	16	PGD	RXDTVALID_DEASSRT_CNT This register specifies the count for port clock for which RxDataValid remains de-asserted as the End of the High Speed Data while entering UX state in Gen2 mode. SSP RX Path will generate a fake pulse to advance the internal pipeline based on this value.
16:14	RW	7	PGD	SKP_THRESHOLD 000 – SKP OS every 20 Blocks 001 – SKP OS every 30 Blocks 010 – SKP OS every 35 Blocks 011 – SKP OS every 36 Blocks 100 – SKP OS every 37 Blocks 101 – SKP OS every 38 Blocks 110 – SKP OS every 39 Blocks 111 – SKP OS every 40 Blocks (Default)
13:12	RW	01	PGD	SKP_OS_LENGTH 00 – 16 Symbol OS Block 01 – 24 Symbol OS Block (Default) 10 – 32 Symbol OS Block
11	RW	1	PGD	DIS_PTM_GEN1 0 – Enable PTM as per specification. 1 – Disable PTM (Do not generate LDM LMP)

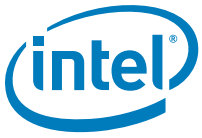
Bit	Access	Default Value	RST/PWR	Description
10	RW	0	PGD	DIS_PTM_GEN2 0 – Enable PTM as per specification. 1 – Disable PTM (Do not generate LDM LMP)
9	RW	0	PGD	SYNC_POLICY_FOR_TS 0 – 1st SYNC will be sent out after 16384 TSEQ or 32 TS1/ TS2. (Default) 1 – 1st SYNC will be set out at start of POLLING or RECOVERY. (Simulation)
8	RW	0	PGD	DC_BAL_POLICY 0 – Spec defined Section 6.4.1.2.2 1 – Treat DC Balance of > 15 same as > 31
7	RW	0	PGD	DIS_DC_BALANCE 0 – DC Balance is Enabled 1 – DC Balance is Disabled
6	RW	1	PGD	TS1_TS2_IS_COUNT 0 – 16 TS1/TS2/IS are transmitted (Default) 1 – 32 TS1/TS2/IS are transmitted This is valid for Polling, Recovery and Hot Reset.
5:4	RW	2	PGD	TSEQ _OS_COUNT 0 – 32 (For Simulation) 1 – 262143 2 – 524288 (Default) 3 – 1048576
3:2	RW	3	PGD	SYNC_FREQ 0 – 8 for TSEQ and 8 for TS1/TS2 (Simulation Mode) 1 – 4096 for TSEQ and 16 for TS1/TS2 2 – 8192 for TSEQ and 16 for TS1/TS2 3 – 16384 for TSEQ and 32 for TS1/TS2 (Default)
1	RW	0	PGD	DIS_SSP_SCRAMBLE_TS This will Disable the SSP scramble for TSEQ, TS1 and TS2. This is not a spec defined mode and can only be used for validation. If set scrambling will remain disabled over riding the Link Configuration in TS1 and TS2. Disabling Scrambling will not impact DC Balance. HOST_CTRL_PORT_LINK_REG[5] will control the disable scrambling configuration for Data Phase.
0	RW	0	PGD	TX_SSP_CRD_POLICY When set, SSP link will not differentiate between Credit type 1 and Credit Type 2 to initiate a new transfer

Table 345. HOST_CTRL_SSP_LINK_REG2

Address Offset: 10 – 13h
Access: RW;

Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31	RW	0	PGD	END_OF_SCD_TX_MODE 0 - Send End of SCD when SCD transmission is complete 1 - Send End of SCD after each individual SCD
30	RW	0	PGD	SSP_SYMBOL_ERR_EN Chicken bit to enable / disable rxstatus bit 2 as the valid SSP error to count. 0 - Ignore rxsatus bit 2. 1 - Count rxstatus bit 2 assertion as an error.
29	RW	0	PGD	USB3_PULSE_QUEUE_MODE Chicken bit to select between Queue implementation between DMA and Port interface 0 - Use the new queue structure 1- Hols" Done" instead of queue to throttle incoming pulse.
28	RW	0	PGD	RXSTANDBY_TX_LFPS If set to '1', it will enable the rx receiver, while controller has started transmitted LFPS. This will only work if RXSTANDBY_UX_EXIT is set. This is not a recommended setting by the USB3 PHYs.
27	RW	0	PGD	RXSTANDBY_U3_EXIT If set to '1', it will enable rx receiver during U3 Exit when starting receiving RxElectIdle.
26	RW	0	PGD	RXSTANDBY_U2_EXIT If set to '1', it will enable rx receiver during U2 Exit when starting receiving RxElectIdle.
25	RW	0	PGD	RXSTANDBY_U1_EXIT If set to '1', it will enable rx receiver during U1 Exit when starting receiving RxElectIdle.
24:23	RW	00	PGD	RXSTANDBY_RECOV_TO Time to keep rxstandby on while entering Recovery from U2/U3 00 - Disabled, turn off immediately 01 - 1us-2us 10 - 81us-82us 11 - 128us-129us If set to nonzero value, RXSTANDBY_UX_EXIT should be kept 0.



Bit	Access	Default Value	RST/PWR	Description
22:20	RW	101	PGD	RXSTANDBY_RXEQ_TO Time to keep rxstandby on while entering RXEQ 000 – Disable, turn off immediately 001 – 1us-2us (Simulation time) 010 – 16us 011 – 32us 100 – 128us 101 – 160us 110 – 192us 111 – 256us
19:18	RW	00	PGD	RXSTANDBY_POLICY Force RXSTANDBY to ON or OFF 00 – Default (set / clear by LTSSM operation) 01 – Always Set 10 – Always Clear 11 – Illegal
17:16	RW	00	PGD	RXSTANDBY_RECOV_U1_TO Time to keep rxstandby on while entering Recovery from U1 00 - Disabled, turn off immediately 01 - 1us-2us 10 - 3us-4us 11 - 81us-82us If set to nonzero value, RXSTANDBY_U1_EXIT should be kept 0
15	RW	0	PGD	DIS_U1_SSIC Override to disable U1 for all SSIC Ports.
14	RW	0	PGD	DIS_U2_SSIC Override to disable U2 for all SSIC Ports.
13	RW	0	PGD	DIS_U1_SS Override to disable U1 for all SS/SSP Ports.
12	RW	0	PGD	DIS_U2_SS Override to disable U2 for all SS/SSP Ports.
11	RW	1	PGD	DIS_U1_DBC Override to disable U1 for all DBC or EXI DBC Ports.
10	RW	1	PGD	DIS_U2_DBC Override to disable U2 for all DBC or EXI DBC Ports.
9:8	RW	00	PGD	00 - Use RECOVERY.ACTIVE, RECOVERY.CONFIG, POLLING.RXEQ, POLLING.ACTIVE, POLLING.CONFIG and LOOPBACK.ACTIVE for block align control assertion. 01 - Set Block align control only during POLLING.ACTIVE and RECOVERY.ACTIVE and LOOPBACK.ACTIVE for both master and slave.10 - Use RECOVERY.ACTVE/POLLING.ACTIVE/ LOOPBACK.ACTIVE to trigger block align control till the time SDS OS is detected 11 - Use OS detection or entry to RECOVERY.ACTIVE/ POLLING.ACTIVE/LOOPBACK.ACTIVE to trigger block align control till the time SDS OS is detected.

Bit	Access	Default Value	RST/PWR	Description
7	RW	0	PGD	SSP_EDB_PKT_ERR_DIS When set to 1, it disables the packet error detection based on EDB framing at the end of packet for SSP. If DPP has EDB after CRC, port will not retry the packet and it will accept it.
6	RW	0	PGD	SSP_END_PKT_ERR_EN When set to 1, it enables the validity of END framing to accept a DPP as a valid DPP.
5	RW	0	PGD	CFG_RXSTANDBY_HDSK_DIS To disable the fix for the pclk assertion based on rxstandby status change in response to rxstandby.
4	RW	0	PGD	CFG_RXSTANDBY_WAIT_END_RXLFPS To disable the fix for which waits for the deassertion of rxelecidle to deassert the rxstandby exiting U1, U2 or U3 state.
3:0	RW	0	PGD	Reserved

Table 346. HOST_CTRL_LDM_DELAY_REG

Address Offset: 13 – 17h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:24	RW	00h	PGD	LDM_Datapath_SS_TX_Delay This is value in tIsochTimestampGranularity (16.667ns) units the delay between initiating the LDM response to the last symbol getting transmitted on the wire Calculating the Response Delay, this value is added to the response delay.
23:16	RW	00h	PGD	LDM_Datapath_SS_RX_Delay This is value in tIsochTimestampGranularity (16.667ns) units the delay between receiving the last symbol of LDM Request on the wire and the time that is latched internally. This value is calculated based on Path delay. Calculating the Response Delay, this value is subtracted from the actual latched time.
15:8	RW	00h	PGD	LDM_Datapath_SSP_TX_Delay This is value in tIsochTimestampGranularity (16.667ns) units the delay between initiating the LDM response to the last symbol getting transmitted on the wire Calculating the Response Delay, this value is added to the response delay.

Bit	Access	Default Value	RST/PWR	Description
7:0	RW	00h	PGD	LDM_Datapath_SSP_RX_Delay This is value in tIsochTimestampGranularity (16.667ns) units the delay between receiving the last symbol of LDM Request on the wire and the time that is latched internally. This value is calculated based on Path delay. Calculating the Response Delay, this value is subtracted from the actual latched time.

Table 347. HOST_CTRL_SSP_LFPS_REG1

Address Offset: 18 – 1Bh
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:29	RO	0	PGD	Reserved
28:23	RW	31d	PGD	TXLFPS_SCD_END_TREP Repeat time between two LFPS Bursts for SDC END. For normal mode of operation this will be multiple of 1us. For speedup mode, it will be multiple of 64ns starting from 384ns. 0: 1us / 256ns …. 31: 32us / 2240ns …. 63: 64us / 4480ns
22:18	RW	11d	PGD	TXLFPS_SCD1_TREP Repeat time between two LFPS Bursts for SDC1. For normal mode of operation this will be multiple of 1us. For speedup mode, it will be multiple of 64ns starting from 832ns. 0: 1us / 256ns …. 9: 10us / 832ns …. 31: 32us / 2240ns
17:13	RW	6d	PGD	TXLFPS_SCD0_TREP Repeat time between two LFPS Bursts for SDC0. For normal mode of operation this will be multiple of 1us. For speedup mode, it will be multiple of 64ns starting from 384ns. 0: 1us / 256ns …. 9: 10us / 832ns …. 31: 32us / 2240ns

Bit	Access	Default Value	RST/PWR	Description
12:10	RW	2d	PGD	TXLFPS_PING_TBURST Burst duration for Ping LFPS in order of 32ns. 0: 32ns … 2: 96ns (Default) .. 7: 256ns Speedup: 32ns
9:5	RW	9d	PGD	TXLFPS_TREP Repeat time between two LFPS Bursts during POLLING. For normal mode of operation this will be multiple of 1us. For speedup mode, it will be multiple of 64ns starting from 256ns. 0: 1us / 256ns …. 9: 10us / 832ns …. 31: 32us / 2240ns
4:0	RW	7d	PGD	TXLFPS_TBURST Duration for which one LFPS burst will be transmitted during POLLING. For normal mode of operation this will be multiple of 128ns. For speedup mode, it will be multiple of 32ns. 0: Illegal 1: 128ns/32ns …. 8: 1.024us/256ns …. 31: 3.968us/992ns

Table 348. HOST_CTRL_SSP_LFPS_REG2
Address Offset: 1C – 1Fh
Access: RW;

Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:28	RW	5d	PGD	TXLFPS_PING_TREP Repeat time for Ping LFPS. 0: 32ms / 8us 1: 64ms / 16us ……. 5: 192ms / 48us(Default) …… 15: 512ms / 128us
27:23	RW	13d	PGD	RXLFPS_TREP_MAX Max duration for detection of Polling LFPS Repeat between bursts. For normal mode of operation this will be multiple of 1us. For speedup mode, it will be multiple of 128ns. 0: 1us / 256ns …. 13: 14us / 1088ns (Default) 31: 32us / 2240ns
22:18	RW	3d	PGD	RXLFPS_TBURST_MIN Min duration for detection of Polling LFPS. For normal mode of operation this will be multiple of 128ns. For speedup mode, it will be multiple of 32ns. 0: 0.128us / 32ns …. 4: 0.640us / 160ns (Default) …. 31: 4.096us / 1024ns
17:13	RW	10d	PGD	RXLFPS_TBURST_MAX Max duration for detection of Polling LFPS. For normal mode of operation this will be multiple of 128ns. For speedup mode, it will be multiple of 32ns. 0: 128ns / 32ns …. 10: 1.408us / 352ns (Default) …. 31: 4.096us / 1024ns

Bit	Access	Default Value	RST/PWR	Description
12:9	RW	11d	PGD	TXLFPS_TLBPS1 LFPS Burst time for transmitting 1 for LBPS. For normal mode of operation this will be multiple of 128ns. For speedup mode, it will be multiple of 32ns. 0: 128ns / 32ns …. 11: 1.536us/384ns (Default) …. 15: 2.048us/512ns
8:5	RW	4d	PGD	TXLFPS_TLBPS0 LFPS Burst time for transmitting 0 for LBPS. For normal mode of operation this will be multiple of 128ns. For speedup mode, it will be multiple of 32ns. 0: 128ns / 32ns …. 4: 640ns / 160ns (Default) …. 15: 2.048us / 512ns
4:0	RW	16d	PGD	TXLFPS_TPWM Transmit PWM Period. For normal mode of operation this will be multiple of 128ns. For speedup mode, it will be multiple of 32ns. 0: 128ns / 32ns …. 16: 2.176us / 544ns (Default) …. 31: 4.096us / 1024ns

Table 349. HOST_CTRL_SSP_LFPS_REG3

Address Offset: 20 – 23h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31	RO	0	PGD	Reserved

Bit	Access	Default Value	RST/PWR	Description
30:27	RW	9d	PGD	RXLFPS_TLBPS1_MIN Min LFPS Burst time for detecting 1 for LBPS. For normal mode of operation this will be multiple of 128ns. For speedup mode, it will be multiple of 32ns. 0: 0.128us / 32ns …. 9: 1.280us / 320ns (Default) …. 15: 2.048us / 512ns
26:23	RW	14d	PGD	RXLFPS_TLBPS1_MAX Max LFPS Burst time for detecting 1 for LBPS. For normal mode of operation this will be multiple of 128ns. For speedup mode, it will be multiple of 32ns. 0: 0.128us / 32ns ….. 15: 2.048us / 512ns
22:19	RW	2d	PGD	RXLFPS_TLBPS0_MIN Min LFPS Burst time for detecting 0 for LBPS. For normal mode of operation this will be multiple of 128ns. For speedup mode, it will be multiple of 32ns. 0: 0.128us / 32ns …. 2: 0.384us / 96ns (Default) …. 15: 2.048us / 512ns
18:15	RW	6d	PGD	RXLFPS_TLBPS0_MAX Max LFPS Burst time for detecting 0 for LBPS. For normal mode of operation this will be multiple of 128ns. For speedup mode, it will be multiple of 32ns. 0: 0.128us / 32ns …. 6: 0.896us / 224ns (Default) …. 15: 2.048us / 512ns

Bit	Access	Default Value	RST/PWR	Description
14:10	RW	10d	PGD	RXLFPS_TGAP_SCD1_MIN Min duration for detection of Polling LFPS Gap between bursts to identify SCD Logic 1. For normal mode of operation this will be multiple of 1us. For speedup mode, it will be multiple of 64ns. 0: 1us / 256ns …. 10: 11us / 896ns (Default) …. 31: 32us / 2240us
9:5	RW	8d	PGD	RXLFPS_TGAP_SCD0_MAX Max duration for detection of Polling LFPS Gap between bursts to identify SCD Logic 0. For normal mode of operation this will be multiple of 1us. For speedup mode, it will be multiple of 64ns. 0: 1us / 256ns …. 8: 9us / 768ns (Default) …. 31: 32us / 4288ns
4:0	RW	4d	PGD	RXLFPS_TREP_MIN Min duration for detection of Polling LFPS Repeat between bursts. For normal mode of operation this will be multiple of 1us. For speedup mode, it will be multiple of 64ns. 0: 1us / 256ns …. 5: 6us / 576ns (Default) …. 31: 32us / 4288ns

Table 350. HOST_CTRL_SSP_LFPS_REG4

Address Offset: 24 – 27h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31	RO	0	PGD	Reserved
30:24	RW	100d	PGD	USB3_WARM_RESET_TIME This defines the time in multiple of 1ms for the Warm Reset. For fastsim, this time is multiple of 1us.

Bit	Access	Default Value	RST/PWR	Description
23:17	RW	60d	PGD	SCD_LFPS_TIMEOUT This corresponds to the tPollingSCDLFPSTimeout as defined in the USB3.1 Spec. For normal mode, this is multiple of 1us and for fast sim, it is multiple of 32ns. If set to '0', this timeout is disabled and LTSSM will move to RXEQ when other conditions are met.
16:14	RW	2d	PGD	SCD_TX_COUNT Number of SCD TX COUNT before moving to next state.
13:11	RW	4d	PGD	LBPM_TX_COUNT Number of LBPM TX COUNT before moving to next state.
10:5	RW	16d	PGD	Reserved (For AR, this is used for RXLFPS_GEN2_BAILOUT_CNT)
4:0	RW	18d	PGD	RXLFPS_TDELIM_MAX Max PWM Period for detecting a delimiter. For normal mode of operation this will be multiple of 128ns. For speedup mode, it will be multiple of 32ns. 0: 0.128us / 32ns …. 18: 2.432us / 608ns (Default) …. 31: 4.096us / 1024ns

Table 351. HOST_CTRL_SSP_CONFIG_REG1

Address Offset: 28 – 2Bh
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31	RW	0	PGD	0: Enable 10G DBC and EXI over DBC functionality 1: Disable 10G DBC and EXI over DBC functionality
30	RW	0	PGD	DIS_EDB_ARC When set, it will disable the fix for the EDB detection for SSP.
29	RW	0	PGD	SPR_DISC_4_DBC When set, SPR would force disconnect the DBC connection same as other Host connections.
28	RW	0	PGD	To disable the fix for generating a PME from legacy path, on detection of a disconnect in RXDETP3 when DAP request is deaserted.
27	RW	0	PGD	Disable the clearing of compliance flag on disconnect. (Alpine Ridge Only)
26	RW	0	PGD	Allowing back to back packets in the TX Packet arbitor. (Alpine Ridge Only)
25	RW	0	PGD	CFG_EB_LOC_DIS When set, EB Location will not be used for the LDM delay calculation.

Bit	Access	Default Value	RST/PWR	Description
24	RW	0	PGD	DIS_EDB_NULLIFIED_PKT_FIX When set, fix for the nullified packet based on EDB detection right after DPH would be disabled.
23	RW	0	PGD	DIS_DPH_WO_DPP_ERR When set, it will disable the detection of Error for DPH without DPP for SSP. Port will not trigger a Recovery for this error.
22	RW	0	PGD	When SET disables creating fake RXDATAVALID in SSP_DESCRAM on LTSSM in RECOV.ACTIVE state so as to enable capturing last Valid data before TS1s from Device "0" RTL Fix Enabled "1" RTL Fix Disabled
21	RW	0	PGD	EXTEND_SSP_GAP_TIMER When set, it will increase the protocol gap timer timeout from the DPH to DPP from 7pclk to 15pclk for SSP.
20:18	RW	0	PGD	EXTEND_POLL_ACT_GEN2 When set to non-zero value, Polling Active time will get extended for 1ms multiple of this field for Gen2. During this time XHCI will continue sending TS1. HOST_CTRL_PORT_LINK_REG[11:9] controls the Polling Active timeout in granularity of 128us, it would only be applicable if EXTEND_POLL_ACT_GEN* is set to zero.
17:15	RW	0	PGD	EXTEND_POLL_ACT_GEN1 When set to non-zero value, Polling Active time will get extended for 1ms multiple of this field for Gen1. During this time XHCI will continue sending TS1. HOST_CTRL_PORT_LINK_REG[11:9] controls the Polling Active timeout in granularity of 128us, it would only be applicable if EXTEND_POLL_ACT_GEN* is set to zero.
14	RW	0	PGD	EXTEND_RXEQTRAIN_POLLACT_GEN2 When set, XCHI will keep driving RxEqTraining PIPE signal while in Polling Active for Gen2 speed.
13	RW	0	PGD	EXTEND_RXEQTRAIN_POLLACT_GEN1 When set, XCHI will keep driving RxEqTraining PIPE signal while in Polling Active for Gen1 speed.
12	RW	0	PGD	RST_POLARITY_RXEQ When set, XHCI will reset the polarity signal to MODPHY when entering RXEQ. It will be re-established after receiving one valid SYNC OS. Default mode is that XHCI will enable it when entering Polling.Active.
11	RW	0	PGD	OS_DEC_ERR_EN When set, it will enable the OS decode error during Polling.Eq and Polling.Active for Gen2 speed. This is based on MODPHY PCR to have a feedback for the OS decode.
10	RW	0	PGD	When set enables link loopback master mode for AR Port 2 only. Not applicable to other projects. For AR port 1, it will be controlled by HOST_CTRL_PORT_LINK_REG[1]
9	RW	0	PGD	DIS_RST_BAILOUT_CNT When cleared, it will reset the bailout count whenever SCD1 or SCD2 is detected. This will help in those cases when devices or repeaters may send SCD1 for longer period of time without going into SCD2.

Bit	Access	Default Value	RST/PWR	Description
8:0	RW	16d	PGD	RXLFPS_GEN2_BAILOUT_CNT Number of LFPS Burst after which LFPS FSM will stop looking for Gen2. 0 - Disabled, Keep looking for Gen2 forever.

Table 352. HOST_CTRL_USB3_RECAL

Address Offset: 2C - 2Fh
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31	RW	0	PGD	Reserved
30	RW	0b	PGD	RECALB_U0_POLICY 0 - Triggers recalibration on U0 exit to Recovery. 1 - Disable U0 to Recovery exit based on RECALB_U0_THRESHOLD and recalibration is not triggered in recovery entry from U0.
29	RW	0b	PGD	RECALB_U3_POLICY 0 - Triggers recalibration on U3 exit. 1 - Disable U3 exit recalibration
28	RW	0b	PGD	RECALB_U2_POLICY 0 - Triggers recalibration on U2 exit. 1 - Disable U2 exit recalibration
27:20	RW	4h	PGD	RECALB_U1_THERSHOLD This field defines error threshold which will trigger Recovery and Recalibration while exiting U1.
19:18	RW	00b	PGD	RECALB_U1_POLICY 00 - Triggers recalibration if bit error count exceeds threshold. 01 - Always trigger recalibration on U1 exit. 10 - Disable U1 exit recalibration
17	RW	0b	PGD	RECALB_ERR_WINDOW_SIZE This defines the size of size of sliding window to accumulate the error for initiating Recovery and recalibration. 0 - 1ms (8 slices of 125us) 1 - 8ms (8 slices of 1ms)
16	RW	0b	PGD	RECALB_DIS_FOR_GEN1 Setting to '1', it will globally disable the recalibration if port operating speed is Gen1.
15:8	RW	4h	PGD	RECALB_THRESHOLD_GEN2 This field defines error threshold which will trigger Recovery and Recalibration.
7:0	RW	4h	PGD	RECALB_THRESHOLD_GEN1 This field defines error threshold which will trigger Recovery and Recalibration.

Table 353. HOST_CTRL_USB3_LFPS_EXIT_REG

Address Offset: 30 - 33h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:28	RO	0	PGD	Reserved
27	RW	0	PGD	USB3_LFPS_EXIT_TX_AFTR_RX_U2_EN This will control the transmission of LFPS after detection of device driven LFPS for U2 exit. 0 - Disable 1 - Enable
26:22	RW	2d	PGD	USB3_LFPS_EXIT_TX_AFTR_RX_TIME This is a time in multiple of 4us, which XHCI will drive after detecting LFPS from the device. This is applicable to U3 and U2 exit.
21:16	RW	7d	PGD	USB3_U3_LFPS_RETRY_TIME This defines the time in multiple of 16ms, controller will retry for the U3 exit on a failed attempt. 0 corresponds to no wait time which will be equavilant to ~12us. For fastsim, this time is in multiple of 16us.
15:10	RW	31d	PGD	USB3_U1_LFPS_EXIT_FAIL This defines the time in multiple of 64us after which U2 LFPS exit will fail. For fastsim, this time is in microsecond
9:4	RW	24d	PGD	USB3_U2_LFPS_EXIT_FAIL This defines the time in multiple of 64us after which U2 LFPS exit will fail. For fastsim, this time is in microsecond
3:0	RW	10d	PGD	USB3_U3_LFPS_EXIT_FAIL This defines the time in ms after which U3 LFPS will fail and it will retry after USB3_U3_LFPS_RETRY_TIME. For fastsim, this time is in microsecond.

Table 354. HOST_CTRL_USB3_CP13_DEEMPH

Address Offset: 34 - 37h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:18	RO	0	PGD	Reserved
17:12	RW	000000	PGD	C+1 Precursor value for CP13
11:6	RW	011101	PGD	C0 value for CP13
5:0	RW	000011	PGD	C-1 Precursor value for CP13

Table 355. HOST_CTRL_USB3_CP14_DEEMPH

Address Offset: 38 - 3Bh
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:18	RO	0	PGD	Reserved
17:12	RW	000100	PGD	C+1 Precursor value for CP14
11:6	RW	011100	PGD	C0 value for CP14
5:0	RW	000000	PGD	C-1 Precursor value for CP14

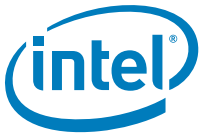


Table 356. HOST_CTRL_USB3_CP15_DEEMPH

Address Offset: 3C - 3Fh
Access: RW;
Size:32 bits
This register will be used as the default De-emphasis for Gen2 operation.

Bit	Access	Default Value	RST/PWR	Description
31:18	RO	0	PGD	Reserved
17:12	RW	000100	PGD	C+1 Precursor value for CP15
11:6	RW	011001	PGD	C0 value for CP15
5:0	RW	000011	PGD	C-1 Precursor value for CP15

Table 357. HOST_CTRL_USB3_CP16_DEEMPH

Address Offset: 40 - 43h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:18	RO	0	PGD	Reserved
17:12	RW	000000	PGD	C+1 Precursor value for CP16
11:6	RW	100000	PGD	C0 value for CP16
5:0	RW	000000	PGD	C-1 Precursor value for CP16

Table 358. HOST_CTRL_SSP_CONFIG_REG2

Address Offset: 44 - 47h
Access: RW;
Size: 32 bits

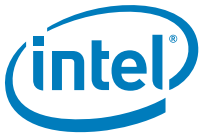
Bit	Access	Default Value	RST/PWR	Description
31:5	RW	0	PGD	Reserved
28	RW	0	PGD	D31IS_EOP_LCMD When set, it will disable the fix for LCMD EOP detection which is feeding into the HDR write enable for missing DPP.
27	RW	0	PGD	EN_REPEATER_TIMEOUTS When set, XHCI will use 10us for PENDING_HP_TIMER, PM_LC_TIMER and PM_ENTRY_TIMER.
26	RW	0	PGD	POLLTO_INACT_DIS When set, LTSSM would not go to inactive state after 3 Polling timeouts of 360 ms as defined by USB3.1 Spec.
25:21	RW	1h	PGD	USB3_UX_ENTRY_DELAY_GEN2 This defines the latency to drive the PHY to enter low power state and start looking for resume signal for Gen2 operation. The latency is multiple of 25.6ns. Register value of zero is illegal.
20:16	RW	1h	PGD	USB3_UX_ENTRY_DELAY_GEN1 This defines the latency to drive the PHY to enter low power state and start looking for resume signal for Gen1 operation. The latency is multiple` of 32ns. Register value of zero is illegal.
15	RW	0	PGD	DIS_LFPS_DET_UX_ENTRY When set, SS Port will wait for the powerdown to get completed before initiating the LFPS detection.

Bit	Access	Default Value	RST/PWR	Description
14:10	RW	3	PGD	USB3_U1U2_EXIT_DET_TIME_GEN2 The time for the Gated logic to detect LFPS based on rxelecidle for U2 and U1 exit. The total time will be multiple of 128ns for Gen2.
9:5	RW	3	PGD	USB3_U1U2_EXIT_DET_TIME_GEN1 The time for the Gated logic to detect LFPS based on rxelecidle for U2 and U1 exit. The total time will be multiple of 128ns for Gen1.
4	RW	0	PGD	SEC_RESET_DIS When set, SEC will not get reset on Hot/Warm Reset and LTSSM going into Polling.IDLE state
3	RW	0	PGD	LEC_RESET_DIS When set, LEC will not get reset on Hot/Warm Reset and LTSSM going into Polling.IDLE state
2	RW	0	PGD	SEC_ERR_CNT_U0 When set, Error count will only increment during U0. This is applicable to both Gen1 and Gen2.
1	RW	0	PGD	SSP_IDLE_ERR_RECAL_DIS When set, it will disable the IDLE symbol error detection feeding into recalibration decision for Gen2.
0	RW	0	PGD	SSP_IDLE_ERR_CNT_DIS When set, it will disable the increment of soft error count based on IDLE symbol Error for Gen2.

Table 359. HOST_CTRL_SSP_CONFIG_REG3

Address Offset: 48 - 4Bh
Access: RW;
Size: 32 bits

Bit	Access	Default Value	RST/PWR	Description
31:5	RW	0	PGD	Reserved
4:2	RW	001	PGD	BLOCKALIGN_TIMER_2 This defines the timer for LTSSM to wait in Polling.Active and Recovery.Active for additional time once BLOCLKALIGN_TIMER_1 expires 000: 0.2us (32 Gen2 port clock) 001: 0.5us (78 Gen2 port clock) 010: 0.75us (118 Gen2 port clock) 011: 1us (156 Gen2 port clock) 100: 2us (312 Gen2 port clock) 101: 3us (469 Gen2 port clock) 110: 4us (625 Gen2 port clock) 111: 6us (937 Gen2 port clock) This time should be programmed more than the time PHY would take to transition from Aligned to Locked state. This timer is only applicable if HOST_CTRL_SSP_LINK_REG2[9:8] is programmed to 01



Bit	Access	Default Value	RST/PWR	Description
1:0	RW	10	PGD	BLOCKALIGN_TIMER_1 This defines the timer for LTSSM to wait in Polling.Active and Recovery.Active for additional time to wait for TS1/TS2 from link partner 00: 32us 01: 64us 10: 128us 11: 256us This timer is only applicable if HOST_CTRL_SSP_LINK_REG2[9:8] is programmed to 01

Table 360. HOST_CTRL_USB3_ERR_COUNT

Address Offset: 64 - 67h
Port 1 …. N: 68h,6Ch,….(64h + (USB3_NPORT-1)*4h)
Access: RW;
Size: 32 bits
Up to a maximum of 16 USB3 Ports
This register will be saved as part of Context Save / Restore.

Bit	Access	Default Value	RST/PWR	Description
31:16	RO	0	PGD	Reserved
15:0	RW	RW1C	PGD	USB3_SOFT_ERR_CNT This register will keep count of soft errors on SS and SSP ports for a particular port. This register is read/write by software and it can be cleared by software by writing to it. Once reached to maximum value, it will stop incrementing.

Table 361. HOST_CTRL_USB3_DEBUG_REG1

Address Offset: C0 - C3h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
[31:USB3_PORTS]	RO	0	PGD	RESERVED
[USB3_PORTS-1:0]	RW	0	PGD	DEBUG_PORT_SEL One hot bit to enable a port for which Software / BIOS would update the HOST_CTRL_USB3_DEBUG_REG2 and HOST_CTRL_USB3_DEBUG_REG3. Once cleared for a port, port will consider BP and forces for that port anymore.

Table 362. HOST_CTRL_USB3_DEBUG_REG2

Address Offset: C4 - C7h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:26	RW	0	PGD	BP_RHUB_VAL

Bit	Access	Default Value	RST/PWR	Description
25:21	RW	0	PGD	BP_LFPS_CTRL_VAL
20:14	RW	0	PGD	BP_AUXPM_VAL
13:8	RW	0	PGD	BP_LTSSM_VAL
7	RW	0	PGD	BP_RHUB This bit is set by software / BIOS along with BP_RHUB_VAL and cleared by hardware when BP is hit.
6	RW	0	PGD	BP_LFPS_CTRL This bit is set by software / BIOS along with BP_LFPS_CTRL_VAL and cleared by hardware when BP is hit.
5	RW	0	PGD	BP_AUXPM This bit is set by software / BIOS along with BP_AUXPM_VAL and cleared by hardware when BP is hit.
4	RW	0	PGD	BP_LTSSM This bit is set by software / BIOS along with BP_LTSSM_VAL and cleared by hardware when BP is hit.
3	RW	0	PGD	NEXT_COMP_PATTERN Set by software to switch to next compliance pattern instead of waiting for the Ping.LFPS. This is self-clearing bit set by software and cleared by hardware when switching is complete.
2:1	RW	00	PGD	FORCE_RATE Once set, this will update the rate and pclkrate signals without rate change handshake through PIPE signals. 00 – Disabled 01 – Force Gen1 Rate 10 – Force Gen2 Rate 11 – N/A
0	RW	0	PGD	POLLING_TIMEOUT_DIS If set to '1', it disables various LTSSM timeouts during Polling states: - tPollingLFPSTimeout - tPollingSCDLFPSTimeout - tPollingLBPMLFPSTimeout - tPollingActiveTimeout - tPollingConfigurationTimeout - tPollingIdleTimeout

Table 363. HOST_CTRL_USB3_DEBUG_REG3

Address Offset: C8 - CBh
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31	RW	0	PGD	WAIT_RHUB Set and clear by software / BIOS to keep the state machine in the state once BP is hit.

Bit	Access	Default Value	RST/PWR	Description
30	RW	0	PGD	WAIT_LFPS_CTRL Set and clear by software / BIOS to keep the state machine in the state once BP is hit.
29	RW	0	PGD	WAIT_AUXPM Set and clear by software / BIOS to keep the state machine in the state once BP is hit.
28	RW	0	PGD	WAIT_LTTSM Set and clear by software / BIOS to keep the state machine in the state once BP is hit.
27:22	RW	0	PGD	FORCE_RHUB_VAL
21:17	RW	0	PGD	FORCE_LFPS_CTRL_VAL
16:0	RW	0	PGD	FORCE_AUXPM_VAL
9:4	RW	0	PGD	FORCE_LTSSM_VAL
3	RW	0	PGD	FORCE_RHUB This bit is set by software / BIOS along with FORCE_RHUB_VAL and cleared by hardware when transitions into new state
2	RW	0	PGD	FORCE_LFPS_CTRL This bit is set by software / BIOS along with FORCE_LFPS_CTRL_VAL and cleared by hardware when transitions into new state
1	RW	0	PGD	FORCE_AUXPM This bit is set by software / BIOS along with FORCE_AUXPM_VAL and cleared by hardware when transitions into new state
0	RW	0	PGD	FORCE_LTSSM This bit is set by software / BIOS along with FORCE_LTSSM_VAL and cleared by hardware when transitions into new state

4.4.4.14 VTIO Capability

All registers under this capability will be saved and restored.

Base Offset = 9000h

Table 364. VTIO Capability Register

Address Offset: 00h - 03h
Default Value:0000_00CBh
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:16	RO	0h	NA	Reserved
15:8	RW/L	06h	PGD	Next Capability Pointer
7:0	RW/L	203h	PGD	Capability ID

Table 365. VTIO BDF Assignment Register1

Address Offset: 04h - 07h
Default Value:0000_0000h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31	RW	0	AON	VTIO Disable 0 : Enable VTIO 1: Disable use of alternate BDF
30:9	RW	0	AON	Reserved
8	RW	0	AON	Port BW Context BDF Assignment 0: Normal 1: Alternate BDF The value of this bit needs to be the same as that of Device Context BDF Assignment
7	RW	0	AON	MSI BDF Assignment 0: Normal 1: Alternate BDF
6	RW	0	AON	Input Context BDF Assignment 0 : Normal 1 : Alternate BDF
5	RW	0	AON	Device Context BDF Assignment 0 : Normal 1 : Alternate BDF
4	RW	0	AON	Scratch Pad Buffers BDF Assignment 0 : Normal 1 : Alternate BDF
3	RW	0	AON	Scratch Pad Buffer Array BDF Assignment 0 : Normal 1 : Alternate BDF
2	RW	0	AON	Device Context Base Address Array BDF Assignment 0 : Normal 1 : Alternate BDF
1	RW	0	AON	Command Ring BDF Assignment 0 : Normal 1 : Alternate BDF
0	RW	0	AON	Event Ring Segment Table BDF Assignment 0 : Normal 1 : Alternate BDF

Table 366. VTIO BDF Assignment Register[2..9]

Address Offset: 08h - 27h
Default Value:0000_0000h
Access: RW for [MAX_SLOTS-1:0]; RO for [255:MAX_SLOTS]
Size:256 bits

Bit	Access	Default Value	RST/PWR	Description
255:0	RW [Based on MAX_SLOTS-1]	0x0	PGD	Per Slot BDF Allocation Registers Note: Max Device Slots Enabled (MAX_SLOTS) in XHC can be less than 255 (Max supported by XHCI Spec.) One bit for each Device Slot. Bit 0 : Reserved Bit 1 : Slot_ID 1 Bit 2 : Slot_ID 2 ... Bit 255 : Slot_ID 255 0 : Normal 1 : Alternate BDF

Table 367. VTIO BDF Assignment Register10

Address Offset: 28h
Default Value:0000_0000h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:0	RW	0x0	PGD	Per Event Ring BDF Allocation Registers One bit for each Event Ring Supported XHCI Spec allows up to 1024 interrupters/Event Rings. Based on the actual number supported by the controller, this register needs to scale. Bit 0: Primary Event Ring Bit 1: Event Ring 1 Bit 2: Event Ring 2 .... 0 : Normal 1 : Alternate BDF

Table 368. VTIO Policy Register

Address Offset: 2Ch
Default Value:0000_0000h
Access: RW
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:0	RW	0x0	PGD	Reserved - for future use

4.4.5 Host Controller Private Configuration Space

The private configuration space is a register space that lies outside the PCI configuration or Host MMIO address spaces. It is a HW private address space that is accessible only via the IOSF-SB channel.

Table 369. EXI Base Address Low (0Ch)

Address Offsets:0Ch – 0Fh
Default Value: TBD
Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:0	RO	0h	NA	TBD

Table 370. EXI Base Address High (10h)

Address Offsets:10h – 14h
Default Value: TBD
Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:0	RO	0h	NA	TBD

Table 371. Private - EP Type Lock Policy 1 (14h)

Address Offsets:14h – 17h
Default Value:00h
Access: RW/L; (this register can be written until the access control is set)
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:8	RO	0h	NA	Reserved
7	RW/L	0	Core	Interrupt IN EP Type: 0 – Interrupt IN EP is allowed 1 – Interrupt IN EP is not allowed
6	RW/L	0	Core	Bulk IN EP Type 0 – Bulk IN EP is allowed 1 – Bulk IN EP is not allowed
5	RW/L	0	Core	Isochronous IN EP Type 0 – Isoch IN EP is allowed 1 – Isoch IN EP is not allowed
4	RW/L	0	Core	Control EP Type 0 – Control EP is allowed 1 – Control IN EP is not allowed
3	RW/L	0	Core	Interrupt OUT EP Type 0 – Interrupt OUT EP is allowed 1 – Interrupt OUT EP is not allowed
2	RW/L	0	Core	Bulk OUT EP Type 0 – Bulk OUT EP is allowed 1 – Bulk OUT EP is not allowed
1	RW/L	0	Core	Isochronous OUT EP Type 0 – Isoch OUT EP is allowed 1 – Isoch OUT EP is not allowed
0	RW/L	0	Core	Policy 1 Enable When set, enables Policy #1 to be globally enabled.

Table 372. Private - EP Type Lock Policy 3 (1Ch)

Address Offsets:1Ch – 1Fh
Default Value:00h
Access: RW/L; (this register can be written until the access control is set)
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:8	RO	0h	NA	Reserved
7	RW/L	0	Core	Interrupt IN EP Type: 0 – Interrupt IN EP is allowed 1 – Interrupt IN EP is not allowed
6	RW/L	0	Core	Bulk IN EP Type 0 – Bulk IN EP is allowed 1 – Bulk IN EP is not allowed
5	RW/L	0	Core	Isochronous IN EP Type 0 – Isoch IN EP is allowed 1 – Isoch IN EP is not allowed
4	RW/L	0	Core	Control EP Type 0 – Control EP is allowed 1 – Control IN EP is not allowed
3	RW/L	0	Core	Interrupt OUT EP Type 0 – Interrupt OUT EP is allowed 1 – Interrupt OUT EP is not allowed
2	RW/L	0	Core	Bulk OUT EP Type 0 – Bulk OUT EP is allowed 1 – Bulk OUT EP is not allowed
1	RW/L	0	Core	Isochronous OUT EP Type 0 – Isoch OUT EP is allowed 1 – Isoch OUT EP is not allowed
0	RW/L	0	Core	Policy 3 Enable When set, enables Policy #1 to be globally enabled.

Table 373. Private - Port Lock Control – Port 1 … N (20…upto 11Ch)

Address Offsets:20h, 24h, … extend to Maxports count.
Default Value:00h
Access: RW/L; (this register can be written until the access control is set)
Size:32 bits
Repeat Maxports times
Addresses:
Port 1 = 020h,
Port 2 = 024h,
Port 3 = 028h …
Port (Maxports) = 020h+(Maxports - 1) * 4d = 11Ch
Maxports is no more than 64d
The following range is reserved for this requirement to support the max of 32 USB2 + 32 USB3 ports for a total of 64 ports (MAXPORTS).

Bit	Access	Default Value	RST/PWR	Description
31:8	RO	0h	NA	Reserved
7	RW/L	0	Core	Enable USB Lock Policy on root port number N: 00h - Port lock not enabled on port N 01h - Policy 1 enabled on port N 02h - Policy 2 enabled on port N 03h - policy 3 enabled on port N 4h to FFh - Reserved

Table 374. Private - DAP Common Control Register

Address Offsets:0x440h
Access: RO, RW;
Size:32 bits
Chassis Restore: S0iX (Regular)
Restore Group: VNNAON
All bits in this register must be in the Always ON Power domain (un-gated SUS or AON - as appropriate)

Bit	Access	Default Value	RST/PWR	Description
31:12	RO	0h	SUS	Reserved
11:0	RW	100h	SUS	HW ID Debounce Timer (HIDT): This field specifies the minimum amount of time that HW ID must stay stable before its value can be used. This field is in the unit of 32 RTC clocks. (Note RTC clock frequency is 32.768KHz) This defaults to 250 ms which equates to 8192 RTC clocks. This field is only used in micro-AB in HW ID mode.

Table 375. Private - DAP USB2 Device Over-Subscription Status Register

Address Offsets:0x458.
Access: RO, RW1C;
Size:32 bits
Records device over-subscription map spanning all USB2 links.
All bits in this register must be in the Always ON Power domain (un-gated SUS or AON - as appropriate)

Bit	Access	Default Value	RST/PWR	Description
31: USBX_USB2_PHY_PORTS	RO	0h	SUS	Reserved: Hardwired to 0
(USBX_USB2_PHY_PORTS-1):0	RW1C	0h	SUS	Device Over-subscribed (DO): For a USB2 link where device over-subscription has been detected, the corresponding bit in this register will be set to 1 by HW. This register will never be cleared by HW. E.g. A USB2 link detected with device over-subscription may go to DEVICE state or DISCONN state in response to relevant external trigger events, but the relevant bit will not be cleared by HW. SW writes 1 to a bit in this register to clear the bit. The register employs one-hot mapping to USB2 link number that is 0-based.

Table 376. Private - DAP eSS Device Over-Subscription Status Register

Address Offsets:0x468.
Access: RO, RW1C;
Size:32 bits
Records device over-subscription map spanning all eSS links.
All bits in this register must be in the Always ON Power domain (un-gated SUS or AON - as appropriate)

Bit	Access	Default Value	RST/PWR	Description
31: USBX_USB3_PHY_PORTS	RO	0h	SUS	Reserved: Hardwired to 0

Bit	Access	Default Value	RST/PWR	Description
(USBX_USB3_PHY_PORTS-1):0	RW1C	0h	SUS	Device Over-subscribed (DO): For a eSS link where device over-subscription has been detected, the corresponding bit in this register will be set to 1 by HW. This register will never be cleared by HW. E.g. A eSS link detected with device over-subscription may go to DEVICE state or DISCONN state in response to relevant external trigger events, but the relevant bit will not be cleared by HW. SW writes 1 to a bit in this register to clear the bit. The register employs one-hot mapping to eSS link number that is 0-based.

Table 377. Private - DAP USB2 Port <N> Control 0 Register

Address Offsets:0x500 + N * 0x10.
Access: RO, RW;
Size:32 bits
Chassis Restore: S0iX (Regular)
Restore Group: VNNAON
Control and status registers for all DRD USB2 links.
All bits in this register must be in the Always ON Power domain (un-gated SUS or AON - as appropriate)

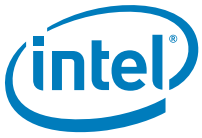
Bit	Access	Default Value	RST/PWR	Description
31:9	RO	0h	SUS	Reserved (RSVD): Hardwired to 0.
8	RW	0b	SUS	SW VBus (SV): SW sets this bit to 1 to inform xDCI of VBus presence. SW clears this bit to 0 to inform xDCI of VBus absence. VBus present in addition to link port in device state will arm the xDCI to communicate through USB interface.

Bit	Access	Default Value	RST/PWR	Description
7:5	RW	3'001b, soft-strap	SUS	Connector Event (CE): HW loads this field upon availability of connector type soft-strap. Value loaded depends on connector type as specified below: Type C:001. Type AB: 001. Type A:000. Type B:011. Express card: 000. SW programs this field to inform HW of the connector event associated with the link port. In connector type aware flow, this field is used in SW mode only. As such, this field applies to Type AB (SW mode) and Type C. This field does NOT apply to Type AB (HW mode), Type A, Type B or Express Card (Express Card behaves like Type A in a USB2 port). Recommended connector type aware programming based on valid use cases is described as follows: In Type AB (SW mode), SW should only program this field to either host subscription or device subscription. In Type C, SW may program this field to any defined value. In connector type agnostic flow (e.g. DnX), SW can program this field to inform HW of any valid connector event sequence regardless of associated connector type. One necessary condition to enable device subscription is that SW programs this field to 11. Additionally, SW VBus must be set to 1 as well before the xDCI is armed to communicate through USB interface. SW is required to poll the Operation State field in the corresponding Port Status register to ensure that HW act on the connector event. This is to help simplify synchronization from prim_clk to rtc_clk in scenario where HW receives new write before current write has been synchronized to rtc_clk domain. Encodings are defined as follows: 000: host subscription. 001: un-subscription. (HW default before connector type soft-strap takes effect) 010: guest subscription. 011: device subscription. 100: DBC subscription. Others: Reserved.
4:0	RO	0h	SUS	Reserved (RSVD): Hardwired to 0.

Note: There are USBX_USB2_PHY_PORTS of such 1DW registers with each register dedicated to one corresponding DRD USB2 link.

Table 378. Private - DAP USB2 Port <N> Control 1 Register

Address Offsets:0x504 + N * 0x10.
Access: RO, RW;
Size:32 bits



Chassis Restore: S0iX (Regular)
Restore Group: VNNAON
Control and status registers for all DRD USB2 links.
All bits in this register must be in the Always ON Power domain (un-gated SUS or AON - as appropriate)

Bit	Access	Default Value	RST/PWR	Description
31:11	RO	0h	SUS	Reserved (RSVD): Hardwired to 0.
10:8	RO	1h, soft-strap	SUS	Connector Type (CT): Specifies type of connector associated with this port. 000: Type C; 001: Type AB. (default) 010: Type A. 011: Type B. 100: Express card or M.2 Socket 2. Others: reserved. Default of this field maybe over-written by soft-strap. SW may program this field to make DAP HW operate in response to the programmed connector type that can be different from the actual physical connector type. One use case is to support BIOS-directed DnX flow via a physical Type A connector.
7:2	RO	0h	SUS	Reserved (RSVD): Hardwired to 0.
1	RW	HW_VBUS_EN_RST_VAL, soft-strap	SUS	HW VBus Enable (HVE): This field applies to Port 0 (0-based) only. HW default value is parameterized. HW loads this field upon availability of switch mode soft-strap. SW may program this field. If set to 1, HW VBus IO pin is used to directly control VBus indication to xDCI. If cleared to 0, SW VBus field is used to directly control VBus indication to xDCI. Any other port behaves as if this field were 0.
0	RW	HW_ID_EN_RST_VAL, soft-strap	SUS	HW ID Enable (HIE): This field applies to Port 0 (0-based) only. HW default value is parameterized. HW loads this field upon availability of switch mode soft-strap. SW may program this field. If set to 1, HW ID IO pin is used to directly control switch. If cleared to 0, connector event field is used to directly control switch. Please note Express Card USB2 port behaves like Type A USB2 port. Any other port behaves as if this field were 0.

Note: There are USBX_USB2_PHY_PORTS of such 1DW registers with each register dedicated to one corresponding DRD USB2 link

Table 379. Private - DAP USB2 Port <N> Status 0 Register

Address Offsets:0x508 + N * 0x10.
Access: RO;

Size:32 bits
Control and status registers for all DRD USB2 links.
All bits in this register must be in the Always ON Power domain (un-gated SUS or AON - as appropriate)

Bit	Access	Default Value	RST/PWR	Description
31:16	RO	0h	SUS	Reserved (RSVD): Hardwired to 0.
15	RO	0h	SUS	Hardware VBus (HV): Indicates live value of HW VBus signal. This bit only applies to Port 0 when configured as micro AB.
14	RO	1h	SUS	Hardware ID (HI): Indicates live value of HW ID signal. This bit only applies to Port 0 when configured as micro AB. Default value of 1 reflects the effect of a weak pullup installed in a platform in absence of any external attachment of a USB host or device. This bit is hardwired to 0 in any other port.
13:8	RO	0h	SUS	Reserved (RSVD): Hardwired to 0.
7:0	RO	10h	SUS	Operation State (OS): This field reflects live value of the DRD operation states with one-hot encodings stipulated as follows: 01h: host. 02h: disconnected. 04h: guest. 08h: device. 10h: PHY initialization. (default, dummy) 20h: EXI BSSB adapter connected. 40h: DBC. 80h: over-subscribed device. Due to clock crossing uncertainties, more than 1 bit may be set, or none at all, while states are transitioning. SW is expected to also accept EXI BSSB (20h) value, while transitioning into all other states (except for PHY Init and Reserved encodings), as the SW intended states maybe overriden by EXI HW. For e.g. if SW transitions CE into host, it should accept the values of 01h or 20h. USB2 PHY needs NOT be initialized. As such, the PHY initialization state carries no practical meaning herein.

Note: There are USBX_USB2_PHY_PORTS of such 1DW registers with each register dedicated to one corresponding DRD USB2 link

Table 380. Private - DAP eSS Port <N> Control 0 Register

Address Offsets:0x600 + N * 0x10.
Access: RO, RW;
Size:32 bits
Chassis Restore: S0iX (Regular)
Restore Group: VNNAON
Control and status registers for all DRD eSS links.
All bits in this register must be in the Always ON Power domain (un-gated SUS or AON - as appropriate)

Bit	Access	Default Value	RST/PWR	Description
31:17	RO	0h	SUS	Reserved (RSVD): Hardwired to 0.
16	RW	0h	SUS	Gen1 PCLK Request (G1PR): This field contributes to the support of Type C connector in a platform that includes FIA. In the flow that sequences MODPHY ownership from guest controller to either xHCI or xDCI, FIA requires GEN1 PCLK which may be provisioned through programming of this field. SW writes this field to 1 to un-gate GEN1 PCLK, or 0 to gate GEN1 PCLK.
15:9	RO	0h	SUS	Reserved (RSVD): Hardwired to 0.
8	RW	1'b0	SUS	SW VBus (SV): SW sets this bit to 1 to inform xDCI of VBus presence. SW clears this bit to 0 to inform xDCI of VBus absence. VBus present in addition to link port in device state will arm the xDCI to communicate through USB interface.
7:5	RW	3'b001, soft-strap	SUS	Connector Event (CE): Refer to the corresponding "DAP USB2 Port <N> Control 0 (0 <= N <= 31)" register field.
4:0	RO	0h	SUS	Reserved (RSVD): Hardwired to 0.

Note: There are USBX_USB3_PHY_PORTS of such 1DW registers with each register dedicated to one corresponding DRD eSS link.

Table 381. Private - DAP eSS Port <N> Control 1 Register

Address Offsets:0x604 + N * 0x10.
Access: RO, RW;
Size:32 bits
Chassis Restore: S0iX (Regular)
Restore Group: VNNAON
Control and status registers for all DRD eSS links.
All bits in this register must be in the Always ON Power domain (un-gated SUS or AON - as appropriate)

Bit	Access	Default Value	RST/PWR	Description
31:11	RO	0h	SUS	Reserved (RSVD): Hardwired to 0.
10:8	RO	1h, soft-strap	SUS	Connector Type (CT): Specifies type of connector associated with this port. HW loads this field upon availability of connector type soft-strap. SW can't program this field. 000: Type C; 001: Type AB. (HW default before connector type soft-strap takes effect) 010: Type A. 011: Type B. 100: Express card or M.2 Socket 2. Others: reserved. Default of this field maybe over-written by soft-strap.

Bit	Access	Default Value	RST/PWR	Description
7:5	RO	0h	SUS	Reserved (RSVD): Hardwired to 0.
4	RW	0h	SUS	Fast Rx Termination Switch Disable (FRTSD): This field enables propagation of xHCI Rx termination to MODPHY Rx termination upon detection of host subscription event instead of based on HOST operation state. This is to hide the switching latency in case the switching latency results in external super-speed capable USB device falling into USB2 mode. The fall into USB2 mode can happen when the external USB device fails to timely detect the USB host in super speed mode thanks to absence of USB host Rx termination within some USB specification constrained time limit. 0 - Enables propagation of xHCI Rx termination to MODPHY Rx termination upon detection of host subscription event, or xDCI Rx termination device subscription event. MODPHY Rx termination is driven to 0 otherwise. 1 - Enables propagation of xHCI Rx termination to MODPHY Rx termination based on HOST operation state. Enables propagation of xDCI Rx termination to MODPHY Rx termination when xDCI samples utmisrp_bvalid at 1. MODPHY Rx termination is driven to 0 otherwise.
3	RW	0b	SUS	Rx Termination Control Override (RTCO): This field specifies how MODPHY Rx termination is controlled in DISCONN state as defined in DAP operation states. 0: xHCI Rx termination is propagated to MODPHY Rx termination in DISCONN state. 1: Neither xHCI nor xDCI Rx termination is propagated to MODPHY Rx termination in DISCONN state. Instead, DAP HW disables MODPHY Rx termination in DISCONN state.
2	RO	0h	SUS	Reserved (RSVD): Hardwired to 0.
1	RW	HW_VBUS_EN_RST_VAL, soft-strap	SUS	HW VBus Enable (HVE): This field applies to Port 0 (0-based) only. HW default value is parameterized. HW loads this field upon availability of switch mode soft-strap. SW may program this field. If set to 1, HW VBus IO pin is used to directly control VBus indication to xDCI. If cleared to 0, SW VBus field is used to directly control VBus indication to xDCI. Any other port behaves as if this field were 0.

Bit	Access	Default Value	RST/PWR	Description
0	RW	HW_ID_EN_RST_VAL, soft-strap	SUS	HW ID Enable (HIE): This field applies to Port 0 (0-based) only. HW default value is parameterized. HW loads this field upon availability of switch mode soft-strap. SW may program this field. If set to 1, HW ID IO pin is used to directly control switch. If cleared to 0, connector event field is used to directly control switch except for Express Card in HW mode. Express Card may dynamically operate in HW mode if the relevant wire-based interface is active. Any other port behaves as if this field were 0.

Note: There are USBX_USB3_PHY_PORTS of such 1DW registers with each register dedicated to one corresponding DRD eSS link

Table 382. Private - DAP eSS Port <N> Status 0 Register

Address Offsets:0x608 + N * 0x10.
Access: RO;
Size:32 bits
Control and status registers for all DRD eSS links.
All bits in this register must be in the Always ON Power domain (un-gated SUS or AON - as appropriate)

Bit	Access	Default Value	RST/PWR	Description
31:16	RO	0h	SUS	Reserved (RSVD): Hardwired to 0.
15	RO	0h	SUS	Hardware VBus (HV): Indicates live value of HW VBus signal. This bit only applies to Port 0 when configured as micro AB.
14	RO	1h	SUS	Hardware ID (HI): Indicates live value of HW ID signal. This bit only applies to Port 0 when configured as micro AB. Default value of 1 reflects the effect of a weak pullup installed in a platform in absence of any external attachment of a USB host or device. This bit is hardwired to 0 in any other port.
13:8	RO	0h	SUS	Reserved (RSVD): Hardwired to 0.
7:0	RO	10h	SUS	Operation State (OS): Refer to the corresponding "DAP USB2 Port <N> Status 0 (0 <= N <= 31)" register field.

Note: There are USBX_USB3_PHY_PORTS of such 1DW registers with each register dedicated to one corresponding DRD eSS link

4.4.6 DbC Private Memory Mapped Address Space Registers

The DbC interfaces that support the EXI transport function use addresses in the Host Address space that are set hard coded and set aside for it by BIOS. This address range does not fall within the MEMBAR of the XHCI host controller and is not affected by the value of the MSE in the XHCI functions PCI config space.

4.4.6.1 Base Address (DbCPrivateMemBase)

The base address for the DbC private memory mapped space is hardcoded as an integration parameter provided by the SOC.

Table 383. DbC GP2 OUT Payload Pointer (low)
Address Offset: 00h

Bit	Access	Default Value	RST/PWR	Description
31:0	RW	00h	Core	Lower DW of payload address pointer

Table 384. DbC GP2 OUT Payload Pointer (high)
Address Offset: 04h

Bit	Access	Default Value	RST/PWR	Description
31:0	RW	00h	Core	Upper DW of payload address pointer

Table 385. DbC GP2 OUT Payload Qualifiers
Address Offset: 08h

Bit	Access	Default Value	RST/PWR	Description
31:16	RW	00h	Core	Reserved
15:8	RW	00h	Core	Destination ID
7:4	RO	0h	Core	Reserved
3:0	RW	0h	Core	Root Space

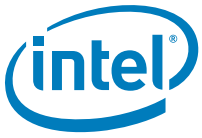
Table 386. DbC GP2 OUT Payload Transfer Length
Address Offset: 0Ch

Bit	Access	Default Value	RST/PWR	Description
31	RW	0b	Core	Data Valid This bit indicates the presence of a valid data buffer and is the "doorbell" that allows the DbC to initiate a DMA transaction. This bit is cleared by HW upon completion of the DMA upto either the specific transfer length, or the host controller sending a short packet.
30:00	RW	00h	Core	Payload Transfer Length Length of the payload buffer in bytes. This is a '1' based count.

Table 387. DbC GP2 OUT Status Pointer (low)
Address Offset: 10h

Bit	Access	Default Value	RST/PWR	Description
31:0	RW	00h	Core	Lower DW of Status address pointer

Table 388. DbC GP2 OUT Status Pointer (high)



Address Offset: 14h

Bit	Access	Default Value	RST/PWR	Description
31:0	RW	00h	Core	Upper DW of Status address pointer

Table 389. DbC GP2 OUT Status Qualifiers

Address Offset: 18h

Bit	Access	Default Value	RST/PWR	Description
31:16	RW	00h	Core	Reserved
15:8	RW	00h	Core	Destination ID
7:4	RO	0h	Core	Reserved
3:0	RW	0h	Core	Root Space

Table 390. DbC GP2 IN Payload Pointer (low)

Address Offset: 1Ch

Bit	Access	Default Value	RST/PWR	Description
31:0	RW	00h	Core	Lower DW of payload address pointer

Table 391. DbC GP2 IN Payload Pointer (high)

Address Offset: 20h

Bit	Access	Default Value	RST/PWR	Description
31:0	RW	00h	Core	Upper DW of payload address pointer

Table 392. DbC GP2 IN Payload Qualifiers

Address Offset: 24h

Bit	Access	Default Value	RST/PWR	Description
31:16	RW	00h	Core	Reserved
15:8	RW	00h	Core	Destination ID
7:4	RO	0h	Core	Reserved
3:0	RW	0h	Core	Root Space

Table 393. DbC GP2 IN Payload Transfer Length

Address Offset: 28h

Bit	Access	Default Value	RST/PWR	Description
31	RW	0b	Core	Data Valid This bit indicates the presence of a valid data buffer and is the “doorbell” that allows the DbC to initiate a DMA transaction. This bit is cleared by HW upon completion of the DMA up to the specific transfer length.
30:00	RW	00h	Core	Payload Transfer Length Length of the payload buffer in bytes. This is a ‘1’ based count.

Table 394. DbC GP2 IN Status Pointer (low)

Address Offset: 2Ch

Bit	Access	Default Value	RST/PWR	Description
31:0	RW	00h	Core	Lower DW of Status address pointer

Table 395. DbC GP2 IN Status Pointer (high)

Address Offset: 30h

Bit	Access	Default Value	RST/PWR	Description
31:0	RW	00h	Core	Upper DW of Status address pointer

Table 396. DbC GP2 IN Status Address Qualifiers

Address Offset: 34h

Bit	Access	Default Value	RST/PWR	Description
31:16	RW	00h	Core	Reserved
15:8	RW	00h	Core	Destination ID
7:4	RO	0h	Core	Reserved
3:0	RW	0h	Core	Root Space

Table 397. DbC DFX OUT Control

Address Offset: 38h

Bit	Access	Default Value	RST/PWR	Description
31:04	RO	00h	Core	Reserved
3:0	RW	00h	Core	Available Credits THe EXI Bridge writes the absolute value of the available credit count into this register field each time it drains an entry from its buffers. Each credit represents a 64 byte EXI packet.

Table 398. DbC DFX IN Payload Pointer (low)

Address Offset: 3Ch

Bit	Access	Default Value	RST/PWR	Description
31:0	RW	00h	Core	Lower DW of payload address pointer

Table 399. DbC DFX IN Payload Pointer (high)

Address Offset: 40h

Bit	Access	Default Value	RST/PWR	Description
31:0	RW	00h	Core	Upper DW of payload address pointer

Note: Qualifiers are not needed for the DFX IN interface, since the qualifiers will be identical to those used for the DFx OUT interface, which are hardcoded.

Table 400. DbC DFX IN Payload Transfer Length

Address Offset: 44h

Bit	Access	Default Value	RST/PWR	Description
31	RW	0b	Core	Data Valid This bit indicates the presence of a valid data buffer and is the "doorbell" that allows the DbC to initiate a DMA transaction. This bit is cleared by HW upon completion of the DMA up to the specific transfer length.
30:00	RW	00h	Core	Payload Transfer Length Length of the payload buffer in bytes. This is a '1' based count.

Table 401. DbC DFX IN Status Pointer (low)

Address Offset: 48h

Bit	Access	Default Value	RST/PWR	Description
31:0	RW	00h	Core	Lower DW of Status address pointer

Table 402. DbC DFX IN Status Pointer (high)

Address Offset: 4Ch

Bit	Access	Default Value	RST/PWR	Description
31:0	RW	00h	Core	Upper DW of Status address pointer

Table 403. DbC TRACE IN Payload Base Pointer (low)

Address Offset: 50h

Bit	Access	Default Value	RST/PWR	Description
31:0	RW	00h	Core	Lower DW of payload base pointer

Table 404. DbC TRACE IN Payload Base Pointer (high)

Address Offset: 54h

Bit	Access	Default Value	RST/PWR	Description
31:0	RW	00h	Core	Upper DW of payload base pointer

Table 405. DbC TRACE IN Payload Qualifiers

Address Offset: 58h

Bit	Access	Default Value	RST/PWR	Description
31:16	RW	00h	Core	Reserved
15:8	RW	00h	Core	Destination ID
7:4	RO	0h	Core	Reserved
3:0	RW	0h	Core	Root Space

Table 406. DbC TRACE IN Transfer Doorbell

Address Offset: 5Ch

Bit	Access	Default Value	RST/PWR	Description
31:19	RW	00h	Core	Reserved
18:11	RW	00h	Core	Payload Offset The Offset in multiples of 1024B from the base pointer – from which to transfer the payload referenced by this doorbell.
10:0	RW	00h	Core	Length of Transfer Payload The Trace Handler writes the length of the payload in the "entry" referenced by this doorbell.The length has an allowed maximum of 1024B

Table 407. DbC TRACE IN Status Pointer (low)

Address Offset: 60h

Bit	Access	Default Value	RST/PWR	Description
31:0	RW	00h	Core	Lower DW of Status address pointer

Table 408. DbC TRACE IN Status Pointer (high)

Address Offset: 64h

Bit	Access	Default Value	RST/PWR	Description
31:0	RW	00h	Core	Upper DW of Status address pointer

Table 409. DbC TRACE IN Status Address Qualifiers

Address Offset: 68h

Bit	Access	Default Value	RST/PWR	Description
31:16	RW	00h	Core	Reserved
15:8	RW	00h	Core	Destination ID
7:4	RO	0h	Core	Reserved
3:0	RW	0h	Core	Root Space

Table 410. DbC Error Control and Status Registers

Address Offset: 6Ch

Bit	Access	Default Value	RST/PWR	Description
31:9	RO	00h	Core	Reserved
8	RW	0h	Core	DbC.Trace.IN
7	RW	0h	Core	DbC.DFx.OUT
6	RW	0h	Core	DbC.DFx.IN
5	RW	0h	Core	DbC.GP2.OUT
4	RW	0h	Core	DbC.GP2.IN
3	RW	0h	Core	DbC.GP1.OUT
2	RW	0h	Core	DbC.GP1.IN
1	RW	0h	Core	Control EP
0	RW	0h	Core	Enable error logging

Table 411. DBC EXI Control and Status Register

Address Offset: 70h

Bit	Access	Default Value	RST/PWR	Description
31	RO	0	Core	DbC.GP2.IN.StatusLog Set when the DMA transfer request status for GP2 IN is completed. Cleared when a new DMA transfer request is received.
30	RO	0	Core	DbC.GP2.OUT.StatusLog Set when the DMA transfer request status for GP2 OUT is completed. Cleared when a new DMA transfer request is received.
29:13	RO	0x0	Core	Reserved
12	RW	0	Core	DbC-ExI Clock Gating Control Disable gating for prim_clk for DbC-ExI logic. By default clock gating is enabled.
11	RW	0	Core	DbC SAICheckPolicy 1: Disable SAI checking on read requests 0: Enable Default SAI check (on Reads & Writes)
10	RW	0	Core	TraceSequencerPipelineDisable Set to disable pipelining of read requests to fabric for different trace transfer requests. By default, trace sequencer would start issuing reads requests to Fabric for a subsequent transfer request while the reads for the previous one hasn't been returned back to DbC 0: Read Pipelining enabled for Trace 1: Disable read pipelining for Trace
9:7	RW	0x0	Core	DbC.MaxPacketSize Configurable MPS for Trace, DFx, GP2 EPs Default = 1KB 000 : 1KB 001 : 64B 010 : 128B 011 : 256B 100 : 512B Others : Reserved

Bit	Access	Default Value	RST/PWR	Description
6:1	RW	0x0	Core	DbC.NumPendingReads Constrain number of read requests pending on Fabric on behalf of DbC Eps. Sequencers limit the number of read requests that will be initiated on Fabric at any given time to NUM_PENDING_READ. NUM_PENDING_READ = [1..READS_PER_MPS] Where READS_PER_MPS is the number of read requests require for 1 MPS for the given EP. Applies for DbC.[Trace|DFx|GP2] IN EPs
0	RW	0	Core	DbC.Trace.PipelineDepth1 Constrain DbC.Trace IN Pipeine to 1 deep. Limit processing of DbC Trace to one transfer at any time. In other wordsUntil Trace data for the first transfer request from NPKH is completed on USB3 interface and status returned back to NPKH, subsequent transfer request is not started, only 1 Trace sequencer is active at any given time.

Table 412. DBC Arbiter Grant Counts

Address Offset: 74h

Bit	Access	Default Value	RST/PWR	Description
31:30	RW	0x0	Core	Reserved
29:27	RW	0x1	Core	Port IN Arbiter Grant Count
26:24	RW	0x1	Core	GP2 IN Port Arbiter Grant Count
23:21	RW	0x1	Core	DFX IN Port Arbiter Grant Count
20:18	RW	0x1	Core	Trace IN Port Arbiter Grant Count
17:15	RW	0x1	Core	Upstream Fabric Read Request Hysteresis Value (Number of clocks)
14:12	RW	0x1	Core	Upstream Fabric DBC(DD) Request Grant Count
11:9	RW	0x1	Core	Upstream Fabric DBC-EXI Request Grant Count
8:6	RW	0x1	Core	Upstream Fabric GP2 Request Grant Count
5:3	RW	0x1	Core	Upstream Fabric DFx Request Grant Count
2:0	RW	0x1	Core	Upstream Fabric Trace Request Grant Count

Table 413. DBC ECO Policy Register1

Address Offset: 78h

Bit	Access	Default Value	RST/PWR	Description
31:24	RW	00h	Core	Reserved
23	RW	0x0	Core	Short Packet Enable for GP2 IN Endpoint
22	RW	0x0	Core	Short Packet Enable for DFx IN Endpoint
21	RW	0x0	Core	Short Packet Enable for Trace IN Endpoint
20:18	RW	0x0	Core	Port Arbitration Grant Count
17	RW	0x0	Core	Reserved for future use

Bit	Access	Default Value	RST/PWR	Description
16	RW	0x0	Core	OUT EP Burst Size Select Default: HW selects the burst size for OUT EPs based on the mode of operation Kernel Debug Mode Only: Supported OUT EP = 1 (GP1) ; Burst Size = 4 Platform Debug Mode Only: Supported OUT EPs = 2 (DFx, GP2), Burst Size = 2 Kernel and Platform debug mode: Supported OUT EPs = 3 (GP1, DFx, GP2) ; Burst Size = 1 When Set to 1, Burst Size = 1
15	RW	0x0	Core	IGNORE EXI_EN
14	RW	0x0	Core	IGNORE DCE
13	RW	0x0	Core	DBC-EXI HCRESET DISABLE When set to '1', DBC/DBC-EXI will not take any action on HCReset. Default behavior is to trigger HCReset flow.
12	RW	0x0	Core	DBC Allow PG When set to '1', DBC/DBC-EXI will allow PG under HW initiated low power modes (D0ix). This could be used in a flow where XHC is allowed to enter low power modes, while debug data will subsequently transported to debug host after re-entry into S0/D0
11:8	RW	0x0	Core	HC Reset/WPR Handling: Timeout Values 0000 : 0 us (trigger exit right away) 0001 : 250 us 0010 : 500 us 1111 : 3.75 ms
7	RW	0x0	Core	Timeout based HC Reset/WPR Handling When set, enable timer based mechanism to allow HCReset and Warm Port Reset to override any "hung" situation due to any flows not completing as expected. Use HC Reset/WPR Handling Timeout values for forcing HCReset/ WPR flows
6	RW	0x0	Core	Reserved - for future use
5	RW	0x0	Core	Internal DBC-EXI Enable "Internal DBC ExI Enable "

Bit	Access	Default Value	RST/PWR	Description
4	RW	0x0	Core	ExI Enable Override Enable When this bit is set, the "Internal DBC ExI Enable " takes priority over the external "ExI Enable" signal received from EXI Bridge IP Default behavior is to use "exio_scr_ectrl_eavails input from ExI Bridge
3	RW	0x0	Core	Trace Status Address When this bit is set, the address for Status Write request will include the address offset. Default address for Trace Status is the base address of the trace request
2	RW	0x0	Core	Enable Non-Transfer Status Enables generation of a status write on each of the interfaces with status indicating the cause of an exception flow trigger condition Default behavior is for the sequencer to return a status completion (for transfer success, or exception scenarios) only when a pending/active DMA is in progress
1	RW	0x0	Core	Enable DBC-ExI on Credit Init Completion Setting this bit will enforce "Credit Init" completion as necessary condition to allow transfers on all 3 interfaces (Trace, GP2, DFx). Default behavior requires successful "Credit Init" completion as necessary condition only to allow DFX OUT EP transfer and not affect other interfaces (Trace, GP2)
0	RW	0x0	Core	Credit Init Trigger Writing a '1' to this bit will trigger "Credit Init" request. A Credit Init request will be initiated irrespective of the status of the last Credit Init request initiated.

Table 414. DBC ECO Policy Register2

Address Offset: 7Ch

Bit	Access	Default Value	RST/PWR	Description
31:6	RO	00h	Core	Reserved
5	RO	0x0	Core	DBC_EXI_RUN Internal version of RUN. Set only when DBC_EXI is enabled and link up as upstream port was due to DBC_EXI =1
4	RO	0x0	Core	DBC RUN Internal version of RUN bit. Set only when DBC(DD) is enabled and link up as upstream port was due to DCE=1

Bit	Access	Default Value	RST/PWR	Description
3	RO	0x0	Core	DBC_EXI_EN Internal version of EXI_EN
2	RO	0x0	Core	DBC_EN Internal version of DBC_EN tracked by HW
1:0	RO	0x0	Core	Credit Init Status Tracks the status of Credit Init Handshake. HW updates this register. o "00" : Credit Init not yet requested o "01" : Credit Init Pending: request sent to ExI Bridge - Not received "Init Credit" value from ExI Bridge o "10" : Credit Init Done : Received "Init Credit" value from ExI Bridge o "11" : Reserved

Table 415. DBC ECO Policy Register3

Address Offset: 80h

Bit	Access	Default Value	RST/PWR	Description
31:0	RW	00h	Core	Reserved for future use

Table 416. DBC ECO Policy Register4

Address Offset: 84h

Bit	Access	Default Value	RST/PWR	Description
31:0	RW	00h	Core	Reserved for future use

Table 417. DBC EXI DCPORTSC Shadow Register

Address Offset: 88h

Bit	Access	Default Value	RST/PWR	Description
31:0	RW	00h	Core	DCPORTSC Shadow register

Table 418. DBC GP2 OUT DMA Status Register1

Address Offset: 8Ch

Bit	Access	Default Value	RST/PWR	Description
31:5	RW	00h	Core	Reserved
4	RW	0x0	Core	GP2 OUT DMA Status Valid When set, indicates GP2 OUT DMA Status is valid This bit is set by DBC HW when a GP2 OUT transfer completes. The bit is cleared when a new GP2 OUT DMA transfer is initiated.

Bit	Access	Default Value	RST/PWR	Description
3:0	RW	0x0	Core	Status of GP2 OUT DMA transfer 0000: Transfer Success 0001: Host initiated Device Reset 0010: HC Reset 0011: Disconnected 0100: Deconfigured 0101: Endpoint Halt 0110: System Error (from fabric) 0111: Request Error Others Reserved

Table 419. DBC GP2 OUT DMA Status Register2

Address Offset: 90h

Bit	Access	Default Value	RST/PWR	Description
31	RW	00h	Core	Reserved
30:0	RW	0x0	Core	Data Length (in Bytes) This field is written by DbC GP2 OUT transfer completed (when successful) or terminated (exceptions/errors). Length would be 1's based . 0x0: 0 Bytes 0x1: 1 Byte 0x2: 2 Bytes … … This field is valid when "GP2 OUT DMA Status Valid" bit is set

Table 420. DBC GP2 IN DMA Status Register1

Address Offset: 94h

Bit	Access	Default Value	RST/PWR	Description
31:5	RW	00h	Core	Reserved
4	RW	0x0	Core	GP2 IN DMA Status Valid When set, indicates GP2 IN DMA Status is valid This bit is set by DBC HW when a GP2 IN transfer completes. The bit is cleared when a new GP2 IN DMA transfer is initiated.
3:0	RW	0x0	Core	Status of GP2 OUT DMA transfer 0000: Transfer Success 0001: Host initiated Device Reset 0010: HC Reset 0011: Disconnected 0100: Deconfigured 0101: Endpoint Halt 0110: System Error (from fabric) 0111: Request Error Others Reserved

Table 421. DBC GP2 IN DMA Status Register2

Address Offset: 98h

Bit	Access	Default Value	RST/PWR	Description
31	RO	00h	Core	Reserved
30:0	RW	0x0	Core	Data Length (in Bytes) This field is written by DbC GP2 IN transfer completed (when successful) or terminated (exceptions/errors). Length would be 1's based . 0x0: 0 Bytes 0x1: 1 Byte 0x2: 2 Bytes … … This field is valid when "GP2 IN DMA Status Valid" bit is set

Table 422. DBC USB2 Protocol Timers1 (USB2PROTMR1)

Address Offset: 0xA0h

Bit	Access	Default Value	RST/PWR	Description
31:20	RW	12'd100	AON	TWTRSTFS: Time a high-speed capable device operating in non-suspended fullspeed must wait after start of SE0 before beginning the high-speed detection handshake. Legal range: > 2.5 µs; < 3000 µs Default: 100 µs Unit: 1 µs
19:7	RW	13'd3000	AON	TUCH/TUCHEND: Minimum duration of a Chirp K from a high-speed capable device within the reset protocol Legal range: > 1 ms; < 7 ms Default: 3 ms Unit: 1 µs
6:0	RW	7'd10	AON	TWFBK: Delay before detecting Chirp K from Host after Device Chirp K is driven. Legal range: Any Default:10 µs Unit: 1 µs

Table 423. DBC USB2 Protocol Timers2 (USB2PROTMR2)

Address Offset: 0xA4h

Bit	Access	Default Value	RST/PWR	Description
31:20	RW	12'd2400	SUS	TWTFS: Time after end of upstream chirp at which device reverts to fullspeed default state if no downstream chirp is detected. Legal range: > 1ms; < 2.5 ms Default: 2.4 ms Unit: 1 µs

Bit	Access	Default Value	RST/PWR	Description
19:8	RW	12'd3060	SUS	TWTREV: Time a high-speed capable device operating in high-speed must wait after start of SE0 before reverting to full-speed Legal range: > 3 ms; < 3.125 ms Default: 3.060 ms Unit: 1 µs
7:0	RW	8'd70	SUS	TCLKSUS: Time to allow PHY to power up when exiting a suspended state. Legal range: Any Default: 70 µs Unit: 1 µs

Table 424. DBC USB2 Protocol Timers3 (USB2PROTMR3)

Address Offset: 0xA8h

Bit	Access	Default Value	RST/PWR	Description
31:24	RW	3	SUS	TDEG: Linestate[1:0] deglitch value. Legal range: > 2.5 µs Default: 3 µs Unit: 1 µs
23	RW	0	SUS	Reserved
22:13	RW	10'd500	SUS	TWTRSTHS: Time a device must wait after reverting to full-speed before sampling the bus state for SE0 and beginning the high-speed detection handshake Legal range: > 100 µs; < 875 µs Default: 500 µs Unit: 1 µs
12:0	RW	13'd3000	SUS	TSUSPEND: Time a device must be suspended after seeing a constant Idle state Legal range: 3 ms Default: 3 ms Unit: 1 µs

Table 425. DBC USB2 Protocol Timers4 (USB2PROTMR4)

Address Offset: 0xACh

Bit	Access	Default Value	RST/PWR	Description
31:20	RW	0	SUS	Reserved
19:16	RW	4'd9	SUS	TL1TOKENRETRY: Device delay before transitioning to L1 after transmitting ACK. Legal range: > 8 µs; < 10 µs Default: 9 µs Unit: 1 µs

Bit	Access	Default Value	RST/PWR	Description
15:8	RW	8'd60	SUS	TL1RESIDENCY: L1 residency. Legal range: > 50 µs Default : 60 µs Unit: 1 µs
7:0	RW	8'd50	SUS	TL1DEVDRVRESUME: Device initiated L1 Exit resume duration Legal range: 50 µs Default: 50 µs Unit: 1 µs

Table 426. DBC USB2 Protocol Timers5 (USB2PROTMR5)

Address Offset: 0xB0h

Bit	Access	Default Value	RST/PWR	Description
31:24	RW	0	SUS	Reserved
23:20	RW	4'd5	SUS	THSIPDOD: Inter-packet Delay (for highspeed) for packets traveling in opposite direction Legal range: > 8; < 192 HS bit time (> 16.667 ns) Default: 83.335 ns Unit: 16.667 ns
19:16	RW	4'd11	SUS	TIPD: Inter-packet Delay (for low-/fullspeed) Legal range: > 2 FS bit time (166.667 ns) Default: 183.337 ns Unit: 16.667 ns
15:8	RW	8'd97	SUS	TBTOHS: HS Bus Timeout Legal range: > 736; < 816 HS bit time Default: 1.625 µs (780 HS bit time) Unit: 16.667 ns
7:0	RW	8'd85	SUS	TBTOFS: FS Bus Timeout Legal range: > 16; < 18 FS bit time Default: 1.417 µs (17 FS bit time) Unit: 16.667 ns

Table 427. DBC USB2 Misc Control (USB2MISCCTRL)

Address Offset: 0xB4h

Bit	Access	Default Value	RST/PWR	Description
31:5	RW	0	SUS	Reserved

Bit	Access	Default Value	RST/PWR	Description
6	RW	0	SUS	DBC Engine Reset Select (DBCERSTSEL): 1: When set, selects the xHCI based reset (HCRST). 0: When cleared, selects IOSF Primary reset (prim_rst_b). It is expected that this bit is set only in S0 to avoid a spurious reset assertion. Note:This bit is the highest priority select line. Setting this bit allows DBC Engine to be reset along with the xHCI when HCRST is set.
5	RW	0	SUS	Aux_clk Dynamic Clock Gate Enable (AUXCLKDCGEN): 1: When set, allows DCG on aux_clk 0: When cleared, disallows DCG on aux_clk Clearing this bit will also disable aux_clk trunk gate
4	RW	0	SUS	USB2 LPM Capability (USB2LPMCAP): 1: When set, the USB2.0 Extension (part of the BOS descriptor) LPM Capability bit will be set. 0: When cleared, the LPM Capability bit will be cleared. LPM is not a supported capability, bit is here for testing purposes only.
3	RW	0	SUS	Force FS Mode (FFSM): 1: When set, USB2 Port is forced to operate at FS only mode. 0: When cleared, USB2 Port can operate in both HS or FS mode. USB2 DBC Device's CHIRP K will be simply suppressed to achieve FS only mode during port reset.
2	RW	0	SUS	Force USB2 PHY SuspendM (FUSB2PHYSUSM): 1: When set, USB2 PHY's suspendm signal is de-asserted (1'b1) 0: When cleared, USB2 PHY's suspendm signal depends on the USB2 Port SM
1	RW	0	SUS	Force USB2 PHY Reset (FUSB2PHYRST): 1: When set, USB2 PHY's UTMI Reset will be asserted. 0: When cleared, USB2 PHY's UTMI Reset will be based upon power on reset. SW will time the USB2 PHY's reset and clear this bit accordingly.
0	RW	0	SUS	Fast Simulation Mode (FASTSIM): 1: Related timers will be scaled by 100x faster 0: Related timers will be according to specification defined values.

Table 428. DBC USB2 Link Error Counter (USB2LNERRCNT)

Address Offset: 0xB8h

Bit	Access	Default Value	RST/PWR	Description
31:24	RW1C	0	SUS	Rx Error Error Count (RXERRCNT): Increments each time an error of this type is seen by the USB2 port. Counter does not over-flow and is held at 8'hFF if error exceeds counter. SW writes 8'hFF to clear this field.

Bit	Access	Default Value	RST/PWR	Description
23:16	RW1C	0	SUS	Timeout Error Count (TOUTERRCNT): Increments each time an error of this type is seen by the USB2 port. Counter does not over-flow and is held at 8'hFF if error exceeds counter. SW writes 8'hFF to clear this field.
15:8	RW1C	0	SUS	PID Error Count (PIDERRCNT): Increments each time an error of this type is seen by the USB2 port. Counter does not over-flow and is held at 8'hFF if error exceeds counter. SW writes 8'hFF to clear this field.
7:0	RW1C	0	SUS	CRC16/5 Error Count (CRCERRCNT): Increments each time an error of this type is seen by the USB2 port. Counter does not over-flow and is held at 8'hFF if error exceeds counter. SW writes 8'hFF to clear this field.

Table 429. DBC EXI DEBUG SW CNTRL AND STATUS OFS

Address Offset: 100h

Bit	Access	Default Value	RST/PWR	Description
31:8	RO	00h	Core	Reserved
7	RW	0x0	Core	Fast SW Timeout Mode 1 : Enable Fast Timeout Simulation Mode. When set, timeout values used for "SW response Timeout" mode will be in micro-seconds. 0 : Normal mode. Timeout values are as defined by "SW response Timeout" register.
6	RW1C	0x0	Core	SW Timeout Status 1: Set by HW when Timeout occurred and HW disabled SW Handling 0: Timeout not triggered Set by HW, Cleared by SW. Timeout will also clear "Debug SW Available" bit.
5:2	RW	0x0	Core	SW response Timeout 0000 : 1 ms 0001: 20 ms 0010: 40 ms 0011: 60 ms 0100: 80 ms 0101: 100 ms 0110: 200ms … 1111: 1100ms
1	RW	0x0	Core	SW Response Timeout Enable: 1: HW will timeout and trigger STALL response if SW did not respond within "SW Timeout" period 0: Timeout is not triggered.

Bit	Access	Default Value	RST/PWR	Description
0	RW	0x0	Core	Debug SW Available: 1: Debug SW has been loaded and is available 0: Debug SW is not available When Debug SW is available, then HW presents the Control Transfer requests to SW and relies on SW to handle the requests.

Table 430. DBC_EXI_DEBUG_REQUEST_INFO_AND_STATUS_OFS

Address Offset: 104h

Bit	Access	Default Value	RST/PWR	Description
31	RW	00h	Core	Response Packet Last: Specifies that this response packet is the last packet for satisfying the current request or if there is additional packets to complete the request. 1 : Current response packet is the last data packet for the current request 0: Current response packet is not the last data packet for the current request. There is one or more additional data packets required to complete the request. For example, If the response data buffer is 512B, and the response is > 512B, then there will be multiple response data packets required, and this bit is set to '0' except for the last one.
30:27	RW	0x0	Core	Response Type: Specifies the type of response that needs to be generated 000 : DATA Response 001: ACK 010: STALL (Request not supported) Others: Reserved For DATA response, associate DATA is written into the "Response Stack" by SW.
26	RW1S	0x0	Core	Debug Response Avail: 1: Valid SW response available for HW 0: No response available SW sets this bit when it has generated a response for a debug request received. HW clears this bit after the response has been consumed (completed the transfer to host).
25:16	RO	0x0	Core	Reserved

Bit	Access	Default Value	RST/PWR	Description
15	RW	0x0	Core	IN Flow Control Detected HW sets this bit to indicate to Debug SW that a Flow Control condition was detected for an IN Transfer and SW needs to switch to mode where SW responds to current request (and not forward looking). This field is valid only when a debug request is pending. The scenario would be when an IN request - ACK TP (Seq#N, NumP=1) was received and the prior Control Transfer request from debug host was ACK TP (Seq#N, NumP=0)
14:12	RW	0x0	Core	Debug Request Error Type Indicates that cause/Type of the error detect. Valid only when "Debug Request Error Detected" bit is '1' Encodings: 000 : No Error 001: DPP Error Others : Reserved
11	RW	0x0	Core	Debug Request Error Detected HW sets this bit to indicate to Debug SW that an error was detected on the packet received on the USB3 link
10:1	RO	0x0	Core	Debug Request Length: Length of any data associated with the current request. This field is valid only when a debug request is pending.
0	RW1C	0x0	Core	Debug Request Pending: 1: Debug request is available for SW to consume 0: No request is pending for SW HW sets this bit to indicate to Debug SW that a control transfer request is pending for SW to handle. SW clears this bit once it has consumed the request.

Table 431. DBC_EXI_DEBUG_REQUEST_STACK_OFS

Address Offset: 108h - 147h

Bit	Access	Default Value	RST/PWR	Description
511:0	RW	00h	Core	Debug Request Stack: 64B Stack for incoming Device request and Data

Table 432. DBC_EXI_DEBUG_RESPONSE_INFO_AND_STATUS_OFS

Address Offset: 148h

Bit	Access	Default Value	RST/PWR	Description
31:16	RW	00h	Core	Response Data Length: Length of data associated with the current response. This field is valid only when a debug response is available. (bit[0] is set). The length of the data packet will be equal to the response data stack size except when the "Request Packet Last = 1" where it may a short packet (< response data stack size)
15:0	RO	0x0	Core	Reserved

Table 433. DBC EXI_DEBUG RESPONSE DATA STACK OFS

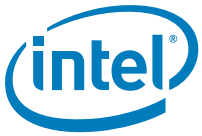
Address Offset: 180h - 37Fh

Bit	Access	Default Value	RST/PWR	Description
4095:0	RW	00h	Core	Debug Response Data: Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

Table 434. DBC EXI DEBUG RESPONSE DATA HEADER OFS

Address Offset: 380h - 38Ch

Bit	Access	Default Value	RST/PWR	Description
95:0	RW	00h	Core	Debug Response Header Response header generated by SW as a response to the current request/command processed by the SW



5.0 Electrical Specifications

5.1 Introduction

This chapter describes Titan Ridge DD DC and AC (timing) electrical characteristics. This includes absolute maximum rating, recommended operating conditions, power sequencing requirements, DC and AC timing specifications and TBT test electrical specification. The DC and AC characteristics include generic digital 3.3V IO specification, as well as other specifications supported by Titan Ridge DD.

5.2 Operating Conditions

5.2.1 Recommended Operating Conditions

See Table 435:

Table 435. Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
Ta	Operation Temperature Rang Commercial (Ambient; 0 CFS airflow)	0		65	°C
Tj	Junction Temperature			105	°C

Note: A solution using Titan Ridge DD should guarantee meeting one of the operating conditions i.e. either Ta is lower than 65C or Tj is lower than 105C.

Below are the thermal parameters for Titan Ridge DD:

ΘJA [deg/W] - 17-21

ΘJB [deg/W] - 10-13

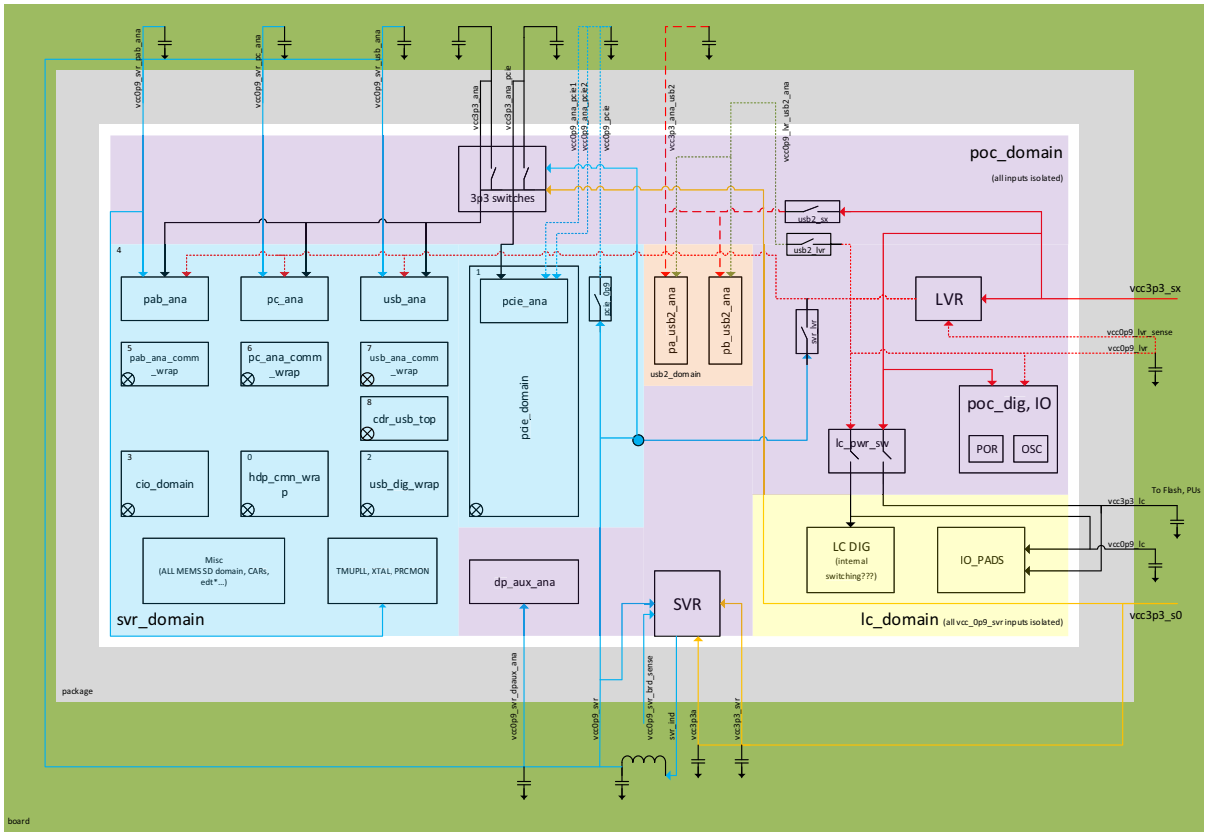
ΘJC [deg/W] - 3-6

5.3 Power Delivery

5.3.1 Power Delivery Introduction

Titan Ridge DD has two sources of 3.3v power supplies, which supply the power to the Titan Ridge DD seven power domains that are regulated and controlled within Titan Ridge DD. Titan Ridge DD controls its own power, based on the connectivity and system state/indications.

Figure 31. Titan Ridge DD Power Delivery



5.3.2 Power Supply specification

5.3.2.1 Power On Sequence

Figure 32. Power On Sequence

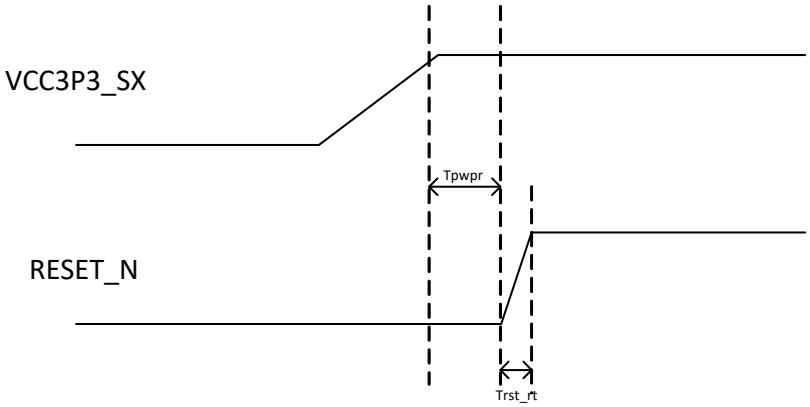


Table 436. Power On Sequence

Parameter	Description	Min	Max	Units	Comments
Tpwpr	From VCC3P3_SX at 90% to RESET_N de-assertion	100	-	us	
Trst_rt	RESET_N rise time	0.1	500	ns	

5.3.2.2 External Power Supply Specification

Table 437. External Power Supply Specification

VCC3P3 (3.3V) Parameters				
Title	**Description**	**Min.**	**Max.**	**Units**
Rise Time	Time from 10% to 90% mark	0.1	100	mS
Monotonicity	Voltage dip allowed in ramp	n/a	0	mV
Slope	Ramp rate at any given time between 10% and 90% Min: 0.8*V(min)/Rise time (max) Max: 0.8*V(max)/Rise time (min)	24	28,800	V/S
Operational Range	Operational range for VCC3P3_SX	3.07	3.465	V
	Operational range for VCC3P3_S0, VCC3P3_SVR, VCC3P3A	3.135	3.465	V

Table 437. External Power Supply Specification

VCC3P3 (3.3V) Parameters				
Title	**Description**	**Min.**	**Max.**	**Units**
Ripple	Maximum voltage ripple (peak to peak) for VCC3P3_SX, VCC3P3A, VCC3P3_SVR and VCC3P3_S0 up to 20MHz	n/a	40	mV
VCC3P3_SX	3.3 V (Sx rail) maximum current	n/a	100	mA
VCC3P3_S0	3.3 V (S0 rail) maximum current	n/a	700	mA

Note: * Please refer to reference design

Note: VCC3P3_S0 power supply shouldn't be applied earlier than VCC3P3_SX

5.3.2.3 Internal Voltage Regulator specifications

The Internal Voltage Regulator supplies Titan Ridge core voltage (0v9). The voltage levels are internally adjusted in order to keep the unit power within target. The following electrical parameters are expected on VCC0P9_SVR:

Table 438. Internal Switching Voltage Regulator Parameters

Title	**Min.**	**Typical**	**Max.**	**Units**
DC set point voltage	0.82		0.97	V
SVR output current	0.01		2.8	A
SVR Switching frequency	980	1000	1020	KHz
peak to peak Ripple at 1MHz switching frequency			4	mV

The Voltage Regulator requires an external inductor and capacitors which should be selected according to the following specifications.

Table 439. External Inductor Parameters

Title	**Min.**	**Typical**	**Max.**
Nominal Value at zero current	0.6µH		0.68µH
Accuracy	-20%		20%

Table 439. External Inductor Parameters

Inductance decreasing at 2.8A	0.6µH			10%
	0.68µH			20%
DCR				20mΩ
AC losses		It is recommended to use the manufacturer calculators to calculate total losses, and not only copper losses.		

Parameters for input and output capacitors are listed below:

Input: 4×10µF, X5R, 0402, 10V or 2×22µF, X5R, 0603, 10V - Ceramic Capacitor.

Output: 3×47µ, X5R, 0603, 6.3V - Ceramic Capacitor.

5.3.2.4 Power Consumption

Table 440. Power Consumption

Mode of Operation	Chip Power	Solution Power	Units
Cable Disconnect / Sleep w/o Wake	-	3	mW
Cable Disconnect S0 / Cable connect CS/RTD3 w/ Wake split arch (USB2)	-	9	mW
Cable Disconnect S0 / Cable connect CS/RTD3 w/ Wake	-	11	mW
1x TBT, x4 PCIe, DP Sink-SRC, DP Sink tunnel	1990	2280	mW
1x TBT, x4 PCIe, DP Sink-SRC, DP Sink tunnel CL0s	1630	1846	mW
1x TBT, x4 PCIe, DP Sink-SRC, DP Sink tunnel CL1	1594	1787	mW
MFDP (USB3.1 Gen2 re-time + x2 DP re-time)	840	920	mW
1x TBT (upstream) x4 PCIe	1375	1525	mW
1x TBT (upstream) DP SRC	1520	1700	mW

Mode of Operation	Chip Power	Solution Power	Units
2x TBT, x4 PCIe, 2x DP Sink tunnel	2270	2670	mW
2x TBT, x4 PCIe, DP Sink-SRC, DP Sink tunnel	2400	2840	mW
1x TBT, DP SRC, USB3.1 xHCI	1350	1500	mW
2x TBT, DP SRC, USB3.1 xHCI	1710	1950	mW
2x TBT, DP SRC, USB3.1 xHCI, x4 PCIe	2025	2330	mW
1x TBT , DP SRC, USB3.1 xHCI, x4 PCIe	1615	1825	mW
1x TBT, x4 PCIe	1350	1500	mW

5.4 DC/AC Specification

5.4.1 Digital I/Os DC specifications

See Table 441 and Table 435.

Table 441. Digital I/Os DC Specification

Symbol	Parameter	Conditions	Min.	Type	Max.	Unit
VCC3P3	Periphery supply		3.135	3.3	3.465	V
VOH	Output High Voltage	IOH = -8mA; VCC3P3 = Min	2.4			V
VOL	Output Low Voltage	IOL = 8mA; VCC3P3=Min			0.4	V
VIH	Input High Voltage		2.0		3.6	V
VIL	Input Low Voltage		-0.3		0.8	V
PU	Internal pullup		59	86	135	kΩ
Cin	Input Pin Capacitance				2	pF

5.4.2 XTAL/Clock Specification

See Table 442:

Table 442. XTAL/Clock Specification

Parameter Name	Symbol	Value
Nominal Frequency		25.000 MHz @ 25^0C
Vibration Mode		Fundamental
Operating/Calibration mode		Parallel
Frequency Tolerance @ 25^0 C	Δf/fo @ 25^0C	±30ppm
Temperature Tolerance	Δf/fo	±30ppm
Operating Temperature	Topr	-20°C to 70°C
Equivalent Series Resistor	ESR	50Ω maximum
Load Capacitance	Cload	20pF
Shunt Capacitance	Cshunt or Co	6pF maximum
Drive Level	DL	0.5mW maximum
Insulation Resistance	IR	500 M Ω minimum at DC 100V
Aging	Δf/fo	±5ppm per year maximum
External on-board Capacitors	C1,C2	20pF
Board Resistance	Rs	0.1Ω maximum

5.4.3 PCIe Electrical Specification

Titan Ridge DD PCIe interface supports the PCIe electrical as defined by the PCI Express Base Specification 3.0.

Note: Titan Ridge DD PCIe Gen3 electrical capabilities supports only the short reach and medium reach channels as defined by the PCI Express Base specification.

5.4.4 DisplayPort Electrical Specification

Titan Ridge DD Display interfaces supports the DisplayPort electrical as defined by the DP 1.2a Specification.

5.4.5 Trace Length Design Considerations

Table 443 defines trace length and insertion loss values that should be taken into consideration while designing boards for Titan Ridge as a function of the supported protocol and speed.

Table 443. Trace Length

Max IL	Port A	Port B	DP SRC	Port E	DPSNK1
CIO @ 10GHz	4 dB (1.5”)	4 dB (1.5”)	NA	NA	NA
CIO @ 5GHz	2.25 dB (2.0”)	2.25 dB (2.0”)	NA	NA	NA
USB3.1 @ 5GHz	6 dB (5.5”)	6 dB (5.5”)	NA	6 dB (5.5”)	NA
USB3.1 @ 2.5GHz	6.5 dB (12”)	6.5 dB (12”)	NA	6.5 dB (12”)	NA
HBR3 @ 4.05GHz	1.8 dB (1.5”)	1.8 dB (1.5”)	3.6 dB (3.1”)	NA	2 dB (1.6”)

Max IL	Port A	Port B	DP SRC	Port E	DPSNK1
HBR2 @ 2.7GHz	1 dB (2″)	1 dB (2″)	2 dB (4″)	NA	1.1 dB (2″)

5.5 Absolute Maximum Ratings

See Table 444.

Table 444. Absolute Maximum Ratings

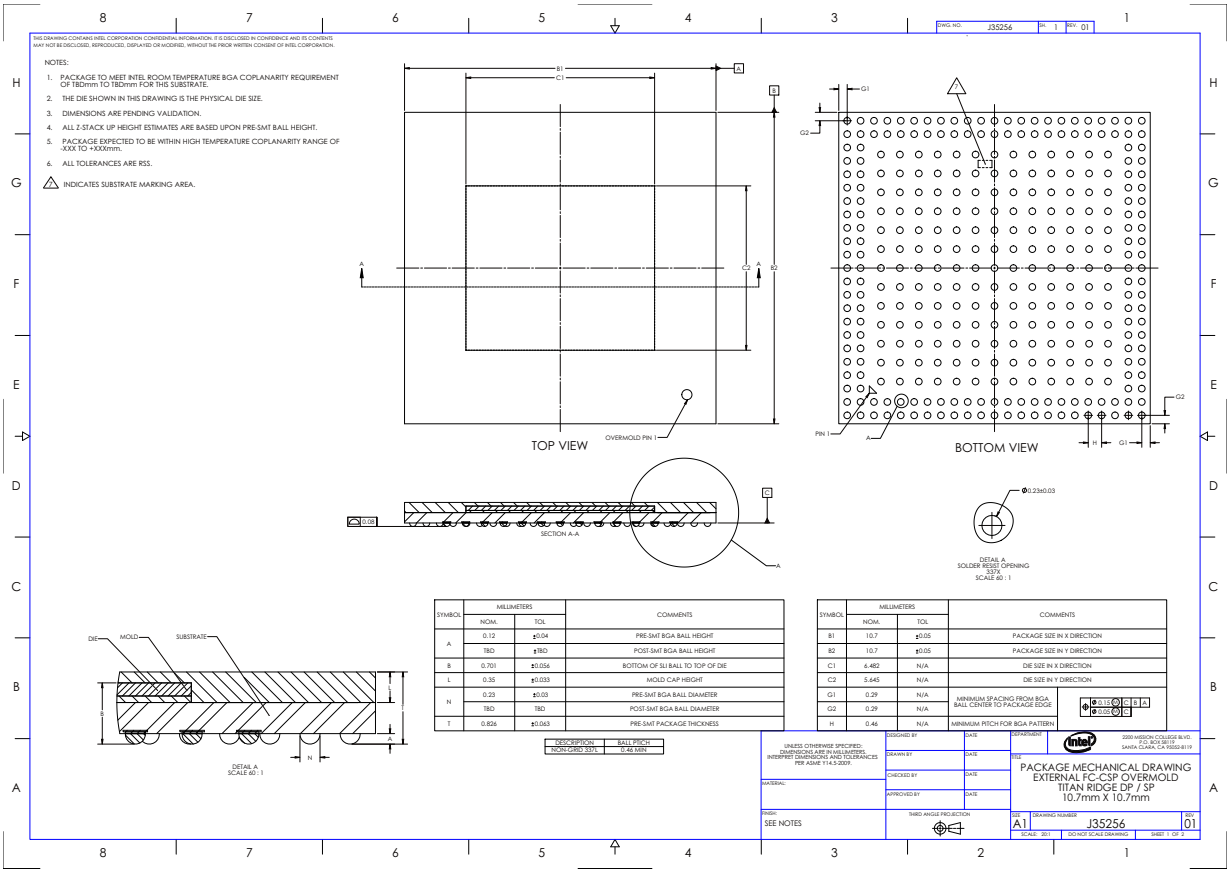
Symbol	Parameter	Min	Max	Units
Tcase	Case temperature under bias	0	105	C
Tstorage	Storage temperature	-65	140	C
Vi/Vo	3.3 V dc Compatible I/Os Voltage	VSS–0.5	4	V
VCC3P3	3.3 V dc Periphery DC Supply Voltage	VSS–0.5	4	V

Note: Ratings in this table are those beyond which permanent device damage is likely to occur. These values should not be used as the limits for normal device operation. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

6.0 Mechanical Specification

6.1 Package Information

Figure 33. Titan Ridge DD package

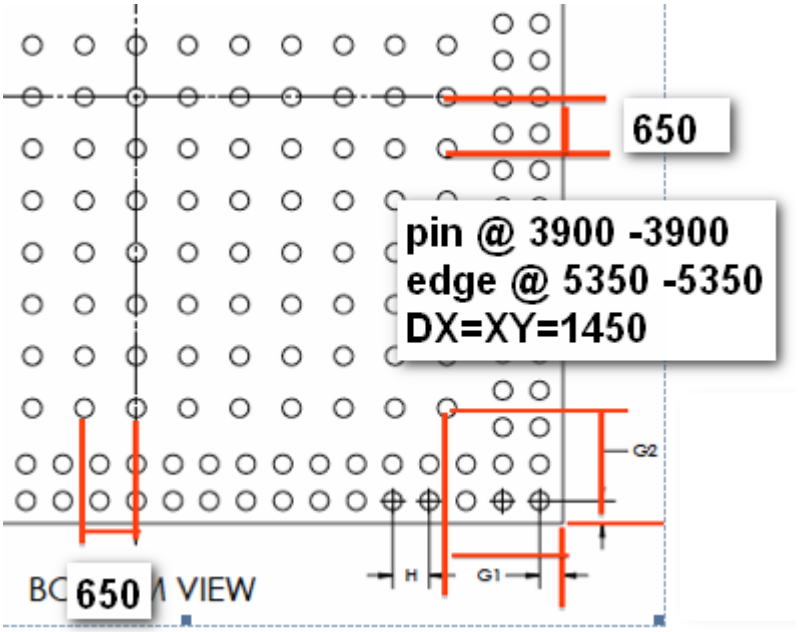


Ball-out is symmetrical In all directions. Outer pitch (X and Y) is 460u. Inner pitch (X and Y) is 650u.

UBM (for bumps) is 80u.

See Figure 34

Figure 34. Inner Pitch distances

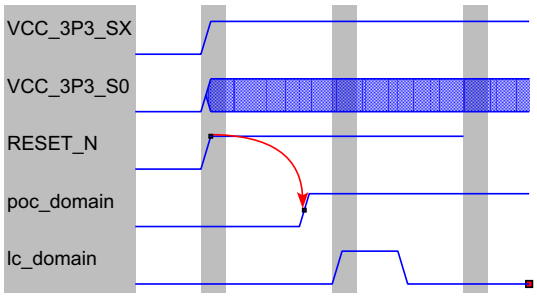


7.0 Power Up and Wake Flows

7.1 Power Up Flow

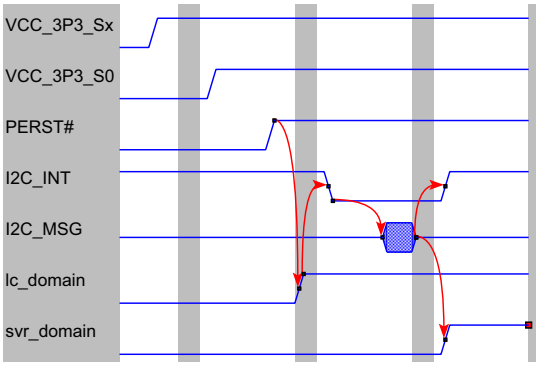
The Host Router power up flow consists of powering up the Sx rail and de-asserting the RESET_N pin of the Host Router. See figure Figure 35. Regardless of the S0 rail state, the Host Router will bring up poc_domain as a result of RESET_N de-assertion. Afterward the lc_domain (Link Controller) will be temporary powered. It will then shut down, unless S0 initializing conditions (described later) exist. The Host Router will stay in this uninitialized state as long as there are no S0 initializing conditions.

Figure 35. Host Power Up Sequencing for Sx Power Rail



To fully power up the Host Router, the S0 power rail should be supplied. The Host Router does not automatically monitor the S0 rails - it relays on FORCE_PWR or SLP_S3_N or PERST_N to detect S0 initialization transition, see Figure 36. PERST_N de-assertion triggers the powering up of the lc_domain. The same is applicable for SLP_S3_N de-assertion or FORCE_PWR assertion. Then (depending on I2C Master/Slave configuration) the Host Router communicates with the Port Controller in order to receive connection information and (in case of wake event) powers up svr_domain and all power domains required for proper wake event handling.

Figure 36. Host Power Up S0 Initialization (Host is I2C Slave)



The S0 initialization sequence is outlined above, assuming Host Router is configured as I2C slave. After PERST_N de-assertion the Host Router asserts I2C_INT which causes the Port Controller to issue I2C messages with connection information.

7.2 Host Router Power States

The system assumes to provide the Host Router power from two separate rails - VCC3P3_SX from a sustain rail and VCC3P3_S0 from S0 rail. The Host Router supports three main power states from an external power rails application perspective:

- Sr - reset power state, initial state (after Sx rail powered up and before power up sequence completed)
- S0 - device connected state, when both S0 and Sx power rails have to be applied
- Sx - device low power state, when S0 power rail can be disconnected, while Sx power state should be sustained

After the Sx power rail is applied, the Host Router enters Sr state. It will remain in this state until RESET_N de-assertion. When RESET_N de-asserted the Host Router will enter and stay in the Sx state (unless S0 initialization procedure is initiated). The Host Router will transition between S0 and Sx states according to system controls, unless RESET_N asserted (which will bring it back to Sr state).

7.3 Sx Entry/Exit Flows

The following section describes the Sx entry/exit flows for the Host Router. The system must perform a pre-notice Sx entry procedure through the TBT2PCIe mailbox in order to notify the entire Thunderbolt tree of the upcoming Sx entry. At the beginning of the pre-notice procedure, BIOS needs to ensure that the Host Router PCIe domain is powered on (as the Host Router can be active in DP or USB re-drive mode, while PCIe power domain is down). To ensure that, the FORCE_PWR line should be asserted.

The Host Router supports two modes of entering Sx state. The first mode is with Thunderbolt wake enabled. In this mode, the Host Router will trigger the CPU exit of low power states when it detects a cable side wake event. The second mode is without Thunderbolt wake enabled. In this mode, the Host Router will not react to cable side wake events.

7.3.1 Entering Sx state

7.3.1.1 Entering Sx state with wake disabled

There are two options to enter Sx state in wake disable mode:

- If the system wishes to keep power supplied to Host Router and connected devices, it should send the Go2Sx_No_Wake Command through the PCIE2TBT Mailbox before entering Sx. In this case, the Host Router and all connected devices will enter Sx state.
- If the system wishes to remove power supply from the Thunderbolt tree during Sx state, it should assert RESET_N prior to powering the device off (In this case BIOS pre-notice flow is not required).

7.3.1.2 Entering Sx state with wake enabled

The Sx entry of the entire Thunderbolt tree is performed automatically after BIOS sends the Go2Sx_Wake Command through the PCIE2TBT Mailbox before entering Sx. In this case, the Host Router and all connected devices will enter Sx state and BIOS command will be acknowledged. After that, the Host Router will wait for PERST_N assertion. ~10mS following PERST_N assertion the Host Router will enter Sx state. At this stage, S0 power rail can be safely removed (indicated by assertion of SLP_S3_N).

7.3.2 Exiting Sx state

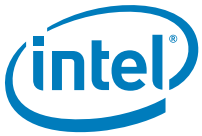
7.3.2.1 Exiting Sx state triggered by system

When exit from Sx state is required by the system, the S0 initialization procedure must be performed. The Host Router monitors RESET_N, FORCE_PWR and SLP_S3_N lines to be able to wake-up from a system event. The system can trigger exiting Sx state by negation of the SLP_S3_N line (after S0 rail is applied). Following SLP_S3_N negation, the Host Router will transition to the S0 state and recreate the state of the entire Thunderbolt tree. If there are connected devices, lc_domain will stay powered and recreate the power state of Host Router equal to the state before entering Sx - allowing communication with BIOS. If there is no connection present, the Host Router will stay with lc_domain powered off similar to regular power up flow.

When there is a connection present: the system, when exiting Sx, should indicate to the Host Router whether there was a Thunderbolt device connected before entering Sx. This is done by the BIOS (through the PCIE2TBT mailbox) using Sx_Exit_TBT_Connected or Sx_Exit_No_TBT_Connected messages. According to the BIOS message, Host Router will perform either a fast link bring-up (if there were Thunderbolt devices connected before Sx entry) or a regular link bring-up (if there were not Thunderbolt devices connected before entering Sx).

7.3.2.2 Exiting Sx state triggered by Thunderbolt wake event

The Host Router monitors the LSRX line to be able to wake-up from a Thunderbolt wake event. Upon Thunderbolt wake event, the Host Router will assert the WAKE_N line to the system until PERST_N is de-asserted by system (WAKE_N will not be asserted if the Host Router woke up due to SLP_S3_N de-assertion). The Host Router will delay powering on of all digital domains (except poc_domain and lc_domain) until SLP_S3_N is de-asserted by the system.



8.0 In-line Functionality

8.1 Thunderbolt Base Protocol Functionality

The Titan Ridge DD controller implements the Thunderbolt base protocol functionality as defined by the Thunderbolt protocol specification, this includes the base protocol as well as the Thunderbolt Host interface adapter, PCIe adapter and DisplayPort adapter.

For more details please refer to the Thunderbolt Protocol Specification.

8.2 Lane Speed

Titan Ridge DD controller supports two lane speeds 10Gbps and 20Gbps. By default, Titan Ridge DD publishes support for lane speed of 20Gbps. Lane speed may be changed by the connection manager.

Both lanes of the same port (P1+P2) should always use the same lane speed. Different ports may use different lane speeds. A lane will come up at 20Gbps only if both the cable and link partner support 20Gbps. Upon cable plug the link controller sets the link speed, before the lane is enabled.

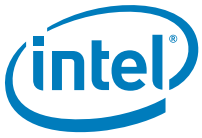
8.2.1 Lane Speed Transition

Speed transition is usually initiated by the connection manager by following the steps below:

- Connection Manager configures the required speed at the down facing ports, by setting PHY_PORT_CS_1/Target_Link_Speed[3:0]. The same setting should be set in both lanes of the down facing port
- Connection Manager sets Link Controller SW_FW_MAILBOX_IN/sw_force_lstx_low[6] (on hosts, cio power should be forced during this stage)
- The Link Controller will force lstx low and disable the high speed link
- Connection Manager clears Link Controller SW_FW_MAILBOX_IN/sw_force_lstx_low[6]
- After at least 100ms. The Link Controller releases lstx and enables the high speed link
- The speed is set to the maximum of the value set in PHY_PORT_CS_1/Target_Link_Speed[3:0], the link partner and the cable
- The negotiated speed is reported at PHY_PORT_CS_1/Current_Link_Speed[19:16]

8.3 Lane Bonding

Lane Bonding or Lane Aggregation is the process of joining 2 physical lanes (running between two Thunderbolt ports) into a single, double width, logical link. Titan Ridge DD supports Lane Bonding. The double width link allows better utilization of the Thunderbolt link by the tunneled protocols.



8.3.1 Lane Bonding Enablement

Lane Bonding is enabled when both ends of the link support and publish dual lane capability. By default, in order to support Legacy hosts, all devices will initially publish single lane capability. It is the responsibility of the CM (internal or external) to upgrade the link to Dual width if both ends support it.

Lane bonding is supported for each port pair (P1+P2) separately.

Note: Lane bonding when lane speed is 10Gbps creates a link of 20Gbps, when lane speed is 20Gbps the logical link speed will be 40Gbps.

8.3.2 Lane Width Transitions

CM may change the link width or disable a port as long as it follows the directions in the table below. The required actions column refers to fields in PHY_PORT_CS_1 (Target Link Width[7:4], Link disable[14], Link Retrain[15]) of the relevant port. The negotiated width is published at the same register (Negotiated Link Width [23:20]). When transiting between single and bonded modes, CM must teardown all active paths prior to width transition.

The table lists the required actions to control ports P1+P2. The table also includes the expected plug/unplug events per transition.

Table 445. Required actions to control ports P1+P2

#	Strat Mode	Require Mode	Require Actions	Results	Comments
1	Bonded Link up	2 Single Lanes up	P1 width=1 P2 width=1, retrain=1	Plug event on P2	TS only. Takes ~640ns. No link drop
2	2 Single Lanes Up	Bonded Link up	Partner P1 width=3 Partner P2 width=3 P1 width=3 P2 width=3, retrain=1	Unplug event on P2	TS only. Takes ~640ns. No link drop
3	Bonded Link up	Both lanes disabled	P2 disable=1 P1 disable=1	Unplug event on P1	
4	Single Lane Up	Single Lane disabled	Pn disable=1, width=1	Unplug event on Pn	Same as in Old-Ridge
5	Single Lane Disabled	Single Lane up	Pn disable=0, width=1	Plug event on Pn	Same as in Old-Ridge
6	Lanes Disabled	Bonded Link up	Do flow 5 for P1, P2. Wait for both plug events Do flow 2		(upstream unplug will cause the partner ports to reset to single)
7	Bonded Link up	Single Lane up, Single Lane disabled	Do flows 1, 4		
8	Single Lane up, Single disabled	Bonded Link up	Do flow 5, wait for plug event, do flow 2		

8.3.3 Lane Monitoring of a Bonded Link

Lane monitoring is enabled also for a bonded link. In case of a Dual link stuck at training or increasing HEC errors count, both ports will be enabled/disabled.

8.4 Forward Error Correction (FEC)

By default FEC is enabled for 20Gb/s TBT links and disabled for 10Gb/s TBT links. SW can change the change the link behavior by performing the following steps:

1. Read the current preference from CM_LC_LINK_CONFIGURATIONS (0x1C0 for PA/0x2C0 for PB):

    Bit0: 10G FEC preferred (default to 0).

    Bit1: 20G FEC preferred (default to 1).

2. Change the setting on the downstream facing LC.

3. Retrain the link by asserting force_lstx_low bit on SW_FW_MAILBOX (0x139[6]/0x239[6]) for a minimum period of 100ms.

4. 10Gb/s link will train with FEC if either side prefers to enable it. 20Gb/s link will train with FEC if both sides prefer to enable it.

5. The current FEC state of the link is reflected in LC_PARTNER_STATE (0x1AA/0x2AA):

    Bit 10: 10G FEC enabled.

    Bit 11: 20G FEC enabled.

FEC Error counters are located at port_cs 0x4a. This already appears in the DS (VSEC_CIO_CS_12):

[15:0] uncorrectable (detected) errors count. Clear by write.

[31:16] correctable errors count. Clear by write.

8.5 Security Schemes

Titan Ridge DD supports different levels of security for device connection and PCIe tunneling.

See Table 446 for Titan Ridge DD defined security levels.

Table 446. Defined Security Levels

Value	Description
0x0	No Security - Allow legacy Thunderbolt devices auto connect – at this mode the connection manager auto connects to a new device plugged in
0x1	User Authorization - Allow User Notification devices at minimum – at this mode the connection manager requests connection approval from the host SW, auto approval may be given based on the Unique ID of the connecting device
0x2	Secure Connect - Allow One time saved key devices at minimum – at this mode the connection manager requests connection approval from the host SW, auto approval is only given if the host challenge to the device is acceptable
0x3	Display Port Only - Allow only DP sinks to be connected (re-driver or DP tunnel, no PCIe tunneling) – at this mode no tunneling is done for PCIe devices
0x4	USB Docking Only - Allow only a single Thunderbolt device to be connected, within the device only the integrated xHCI controller is enabled, all PCIe functions are disabled and no additional tunneling is supported.
0xF-0x5	Reserved

Titan Ridge DD Unique ID is fused in the Thunderbolt controller as part of the manufacturing process. Once set the Unique ID can't be altered.

The default value of the security level for the Titan Ridge DD device is loaded from flash memory. The default security level is 0x1

8.5.1 User Authorization

At this security level the connecting device indicates the CM of the Thunderbolt link connection; the CM requests host driver approval for the specific Unique ID that got connected prior to the PCIe tunnel creation. During the first connection of a unique ID the user will be prompt to approve.

The user will need to approve the interface and choose between a single/permanent/no connection approval.

Once a device is approved for permanent auto connect, its unique ID is saved by the SW as part of an ACL list for future auto connection (no user involvement).

8.5.2 Secure Connect

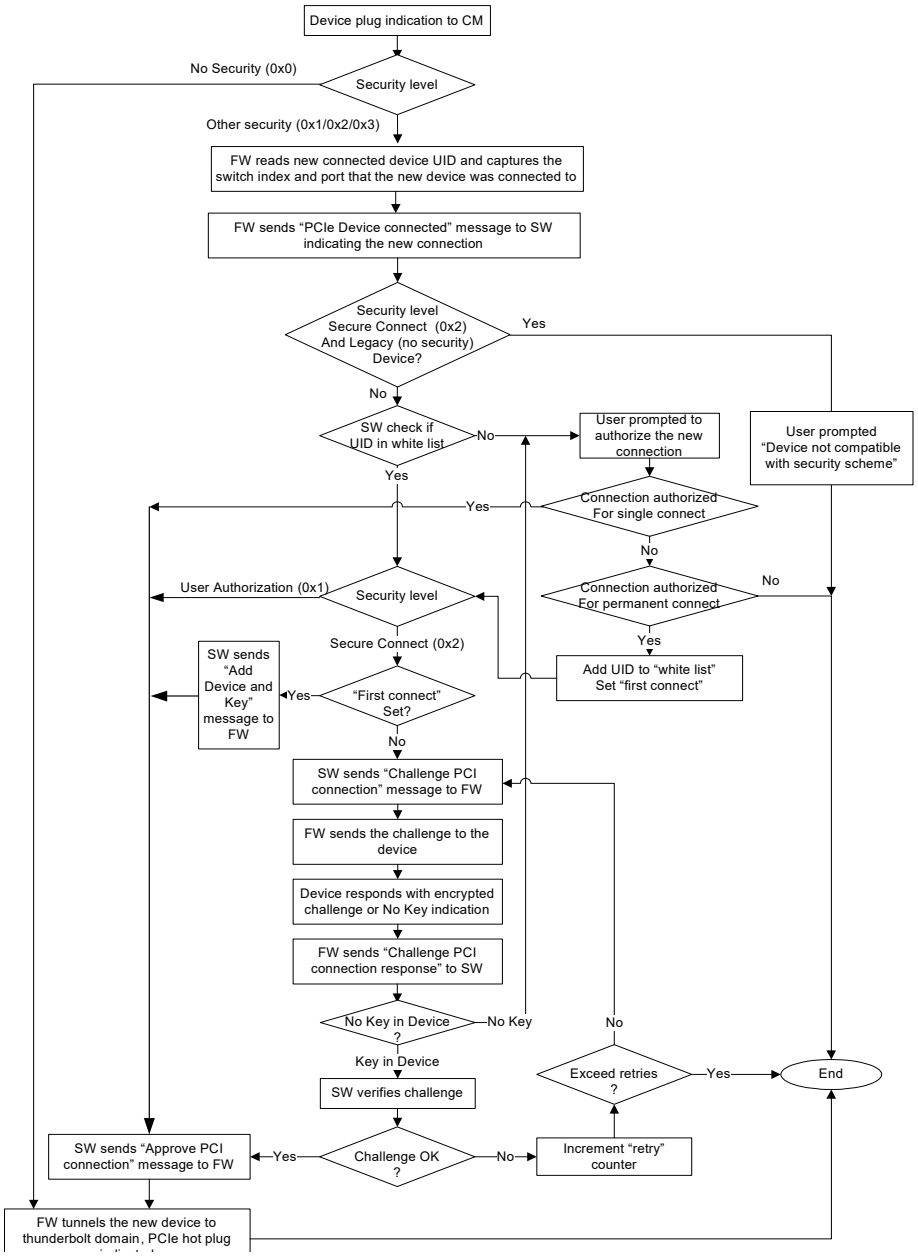
This level of security will not be available on Controllers prior to Falcon-Ridge generation.

At this security level the connecting device indicates the CM of the Thunderbolt link connection; the CM requests host driver approval for the specific Unique ID that got connected prior to Thunderbolt tunnel creation. During the first connection of a unique ID the user will be prompt to approve.

Once a device is approved by the user, the host would generate and send to the device a random Key. Together with the Unique ID the device will be added to the ACL list for future auto connection (no user involvement). On future connections of the same device the Unique ID is sent to the host, the host sends the device a challenge (random number value) and expects to get the value encrypted using the pre assigned key. Once received, the host checks the encryption and approves/rejects the tunnel creation to the CM.

If the process fails a pre-set number of times - the SW would treat the device as a new device connected and prompt the user to re-approve.

Figure 37. Device Authorization Sequence



8.5.3 Security Level Change

As needed, the security levels can be changed by the user at the BIOS menu by communicating with the CM through the PCIE2TBT/TBT2PCIE mailbox utilizing the following flow:

- BIOS drives POC_GPIO_3 high
- BIOS enumerates the Host Router (if needed)
- BIOS uses the PCIE2TBT mailbox to set the new security level (Command = "Set security level")
- CM gets the new security settings
- CM verifies POC_GPIO_3 is set by checking gpio_data_in[3]
- If set CM updates the new security mode in NVM
- If cleared security setting will not be updated in NVM
- CM completes the SW transaction by indicating Set security level Done in the TBT2PCIE register with the security settings as received from the PCIE2TBT command
- On a security mode change CM disconnects all PCIe paths, PCIe paths can re-connect on security level 0x0 only, other security levels will require user approval as the ACL list should be cleared
- BIOS polls the TBT2PCIE register to get the "Done" indication
- BIOS should use the PCIE2TBT mailbox to verify the new security level was set (Command = “Get security level”)
- CM completes the SW transaction by indicating Get security level Done in the TBT2PCIE register with the security settings from NVM
- BIOS drives POC_GPIO_3 low
- Driver should clear the saved ACL list on any security mode change
- The driver is notified of the current security level in the Driver Ready Response message

8.6 Quality of Service (QoS) support

Thunderbolt protocol tunnels DisplayPort and PCIe protocol across the Thunderbolt domain, DisplayPort traffic is isochronous and as such is given the highest priority when tunneled over Thunderbolt. PCIe traffic can be either isochronous or bulk/best effort. Titan Ridge DD implements quality of service features to enable different PCIe traffic types/streams get different priorities and/or allocation as part of the Thunderbolt tunneled PCIe traffic for devices that require such capabilities.

The capabilities added in Titan Ridge DD include:

- Two virtual channels (VC) within the PCIe domain to be used for upstream Rd/Wr and downstream completions to enable higher priority (ISOC) traffic to bypass bulk PCIe traffic
- Completion Allocation buffers inside DN bridges per VC to allow draining downstream completion from UP bridge Flow control buffer
- Ability to restrict the outstanding upstream reads sent from an upstream/downstream bridge to the amount of buffering supported in the completion buffer of that UP/DN bridge

8.6.1 Completion Allocation Buffers (CAB)/Memory read moderation

Preallocate completion buffers in downstream bridges, prior to sending read request up to root complex so that a downstream port doesn’t block other downstream ports, and limit the amount of memory read requests sent to the Root complex.

When read request is processed, completions stream at wire speed down and do not block other requesters completions. If there is no space in completion buffers, read request is not sent upstream. Such preallocation is needed only in DS bridges that face PCIe over TBT tunnels. Physical devices are expected to be ready to drain completions without back pressure.

Preallocation buffers (and configurations) are provided for both VC0 and VC1 priority channels.

8.6.1.1 CAB SW Control

CAB control contains enabling of Completion Allocation Buffer inside Downstream Port and option to limit the amount of outstanding read requests in upstream direction. The read moderation can be applied in Downstream Port or Upstream Port.

Two Vendor Registers (per bridge) controls these (one for each VC):

- VESC_REG 18 (Offset 550h): CAB VC0 register
- VESC_REG 19 (Offset 554h): CAB VC1 register

The structure of these two register is identical, main controls described below (for the full register description "VESC_REG 18 (Offset 50h): CAB VC0 register")

- Bit 0 enables the Completion Allocation Buffer (valid for DN port), When 0, completions flowing towards this DN port will be stored only in the common completion buffer of the US port (legacy mode)
- Bit 1 enables the MemRd moderation
- Bits 31:16 is the threshold of outstanding data in DW (loaded with bit 2)

These registers enable the configuration of the following functionalities:

Downstream Port:

- Ability to enable (per VC) the completion buffer
- Ability to control (per VC) the outstanding upstream read request data in each downstream port

Upstream Port:

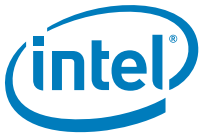
- Ability to control (per VC) the outstanding upstream read request data in the upstream port

8.6.2 Virtual Channel Support

Virtual channel implementation is according to PCIe 3.0 specification, for all traffic types (Posted, None Posted, Completions). Two virtual channels have been implemented VC0, VC1 including VC Extended Capability, Flow Control buffers per VC and VC arbitration inside PCIe Switch.

VC0/VC1 fully supported within PCIe in Thunderbolt along with set of custom capabilities to enable:

- Ability to configure VC1 from Vendor Register, that act as shadow registers for the VC Extended Capability, to hide from PCIE Software any existence of VC1 channel.
- Custom Weighted Round Robin VC Arbitration control from Vendor Registers instead VC Extended Capability tables.
- Physical PCIe links to support only VC0 and still route ingress / egress traffic to VC0 or VC1 channel (these for the links connecting to the root port, end point or legacy Thunderbolt devices)
- Ingress and Egress TC re-mapping, including some flexible configuration per Requester ID, to be used on the physical facing downstream bridges



These can be summarized by four traffic flows:

1. Upstream memory requests (MemWr / MemRd)
   - Memory TC can be remapped to TCx inside the Downstream Port facing endpoint to flow on VC1
   - Upstream Port facing Root Complex will remap only MemWr TCx back to TC0
2. Upstream completions (Cpl / CplD) stay as is with TC0 on VC0 channel, and additional custom implementation will allow upstream VC0 Completion to push upstream VC0 and VC1 posted packets.
3. Downstream completions (CplD)
   - Root complex returns completions with the same TCx value of the respective request
   - Downstream ports facing Endpoint will remap Cmpl TCx back to TC0
4. Downstream memory request (MemWr / MemRd) stay as is with TC0 on VC0 channel.

8.6.2.1 Custom VC SW Control

QoS by default is controlled from VC Extended Capability (VC1 enable and TC/VC mapping) as described in PCIe Specification.

But for supporting of custom VC in Thunderbolt there are additional custom set of controls.

Several bits and registers controls these custom additional features:

- VESC_REG 2 (Offset 510h) bit 2 - Master VC1 enable for PCIe Switch and should be set in Upstream Port

Per Bridge configuration:

- VESC_REG 21 (Offset 55Ch): QoS - Load priority & Custom mode register
- VESC_REG 22 (Offset 560h): Shadow port VC Capability and VC Resource Control register
- VESC_REG 23 (Offset 564h): TX and Rx TC remapping register
- VESC_REG 24-31 (Offset 568h - 584h): Rx remapping BDF tables.

8.6.2.2 Custom Mode Control

PCIe Port (Upstream or Downstream) can be configured either to custom VC mode in which both VC0 and VC1 are enabled on the PCIe link and the only difference from Specification mode is that it is controlled from vendor registers or Port can be configured to be in custom VC0 only mode in which only VC0 is enabled externally on the link, while internally it has VC1 channel + VC1 Flow Control Buffers and Ingress / Egress TC remapping is used to adapt between these two parts.

There would be four modes of configuration/operation and any Thunderbolt PCIe Bridge that is enabled for custom VC will need to be configured as one of these 4 options:

1. Upstream facing Root (physical link of Host controller or upstream Titan Ridge DD port facing legacy Thunderbolt device) custom VC0 only mode + Egress TC remapping + Upstream read moderation
2. Downstream facing TBT (Downstream Titan Ridge DD port facing Titan Ridge DD device) custom VC0 + VC1 mode + TC/VC mapping + CAB + DN read moderation
3. Upstream facing TBT (Upstream Titan Ridge DD port facing Titan Ridge DD Host/Device) - custom VC0 + VC1 mode + upstream read moderation

4. Downstream facing Endpoint (physical link of Titan Ridge DD Device port or downstream Titan Ridge DD port facing Thunderbolt legacy device) custom VC0 only mode + Ingress / Egress TC remapping + CAB + DN read moderation

General Port mode is controlled with VESC_REG 21 bits 25,24 (custom mode is enabled through bit 24 and setting also bit 25 will put the port to custom VC0 mode)

8.6.2.3 VC Arbitration control

There are two stages of VC arbitration in egress of each PCIE Bridge.

1. First stage resides in PCIE Switch interconnection and it is WRR within each VC per packet type (NP,P,CMPL)
2. Second stage resides in PCIE Bridge before Retry Buffer and it is WRR between VC over all packet types (NP/P/CMPL)

VC arbitration is controlled by simple priority value of each stage which defines the ratio between VC1 and VC0 packets.

First arbitration stage is controlled by stage VESC_REG 21 bits [7:0] (which is loaded with bit 16)

Second arbitration stage is controlled by stage VESC_REG 21 bits [15:8] (which is loaded with bit 18)

Actual Use:

- Downstream
  - — Weighted Round Robin arbitration (control) of data completion between VCs
  - — Weighted Round Robin arbitration (control) over all Types (C, P, NP) between VCs
- Upstream
  - — Round Robin arbitration between downstream Ports per type per VC (no SW control)
  - — Weighted Round Robin arbitration (control) per Type (P, NP) between VCs
  - — Weighted Round Robin arbitration (control) over all Types (P, NP) between VCs

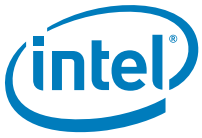
8.6.2.4 Shadow VC1 control

When custom mode is enabled VC Extended Capability doesn’t have any effect and should stay as if only VC0 is enabled (with all TC mapped to VC0).

VESC_REG 22 acts as minimized shadow register for several registers in VC Extended Capability and controls the VC1 enable + TC/VC remapping.

- Bits [15:0] are used as shadow for Port VC Capability Register 1.
  - — Bits [2:0] and [6:4] are Extended VC count fields and should be loaded to 001b
- Bits [31:16] are used as shadow VC Resource Control Register for VC1.
  - — Bit 31 is VC1 enable and bits [26:24] is the VC ID, which should be loaded to 001b
  - — Bits [23:16] are the TC/VC1 mapping (TC/VC0 mapping will be complement to this configuration)

Note: these configuration should be done in all VC1 related ports (in regular custom mode and also in custom VC0 mode)



8.6.2.5 TC Remapping control

VESC_REG 23 is the main register that controls Ingress / Egress TC remapping which should be used at ports in custom VC0 only modes in order to prioritize some traffic and rout it to VC1 channel within PCIE Switch.

VESC_REG 23 Bits [15:0] are used to control Tx/Egress TC remapping.

- Bits 3:0 are per packet type bits that enables to remap all TC to TC0, before packet is transmitted
- Bits 7:4 are per packet type bits that enables to remap one specific TC (bits 10:8) to TC0, before packet is transmitted

VESC_REG 23 Bits [31:16] are used as shadow Rx / Ingress TC remapping.

- Bits 19:16 are per packet type bits that enables to remap all incoming packets to specific TC (bits 22:20)
- Bits 26:23 are per packet type bits that enables to remap incoming packets with non-matching BDF to BDF table to specific TC (bits 29:27)

Note: If Ingress TC remapping is not enabled globally, then BDF table is used and if packet doesn't match the table the default option is used.

VESC_REG 24-31 are registers that acts as 8 entry table for the Ingress TC remapping and enables to do the remapping based on

The structure of each entry is similar:

- Bits 3:0 are per packet type bits that enables to remap TC of incoming packets that their BDF matches bits 31:16 to specific TC (bits 6:4)
- Bit 7 enables to ignore function number, which enables to treat Multi-function Device as one unit and remap all its packets.

These registers enable the configuration of the following functionalities:

- Downstream Port
  - Ingress TC remapping per type either for whole traffic or per Requester ID (to be used for P, NP)
  - Egress TC remapping per type (to be used only for Cmpl)
- Upstream Port
  - Egress TC remapping per type (to be used only for P)

8.6.3 QoS Configuration flow

The configuration flow should be done according to the following steps

- Power up of Host/Device
- NVM based configurations - General VC1 settings, initial setup of WRR arbitration + default TC re-mapping + default CAB and read moderation, none of these features is enabled
- Thunderbolt link established
- CM reads host/device characteristics from NVM (DROM)
- CM updates the configuration as needed and enables the proper functionalities (Impacted by upstream/downstream device type and topology in the daisy chain)
- PCIe tunnel created, PCIe link up, PCIe enumerated

- CM/SW updates last configurations as needed - TC remapping on BDF configuration (if needed), read moderation throughout the Thunderbolt tree (as needed), need to avoid this configuration during traffic (device needs to be idle/paused), Dynamic Host upstream configuration could change (enable VC1/TC remapping) if a QoS device was connected

DROM content should add characteristics that would help CM configuration and should reflect:

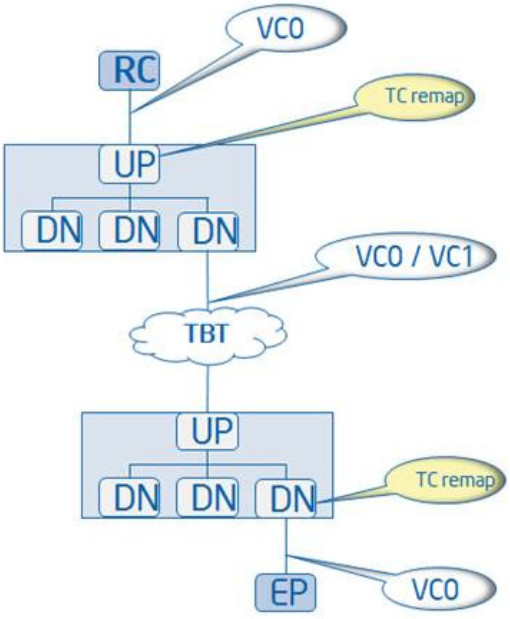
- Per downstream bridge information:
- Per direction (Up/Dn) Max BW (global)
- Per direction (Up/Dn) Min BW (ISOC)
- Number of PCIe functions (for MFD)
- Max outstanding read data (in Bytes)

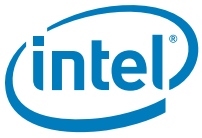
8.6.4 Basic register configuration for the four different modes of operation (Example):

As indicated, there are basically four main options to enable custom VC1 depending on the Port type and whether it faces the Thunderbolt link or not.

Over Thunderbolt link with partner that supports as well VC1, the link can be with two channels (Same as regular Spec mode, just controlled from vendor registers).

For the Port that faces a physical link (or legacy Thunderbolt device that doesn't support VC1), the custom VC will be configured internally only, using TC remapping.





8.6.4.1 Upstream facing physical link (Root)

This port is in custom VC0 only mode with additional configuration of Egress (P) TC remapping and TC/VC mapping.

MemRd moderation can be configured to limit overall outstanding read request that flows toward Root.

- VESC_REG 18 (offset 0x550)
  - vesc_reg18[1] - VC0 MemRd moderation enable in Upstream Port
  - vesc_reg18[2], [31:16] - Load MemRd moderation threshold for VC0 in units of DW
- VESC_REG 2 (offset 0x510)
  - vsec_reg2[30] - Enable VC1 in PCIE Switch
  - vesc_reg2[28] - Bypass Credit Check
- VESC_REG 21 (offset 0x55C)
  - vsec_reg21[25], [24] - Custom VC0 only mode (VC0 only)
  - vsec_reg21[30], [29], [26] - Rx TC/VC map according to Spec (0xFF) + map according to source
  - vesc_reg21[16], [7:0] = 08h to set per type arbitration (or other required priority value)
  - vesc_reg21[18], [15:8] = 08h to set over all type arbitration (or other required priority value)
- VESC_REG 22 (offset 0x560)
  - vsec_reg22[31], [26:24] = 001b, [23:16] = 02h - Shadow Register to map TC1 to VC1 (also possible other mapping, for example 0xFE)
- VESC_REG 23 (offset 0x564)
  - vsec_reg23[0] - Re-Map all Posted back to TC = 0

8.6.4.2 Downstream facing link over TBT domain

This port is in custom VC0 + VC1 mode with configuration of TC/VC mapping (VC0 and VC1 credits are exchanged with partner over TBT link)

CAB buffer along with MemRd moderation can be configured to limit outstanding read request that flows toward Root.

- VESC_REG 18 (offset 0x550)
  - vesc_reg18[0] - VC0 CAB enable in Downstream Port
  - vesc_reg18[1] - VC0 MemRd moderation enable in Downstream Port
  - vesc_reg18[2], [31:16] = 0080h - Load MemRd moderation threshold for VC0 in units of DW (to 4K bit = 128 DWs)
- VESC_REG 21 (offset 0x55C)
  - vsec_reg21[24] - Custom VC mode
  - vsec_reg21[30], [29], [26] - Rx TC/VC map according to Spec (0xFF) + map according to source
  - vesc_reg21[16], [7:0] = 08h to set per type arbitration (or other required priority value)
  - vesc_reg21[18], [15:8] = 08h to set over all type arbitration (or other required priority value)
- VESC_REG 22 (offset 0x560)

  - vsec_reg22[31], [26:24] = 001b, [23:16] = 02h - Shadow Register to map TC1 to VC1 (also possible other mapping, for example 0xFE)

8.6.4.3 Upstream facing link over TBT domain

This port is in custom VC0 + VC1 mode with configuration of TC/VC mapping (VC0 and VC1 credits are exchanged with partner over TBT link).

- VESC_REG 2 (offset 0x510)
  - vsec_reg2[30] - Enable VC1 in PCIE Switch
- VESC_REG 21 (offset 0x55C)
  - vsec_reg21[24] - Custom VC mode
  - vsec_reg21[30], [29], [26] - Rx TC/VC map according to Spec (0xFF) + map according to source
  - vesc_reg21[16], [7:0] = 08h to set per type arbitration (or other required priority value)
  - vesc_reg21[18], [15:8] = 08h to set over all type arbitration (or other required priority value)
- VESC_REG 22 (offset 0x560)
  - vsec_reg22[31], [26:24] = 001b, [23:16] = 02h - Shadow Register to map TC1 to VC1 (also possible other mapping, for example 0xFE)

8.6.4.4 8.5.4.4 Downstream facing physical link (Endpoint)

This port is in custom VC0 only mode with additional configuration of Ingress (NP/P) / Egress (Cmpl) TC remapping and TC/VC mapping.

- VESC_REG 2 (offset 0x510)
  - vesc_reg2[28] - Bypass Credit Check
- VESC_REG 21 (offset 0x55C)
  - vsec_reg21[25], [24] - Custom VC0 only mode (VC0 only) + map according to source + Rx TC/VC map according to Spec FF reg
  - vsec_reg21[30], [29], [26] - Rx TC/VC map according to Spec (0xFF) + map according to source
  - vesc_reg21[16], [7:0] = 08h to set per type arbitration (or other required priority value)
  - vesc_reg21[18], [15:8] = 08h to set over all type arbitration (or other required priority value)
- VESC_REG 22 (offset 0x560)
  - vsec_reg22[31], [26:24] = 001b, [23:16] = 02h - Shadow Register to map TC1 to VC1 (also possible other mapping, for example 0xFE)
- VESC_REG 23 (offset 0x564)
  - vsec_reg23[2] - Re-Map all Completions back to TC = 0.
  - vsec_reg23[16], [17], [22:20] = 001b - Re-Map all Rx Posted and Non-Posted to TC1 (also possible to configure the BDF table instead)

8.7 PCIe Phy Eye Monitor

The Titan Ridge DD PHY features the capability to perform on-chip eye diagram scan at the receiver, which allows the user to "see" the eye opening (height and width) of the received data after equalization. This is a frequently utilized tool enabling characterization of the receiver equalizer.

8.7.1 Overview

The on-chip eye feature works by sweeping the time-axis (x) and the voltage-axis (y), and the corresponding bit error ratio is calculated by comparing "roaming" sample with the data sample. BER is a function of x-offset and y-offset, and it is calculated at each (x-offset, y-offset) point. The result of a BER scan eye diagram is a two-dimensional matrix that can be displayed using different color shades representing varying BER values.

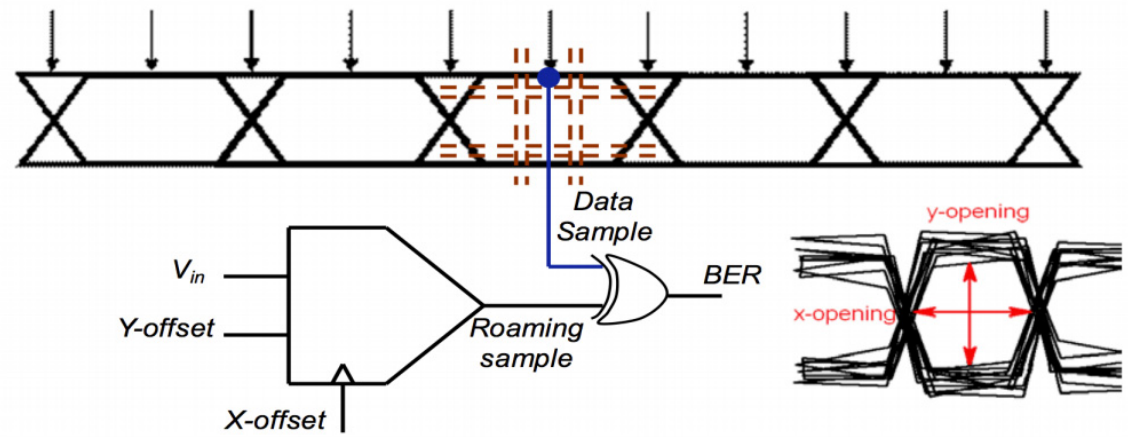


Figure 38. Overview of On-chip Eye Measurement

The on-chip eye measurement can occur during normal operation of the link, and is non-destructive to the link. The on-chip eye is "data-agnostic" - it does not require any specific data sequence and can be used with any PRBS sequence.

The measurement procedure is intended to be implemented in software on the host system. The software needs to read/write the registers that program the x- and y-offset sweeps, and read out the BER measurement for each corresponding point. Once all of the data points have been captured, a 2-D image may be plotted based on the results. An example eye plot captured for 10Gbps data using x-offset of 3ps, y-offset of 20mV, and 562 receive data bits is shown in Figure 39.

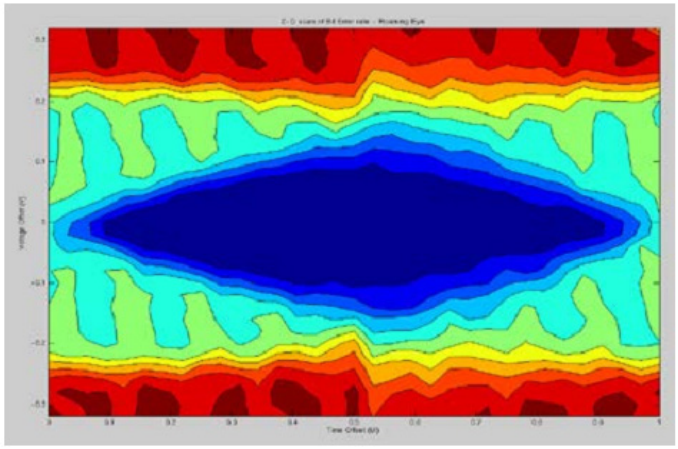


Figure 39. Example BER Eye Plot

Although BER scan eye diagram shows the eye opening of the received signal after equalization, it is not as intuitive as the eye diagrams generated on an oscilloscope. To gain better understanding of the variation in BER captured in the entire range, we need to know the rate of change when the x-offset steps into the next bit or when the y-offset crosses the next level. This is achieved by taking derivatives of the BER in both x-offset and y-offset directions, and combing the two gradient maps into a single map by calculating the root of the square sum of the two gradients. Aside from the eye opening information, this gradient plot also lets you know the transitions and crossing points. As an example, Figure 40 shows a simulated eye on the left and its corresponding gradient plot on the left.

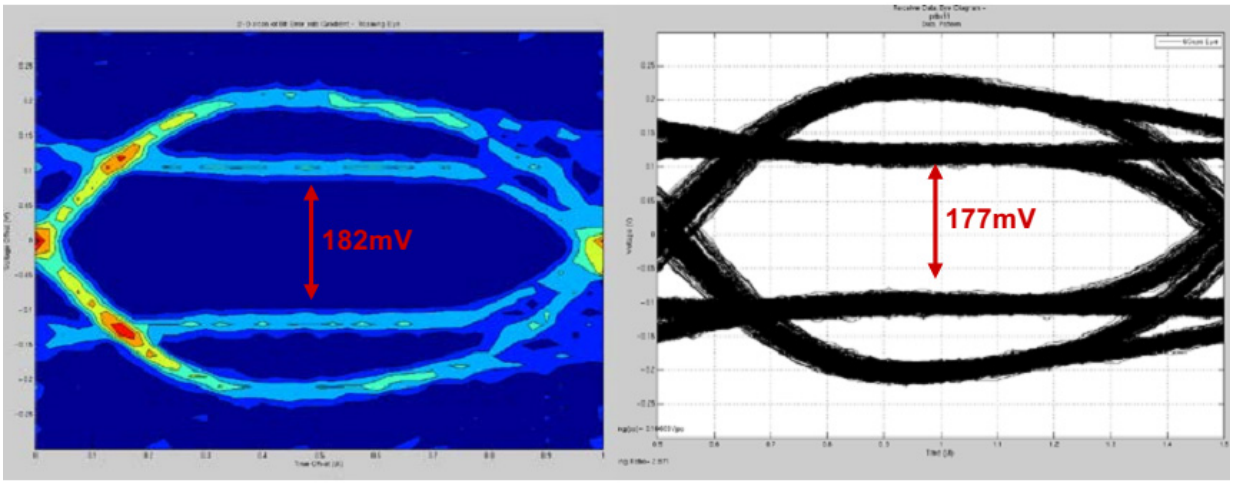
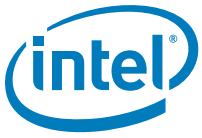


Figure 40. Left – Gradient of BER Plot, Right – Simulated Eye

For the x-offset (time), the offset can be set to address the full horizontal eye opening; for the y-offset (amplitude), the offset can be set to address ±256mV.

X-offset (Time) - Resolution: 2ps ± 1ps, Range: 1UI

Y-offset (Amplitude) - Resolution: 4mV, Range: +/-256mV



8.7.2 Measurement Procedure

The on-chip eye measurement can be made either in a test environment where the PHY TX sends out test patterns that are looped back externally off-chip to the RX, or in a normal link environment where the RX is receiving data from the TX at the other end of the link.

To measure the on-chip eye:

1. RX serial data pattern is provided either directly through the RX pads or through the loop back of the TX serial output (one of the available patterns used in the BIST must be provided).

2. Setup the x/y-offset resolution, the number of bits to accumulate for each measurement point, and the color-coding scheme representing the number of errors accumulated.

3. Use the AHB interface to shift the y-offset and x-offset relative to the sampling clock.

4. For each shift, wait the amount of time needed to accumulate the number of bits specified and count the number of bit errors by reading the AHB register eye_scan_wait_len.

5. After all sweeps are done, post-process the data and display the eye.

8.7.3 Measurement procedure Pseudo-code

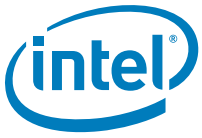
```
################################################################
## Pseudo code for Eye Monitor PCIe
################################################################


write (AHB block, Address, bits, Data)
read (AHB block, Address, bits)
TbusRead (TBUS block, address,bits)

EM Setup
# enabeling bist generator
Write (LANE,0x7,[5:5], 0x1);# bist_gen_cdn=1;
Write (LANE,0x7,[7:7], 0x1);# bist_gen_en=1;
Write (LANE,0xe,[6:6], 0x1); #Clear Rx BER counter;
Write (LANE,0xe,[5:5], 0x1);# enabeling bist CHECKER
#############################################
##      Step1 - Setup PMA for eye monitor mode
#############################################
Write (Lane,0x34,[0:1], 0x1);  #Msm_out_ovr_pd_vscan_dac[1:0] = 1
 Write (Lane,0x38,[2:3], 0x1); #Msm_out_ovr_rst_s2p_async[1:0] = 1
Write (Lane,0x63,[5:6], 0x1); #Pma_ln_rst_phd[0] = 1
Write (Lane,0x23,[6:7], 0x1); #Gcfsm_out_dr_slicer_vscan_ena270_ovr_o[1:0] = 1
Write (Lane,0x23,[4:5], 0x3); #Gcfsm_out_dr_slicer_vscan_en90_ovr=1->3
Write (Lane,0x65,[5:5], 0x1); #Pma_ln_dr_eye_ena90=1
Write (Lane,0x28,[0:0], 0x1); #Gcfsm_out_dr_vscan_ovr_o=1
Write (Lane,0x28,[1:7], 0x0); #Gcfsm_out_dr_vscan_ovr_o[7:1] = Desired Values
Write (Lane,0x64,[7:7], 0x0); #[7] pma_ln_dr_eye_dly_o[8:7] = Desired Values
Write (Lane,0x65,[0:0], 0x1); [8] pma_ln_dr_eye_dly_o[8:7] = Desired Values
If( Gen==1)
Write (Lane,0x57,[0:1], 0x1);
End
If( Gen==2)
Write (Lane,0x57,[0:1], 0x0);
End
If( Gen==3)
Write (Lane,0x6a,[0:1], 0x0);
End
Write (Lane,0x64,[0:6], 0x0); #pma_ln_dr_eye_dly_o[6:0] = Desired Values


#################################################
##      Step2 - Setup Eye monitor Digital logic
#################################################
```

```
Write (COMLANE,0x31,[0:0], 0x1); #Eye_scan_counter_en_o = 1
Write (COMLANE,0x35,[0:7], 0x7f); #Eye_scan_wait_len
Write (COMLANE,0x36,[0:3], 0x0); #Eye_scan_wait_len
Write (COMLANE,0x31,[2:2], 0x1); #Eye_scan_shift_en
Write (COMLANE,0x31,[3:3], 0x0); #Eye_scan_shift_dir
Write (COMLANE,0x31,[4:4], 0x0); #Eye_scan_shift_2bits
If( Gen==1)
Write (COMLANE,0x31,[4:4], 0x1);
End
Write (COMLANE,0x32,[0:7], 0xf7); #Eye_scan_mask
Write (COMLANE,0x33,[0:7], 0xff); #Eye_scan_mask
Write (COMLANE,0x34,[0:2], 0x7); #Eye_scan_mask


EM Capture
For Y=0:127
Write (LANE,0x28,[1:7], 2*Y); #writes VSCAN offset
For X=0:127
        Write (LANE, 0x64,[0:6], X);# writes delay line value to be used for this instance of the eye monitor sweep
        Write (COMLANE,0x31,[1:1], 0x1); #enable eye scan run
          Chkbit=TbusRead(LANE,0x8d,[8,8]); # Check that bit [8] eye_scan_cntr_ready_i = 1'b1
          while ( Chkbit!=1)
                  Chkbit=TbusRead(LANE,0x8d,[8,8]); # Check that bit [8] eye_scan_cntr_ready_i = 1'b1
          End
#Read Error count out of test bus.  Typically this is recorded into a text file with X-location, y-location and error count
          BER1= TbusRead(LANE,0x19,[0,11]);
BER2= TbusRead(LANE,0x1a,[8,11]);
BER=BER1|BER2
Write (COMLANE,0x31,[1:1], 0x0); #enable eye scan run
End
End


EM Return
Write (COMLANE,0x31,[0:0], 0x0); #Eye_scan_counter_en_o
Write (LANE,0x28,[0:0], 0x0); #Gcfsm_out_dr_vscan_ovr_o
Write (LANE,0x23,[4:5], 0x0); #Gcfsm_out_dr_slicer_vscan_en90_ovr
Write (LANE,0x23,[6:7], 0x0); #Gcfsm_out_dr_slicer_vscan_ena270_ovr_o
Write (LANE,0x6a,[0:1], 0x0); #Pma_ln_sr_slicer_edge_by_gen3_o
Write (LANE,0x57,[0:1], 0x0); #Pma_ln_sr_slicer_edge
Write (LANE,0x65,[5:5], 0x0); #Pma_ln_dr_eye_ena90
Write (LANE,0x63,[5:6], 0x0); #Pma_ln_rst_phd
Write (LANE,0x38,[2:3], 0x0); #Msm_out_ovr_rst_s2p_async[1:0]
Write (LANE,0x34,[0:1], 0x0); #Msm_out_ovr_pd_vscan_dac[1:0]
```

8.8 Display Port Phy Configuration section

The DP phy config NVM section is located at the beginning of the DP phy controller dram section, after the 2 size bytes. It holds phy configurations for SNK1 and SRC1, as described in the table below. Note that the offsets are in Bytes.

Byte Offset	Field Name	Description	Default
DP_PHY_DRAM_SECTION			
15:0	Header	holds a string to allow easy identification in the image	DP_PHY_SECTION
16:00	Reserved		



Byte Offset	Field Name	Description	Default
17	SNK1_SRC1_lane_np_swap	[0] - SNK1_Rx0 NP swap [1] - SNK1_DRx0 NP swap [2] - SNK1_DRx1 NP swap [3] - SNK1_Rx1 NP swap [4] - SRC1_DTx0 NP swap [5] - SRC1_Tx0 NP swap [6] - SRC1_Tx1 NP swap [7] - SRC1_DTx1 NP swap	0x00
18	Reserved		
19	Reserved		

8.9 Display Port Phy Eye Monitor

The Display Port phy eye monitor is activated in the same way as in CIO (Please refer to Section 8.10.6.1, "CIO Eye Monitor activation flow" on page 462).

Note: The target configuration space is Device Space (0x2) and the port being accessed is 0 or 1 (port A or B respectively).

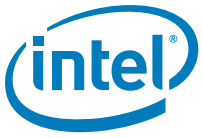
8.10 CIO Phy

8.10.1 CIO Phy NVM Configuration section

The cio phy config NVM section is located at beginning of the cio phy controller dram section, after the 2 size bytes. It holds phy configurations for PA and PB, as described in the table below. Note that the offsets are in Bytes.

Byte Offset	Field Name	Description	Default
PHY_DRAM_SECTION			
15:0	Header	holds a string to allow easy identification in the image	CIO_PHY_SECTION
16	PA_PB_lane_np_swap	[0] - PA_Rx0 NP swap [1] - PA_Tx0 NP swap [2] - PA_Tx1 NP swap [3] - PA_Rx1 NP swap [4] - PB_Rx0 NP swap [5] - PB_Tx0 NP swap [6] - PB_Tx1 NP swap [7] - PB_Rx1 NP swap	0x00
17	Reserved		

Byte Offset	Field Name	Description	Default
18	Reserved		
19	Reserved		
Port A Primary Tx FFE			
21:20	PA default_txffe_cio_20g_active_index[lane]	Default preset for a 20Gbps cio link when connected to an active cable. Byte per lane	0x0101
23:22	PA default_txffe_cio_20g_passive_index[lane]	Default preset for a 20Gbps cio link when connected to an active cable. Byte per lane	0x0101
25:24	PA default_txffe_cio_10g_active_index[lane]	Default preset for a 10Gbps cio link when connected to an active cable. Byte per lane	0x0101
27:26	PA default_txffe_cio_10g_passive_index[lane]	Default preset for a 10Gbps cio link when connected to an active cable. Byte per lane	0x0101
31:28	PA usb3_lfps_txffe[lane]	Txffe settings for usb3 during lfps. Word per lane [15..12] - tx_sw_post1 [11] - tx_sw_sel_pre1_post20 [10..3] - tx_sw_inv [2..0] - tx_sw_pre	0x0
35:32	PA usb3_gen1_txffe[lane]	Txffe settings for usb3 gen1. Word per lane [15..12] - tx_sw_post1 [11] - tx_sw_sel_pre1_post20 [10..3] - tx_sw_inv [2..0] - tx_sw_pre	0x48004800
39:36	PA usb3_gen2_txffe[lane]	Txffe settings for usb3 gen2. Word per lane [15..12] - tx_sw_post1 [11] - tx_sw_sel_pre1_post20 [10..3] - tx_sw_inv [2..0] - tx_sw_pre	0x38023802
47:40	Reserved		
Port B Primary Tx FFE			
49:48	PB default_txffe_cio_20g_active_index[lane]	Default preset for a 20Gbps cio link when connected to an active cable. Byte per lane	0x0101
51:50	PB default_txffe_cio_20g_passive_index[lane]	Default preset for a 20Gbps cio link when connected to an active cable. Byte per lane	0x0101



Byte Offset	Field Name	Description	Default
53:52	PB default_txffe_cio_10g_active_index[lane]	Default preset for a 10Gbps cio link when connected to an active cable. Byte per lane	0x0101
55:54	Default_txffe_cio_10g_passive_index[lane]	Default preset for a 10Gbps cio link when connected to a passive cable. Byte per lane	0x0101
59:56	PB usb3_lfps_txffe[lane]	Txffe settings for usb3 during lfps. Word per lane [15..12] - tx_sw_post1 [11] - tx_sw_sel_pre1_post20 [10..3] - tx_sw_inv [2..0] - tx_sw_pre	0x0
63:60	PB usb3_gen1_txffe[lane]	Txffe settings for usb3 gen1. Word per lane [15..12] - tx_sw_post1 [11] - tx_sw_sel_pre1_post20 [10..3] - tx_sw_inv [2..0] - tx_sw_pre	0x48004800
67:64	PB usb3_gen2_txffe[lane]	Txffe settings for usb3 gen2. Word per lane [15..12] - tx_sw_post1 [11] - tx_sw_sel_pre1_post20 [10..3] - tx_sw_inv [2..0] - tx_sw_pre	0x38023802
75:68	Reserved		

8.10.2 Transmitter Equalization (TXFFE)

8.10.2.1 Introduction

Titan Ridge DD transmitters at PA, PB and SRC0 share the same transmitter equalization structure, as shown in the figure below

Each transmitter consists of 7 drivers of different weights. Total weight of all drivers (full swing) is 22.

Three drivers (of weight 1, 2, 4) can be configured to drive either the main tap, pre-tap or post2 tap (controlled by tx_sw_pre[2:0]).

Four drivers (of weight 1, 2, 4, 8) can be configured to drive either the main tap or the post1 tap (controlled by tx_sw_post[3:0])

Any driver can also be configured to driver the opposite value (tx_sw_inv[6:0]).

Example A: Full swing - C0=1 (22/22):

- tx_sw_pre= 3'b0

- tx_sw_post= 4'b0
- tx_sw_inv= 7'b0

Example B: C-1=-0.09 (-2/22), C0=0.77 (17/22), C1=-0.14 (-3/22):

- tx_sw_pre= 3'b010
- tx_sw_post= 4'b0011
- tx_sw_inv= 7'b0

Example C: Low swing configuration, with post2: C0=0.68 (15/22), C1=-0.09 (-2/22), C2=-0.05(-1/22):

- tx_sw_pre= 3'b001
- tx_sw_post= 4'b0010
- tx_sw_inv= 7'b0000010

8.10.2.2 CIO TXFFE Setup

Titan Ridge DD implements the CIO TXFFE presets table as defined in the TBT Interconnect Specification.

The default TXFFE preset can be configured in NVM (see cio phy NVM configuration), per connection type - 20Gbps, 10Gbps active or 10Gbps passive.

8.10.2.3 USB TXFFE Setup

Titan Ridge DD implements the USB TXFFE settings as defined in the USB Spec. The TXFFE settings are read from NVM, and can be modified per usb3 gen1 or gen2 (see cio phy NVM configuration section).

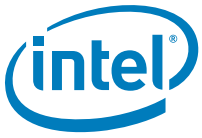
8.10.2.4 TXFFE Setup for DFT

User may change the TXFFE settings on-the-fly by directly modifying the per_lane.tx_ctrl_swing register once the transmitter is active. The settings may be overwritten upon enabling of the transmitter (reset to the NVM configuration), or upon partner request (CIO only).

8.10.3 Lane Swap Considerations

8.10.4 PRBS configuration

The sections below describe the procedure for enabling/disabling PRBS on PA/PB for CIO testing.



8.10.4.1 Enabling PRBS at the Transmitter

The following steps are required in order to transmit PRBS on PA/PB.

Note that some of the commands are per port and others are per lane. Repeat the commands as required.

1. Set the port to CIO mode with the required speed. Unless done externally, use the following LC registers (in this order):
   — Set LC.SW_FW_MAILBOX_IN.debug_halt_fw = 1'b1
   — Set LC.LINK_MODE.lc_cio_speed (1'b0 for 10G, 1'b1 for 20G)
   — Set LC.LINK_MODE.lc_cio_mode = 1'b1

Wait for per_port.common_lc_link_mode.phy_port_init_done == 1'b1

2. Enable the required lane transmitter. Unless done externally, use the following LC register:
   — Set LC.PHY_RX_TX_EN_REG.fw_en_tx_phy_l0/1 = 1'b1
   — Wait for per_lane.TX_CTRL.tx_is_active == 1'b1
3. Select the PRBS pattern to transmit by setting per_lane.TX_DFT_CTRL.dft_tx_prbs_sel
4. Enable the PRBS by setting per_lane.TX_DFT_CTRL.dft_en_tx_prbs = 1'b1
5. Disable the PRBS when done, by setting per_lane.TX_DFT_CTRL.dft_en_tx_prbs = 1'b0
6. Release the LC registers if needed, in the opposite order

8.10.4.2 Enabling the PRBS Checker at the Receiver

The following steps are required in order to check the received PRBS on PA/PB.

Note that some of the commands are per port and others are per lane. Repeat the commands as required.

1. Set the port to CIO mode with the required speed. Unless done externally, use the following LC registers (in this order):
   — Set LC.SW_FW_MAILBOX_IN.debug_halt_fw = 1'b1
   — Set LC.LINK_MODE.lc_cio_speed (1'b0 for 10G, 1'b1 for 20G)
   — Set LC.LINK_MODE.lc_cio_mode = 1'b1.

Wait for per_port.common_lc_link_mode.phy_port_init_done == 1'b1.

2. Make sure there is valid high speed data and enable the required receiver lane. Unless done externally, use the following LC register:
   — Set LC.PHY_RX_TX_EN_REG.fw_en_rx_phy_l0/1 = 1'b1
   — Wait for per_lane.CAR_CTRL.rx_eq_done == 1'b1
3. Select the PRBS pattern to compare by setting per_lane.RX_DFT_CTRL.dft_rx_prbs_sel
4. Enable the PRBS checker by setting per_lane.RX_DFT_CTRL.dft_en_rx_prbs = 1'b1

Verify that per_lane.RX_DFT_STATUS.dft_rx_prbs_ber_lock == 1'b1

5. Clear the error and symbol counters by setting per_lane.RX_DFT_CTRL.rx_ber_counter_clr = 1'b1
6. Enable the error and symbol counters by setting per_lane.RX_DFT_CTRL.rx_ber_counter_en = 1'b1

7. Stop the error and symbol counters after the required test time, by setting per_lane.RX_DFT_CTRL.rx_ber_counter_en = 1'b0
8. Verify that per_lane.RX_DFT_SYMBOL_COUNTER_HIGH/LOW match the test time
9. Read BER counter from per_lane.RX_DFT_BER_COUNTER.ber_cntr
10. Release the LC registers if needed, in the opposite order

8.10.5 PA/PB Rx Eye Quality

Once the lock process is completed (per_lane.CAR_CTRL.rx_eq_done == 1'b1), the width of the equalized eye is available.

The eye opening in percentage is given by 100*(Width)/(Steps_per_UI).

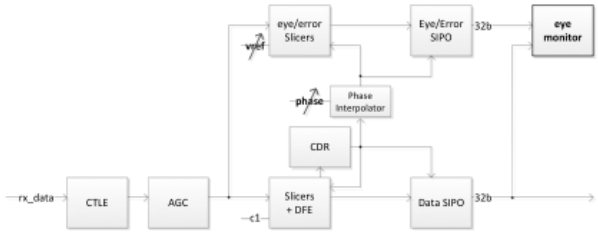
Width (measured in PI Steps) can be read from per_lane.LANE_MM4.best_eye_width.

Steps_per_UI can be obtained from the table below.

Mode	Speed (Gbps)	Steps per UI [PI steps]
CIO	20.625	64
CIO	10.3125	128
USB	10.0	128
USB	5.0	256

8.10.6 CIO Eye Monitor

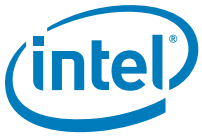
The PA/PB main Rx phy modules are shown the image below.



The eye monitor is used to sample the input signal after applying CTLE and AGC corrections. It does not monitor the eye after DFE, though it is capable of representing such eye diagrams.

The eye monitor slicers sample the signal at a predefined location. It then compares the sampled values to the main data stream decisions, and counts the errors.

The eye monitor uses dedicated slicers, therefore it can be used without affecting the main data stream (assuming it's used for limited periods and/or work conditions are kept the same). There are two slicers dedicated for the eye monitor, one sampling odd bits and the other sampling even bits. The slicers have separate voltage reference controls, though typically both should be set to the same value.



The eye monitor is also used for functional tasks during the lock stage and afterwards, thus it is needed to request control before using it and to properly release it when done. Note that the eye monitor is useless unless the rx CDR is locked.

The eye monitor sampling point can be moved vertically in both directions, by changing the voltage reference of the related slicers. The vertical resolution is ~2.36mv differential, with a total of 256 steps.

The sample point can also be moved horizontally in both directions. The step size for CIO / USB modes is ~0.76ps / ~0.78ps respectively. For CIO 20Gbps each UI is 64 steps. For CIO or USB at 10Gbps each UI is 128 steps. For USB 5Gbps, each UI is 256 steps.

8.10.6.1 CIO Eye Monitor activation flow

The following steps are required to enable the eye monitor:

1. Make sure rx CDR is locked - verify per_lane.CAR_CTRL.rx_eq_done == 1'b1
2. Request control for the eye monitor, by setting the sw_fw eyemon_request_control command in per_lane.SW_FW_MAILBOX (command 0x2). Wait for ack
3. Read the current horizontal position at per_lane.EYEMON_ANA.pi_phase_monitor. Keep this value, as it must be restored before releasing the eye monitor.
4. Position the eye monitor:
   - Horizontal - by default, the eye monitor position is near the middle of the eye. Move the required number of steps by issuing a sw_fw eyemon_move_horizontal command, 0x4. Wait for ack
5. Run eye monitor, by setting per_lane.SW_FW_MAILBOX:
   - Set symbol count bits[19:0]
   - FW command 0x7
   - Wait for ack
6. The vertical results vector is divided to 4 banks of registers arranged top down with a total of 255 steps. To Read the results:
   - read target offset 0xAF0-0xAFF, each DW contains 4 bytes of error counts out of the 1st quarter of positive steps location. [0xAF0:127- 0xAFF:64]
   - read target offset 0xCF0-0xBFF, each DW contains 4 bytes of error counts out of the 2nd quarter of positive steps location. [0xBF0:63- 0xBFF:0]
   - read target offset 0xCF0-0xCFF, each DW contains 4 bytes of error counts out of the 3rd quarter of negative steps location. [0xCF0:0- 0xCFF:(-63)]
   - read target offset 0xDF0-0xDFF, each DW contains 4 bytes of error counts out of the 4th quarter of negative steps location. [0xDF0:(-64)- 0xDFF:(-127)]
7. For next horizontal step, repeat from Step 4
8. When completed:
   - Move the eye monitor to its original horizontal position by issuing the sw_fw eyemon_move_horizontal command, as required. Do NOT wrap around to get back to position - the total number of steps moved left must be equal to the total number of steps moved right. Verify that the horizontal location (per_lane.EYEMON_ANA.pi_phase_monitor) is equal to what it originally was.
9. Release the eyemon by issuing a sw_fw eyemon_release_control command, 0x3. Wait for ACK

Note: The target configuration space is Device Space (0x2) and the port being accessed is 0 or 1 (port A or B respectively).

8.10.7 CIO Phy SW FW Mailboxes

Each cio phy port and each lane have a sw_fw_mailbox register used for various SW interactions.

The mailboxes are located at the first memory mapped offset of each section.

The most significant byte (sw_fw_mailbox[31:24]) holds the command and the rest of the mailbox (sw_fw_mailbox[23:0]) is used for arguments.

Unless stated otherwise, when FW completes a command, it clears the command field (sw_fw_mailbox[31:24]).

8.10.7.1 Per port sw_fw_mailbox:

The table below lists the supported commands for the per_port.SW_FW_MAILBOX:

Command Name	Description	Command Encoding [31:24]	Arguments [23:0]
port_controller_halt	Halt the FW, for debug. This command is not cleared by FW. It is acknowledged by FW clearing of bit 0. Command field should be cleared by SW in order to release.		[0] - SW should set this bit when issuing the command. FW will clear it when halted

8.10.7.2 Per lane sw_fw_mailbox:

The table below lists the supported commands for the per_lane.SW_FW_MAILBOX:

Command Name	Description	Command Encoding [31:24]	Arguments [23:0]
eyemon_request_control	Request control for the eyemon logic	0x02	
eyemon_release_control	Release the eyemon logic	0x03	
eyemon_move_horizontal	Move the eyemon horizontally	0x04	[8] - 0 Move left, 1 Move right [7:0] number of steps to move
Eyemon_dump_eye_height	Dumps error counter vertical vector of current eyemonitor location	0x07	[19:0] - symbols count [23:20] - mask type

8.11 CIO Bandwidth Monitoring

CIO Bandwidth Monitoring is a DFT feature that allows measuring bandwidth of traffic within the CIO Ports.

The bandwidth monitoring is controlled from a Control Port Register (Device Configuration Space), see Table 24, "DFT Vendor-Specific Capability Register Attributes" on page 107

- DFT7[0] - BW_CNT_EN - When this bit set, bandwidth counters in all CIO protocol adapters are enabled
- DFT7[2:1] - BW_CNT_PERIOD - This field select the time period for the bandwidth measurement (0 - 1sec, 1 - 2sec, 2 - 4sec, 3 - 8sec)

Once enabled, all protocol adapters enable two counters to start counting the amount of bytes that traverse to each of the directions (Egress/Ingress). Bandwidth measuring counters are 36 bits wide. Once the count period elapses the counter's values are loaded into two registers that capture Egress/ Ingress bandwidth. Registers are 32 bits, and reflect bits [35:4] of the counter (the value in the register is in Quad DW / 16 Bytes granularity). After the load, the protocol adapters reset these two counters and starts the next count period (the results are loaded at the end of each period). All protocol adapters do this simultaneously by getting the same strobe at the end of each period. This ensures results between different protocol adapters are reflecting captures of the same time period.

In each protocol adapter there are two counters/registers which are located after the existing counters. The first counter is Tx-Egress and the second counter is Rx-Ingress (see Table 65, "Counters Configuration Register Attributes" on page 299).

8.12 Titan Ridge I2C Master Protocol

Titan Ridge communicates as an I2C master with a PD Controller as an I2C slave. As I2C master it operates at Fast mode (400KHz) speed.

Titan Ridge I2C master does not support a multi-master environment. Titan Ridge supports clock stretching. The PD Controller addresses are predefined as follows:

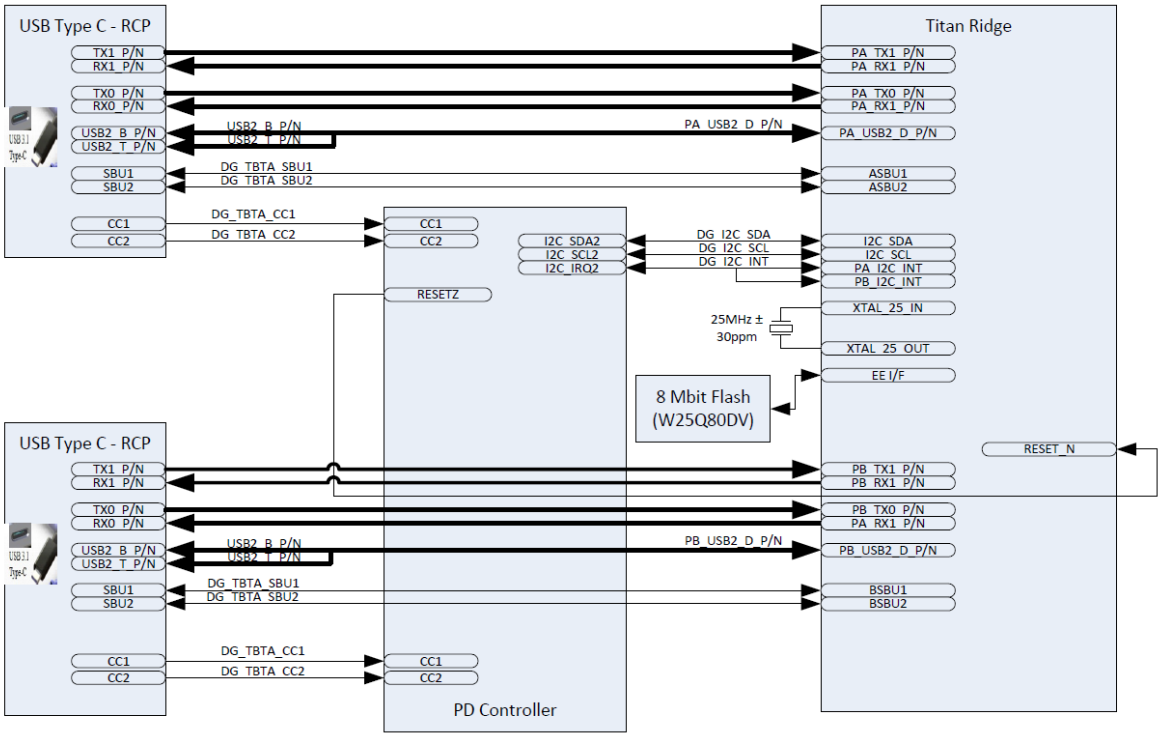
- 0x38 (8 bit 0x71/0) shall be used for the primary PD Controller connected to Titan Ridge Port A
- 0x3F (8 bit 0x7F/E) shall be used for the secondary PD Controller connected to Titan Ridge Port B

The PD Controller shall have an open-drain output to interrupt Titan Ridge. Upon cable connection, or status change, the interrupt line shall be held low by the PD Controller. The interrupt line shall be held low until cleared by Titan Ridge writing the I2C_INT_ACK bit in the Data Control register, Table 447. A PD Controller with two ports or two PD controllers may wire OR the two interrupts.

Titan Ridge is a level triggered interrupt. Titan Ridge acknowledges the Interrupt by updating the Data Control register, Table 447. The Data Control register shall be monitored by the PD Controller for changes. Titan Ridge may update the Data Control register without an Interrupt from the PD Controller.

The connections between Titan Ridge as I2C Master and the PD controller and a Host are shown in Figure 41.

Figure 41. Dual Port Titan Ridge to PD Controller Connection



8.12.1 Register read/write flow via I2C

The I2C Interface transaction layer implements register access. The Sub-address phase of the I2C write is used to provide the register number to be accessed. The remaining data provided during the write phase is used to write data to the selected register. The following read phase is used to read data from the selected register. A transaction shall either read or write, but shall not attempt both at the same time.

A write transaction consists of the following:

- 1st byte: USB PD Controller slave address with the R/W' bit cleared
- 2nd byte: register address
- 3rd byte: byte count N. The USB PD Controller should ignore this byte and act on the actual number of bytes sent
- 4th to (N+3): N data bytes
- Stop bit

A read transaction consists of the following:

- 1st byte: USB PD Controller slave address with the R/W' bit cleared.
- 2nd byte: register address
- Repeated start
- 3rd byte: USB PD Controller slave address with the R/W' bit set.
- 4th byte: 1st response byte from USB PD Controller - register size

- 5th byte: until Titan Ridge sends the stop bit: response from USB PD Controller - register data bytes LSB first. If the register size is smaller than the amount of data bytes attempted to read, return either 0x00 or 0xFF for the remaining bytes.

8.12.2 Titan Ridge Data Control Register

Titan Ridge uses the 4-byte Data Control register, Table 447, at address 0x50 to communicate with the PD Controller when in I2C master mode. The PD Controller asserts the Interrupt low on any change to the Data Status Register, Table 448. Titan Ridge acknowledges the Interrupt by writing to the Data Control Register I2C_INT_ACK. This bit should be implemented as self-clear. Any change that happens after the initial interrupt but before writing this bit may cause interrupt re-assertion.

In a two port Thunderbolt Device, the first connected port communicates a Host connection to the second port. This allows the second port to configure its capabilities based on the type of Host connected on the first port.

Table 447. Data Control Register Description (Address 0x50 for I2C Master, RO)

Bit Number	Name	Description	Comments
0	TBT_Host_Connected	0 – No Thunderbolt Host connected upstream 1- Thunderbolt Host Connected	Device Only: Indication to a downstream port a TBT Host is connected upstream.
1	Reserved	0	Must be set to 0.
2	I2C_INT_ACK	0 - Do Nothing 1 – Titan Ridge acknowledge for the interrupt	Host or Device: Set by Titan Ridge when in I2C master Mode. Not used when Titan Ridge is in I2C Slave Mode.
3	Reserved	0	Must be set to 0.
4	USB_Host_Connected	0 - No USB Host connected upstream 1 - USB Host connected upstream	Device Only: Indication to a downstream port a USB Host is connected upstream. (not a TBT Host).
5	DP_Host_Connected	0 - No DP Host connected upstream 1 - DP Host connected upstream	Device Only: Indication to a downstream port a DP Alt Mode Host is connected upstream. If DP multi-function with USB, also set USB_Host_Connected. Only valid for a TBT Device.
[13:6]	Reserved	0	
13	IRQ_ACKfmTR	0 - No IRQ_ACK 1 - HPD_IRQ_ACK	Host Only: Titan Ridge sets IRQ_ACKfmTR=1 in response to DataStatus.IRQ_HPD_StickyfmPD=1. Titan Ridge sets IRQ_ACKfmTR =0 in response to DataStatus.IRQ_HPD_StickyfmPD=0.

Table 447. Data Control Register Description (Address 0x50 for I2C Master, RO)

Bit Number	Name	Description	Comments
14	IRQ_HPDStickyfmTR	0 - No IRQ HPD 1- IRQ HPD Device may only set IRQ_HPD=1 when also setting HPD_LVL=1	Device Only: Titan Ridge sets IRQ_HPDStickyfmTR=1 in response to receiving a hardware IRQ HPD signal from a connected DP Sink. Titan Ridge sets IRQ_HPDStickyfmTR=0 in response to receiving a DataStatus.IRQ_ACKfmPD=1. Titan Ridge shall not set IRQ_HPDStickyfmTR=1 again until it has written an IRQ_HPDStickyfmTR=0. The PD Controller shall queue the IRQ_HPDStickyfmTR only on a 0 to 1 transition.
15	HPD_LVLfmTR	0 - HPD pin Low 1 - HPD pin High	Device Only: Titan Ridge sets HPD_LVLfmTR in response to receiving a hardware HPD high or low signal from a connected DP Sink.
[31:16]	Reserved	0	

8.12.3 Titan Ridge Data Status Register

Titan Ridge determines its operating mode by reading the Data Status register, Table 448, after seeing an Interrupt from the PD Controller. The Data Status register is a 4-byte register, RO, starting at address 0x5F.

Titan Ridge reads the Data Status register and then clears the Interrupt in the Data Control register, Table 447, to avoid missing status changes.

Table 448. Data Status Register

Bit Number	Name	Description	Comments
0	Data_connection_present	0 – no connection present. Other bits in this register should be ignored. 1 – connection present. Connection type defined by other bits in this register[1,2]	
1	Connection_orientation	0 – normal. PD communication on CC1 line 1 – reversed. PD communication on CC2 line	
2	Active_cable	0 – Passive cable[1] 1 – TBT Active cable From DFP SOP TBT Enter Mode VDO B22	
3	OverCurrentorTemp	0 - An over-current/over-temperature event has not occurred[1,2] 1 – An over-current/over temperature event has occurred	Used for xHCI controller to present over current event.
4	Usb_2_connection	0 – No USB2 connection 1- USB2 connection. Can be in the TBT Mode with a USB2 connection to read the billboard[1]	Titan Ridge will determine if USB2 is xHCI or external path in a TBT device

Table 448. Data Status Register

Bit Number	Name	Description	Comments
5	Usb_3_connection	0 – No USB3.1 connection[2] 1 – USB3.1 connected[1]	
6	Usb_3_speed	0 – USB3.1 is limited to gen1 (5G only)[2] 1 – USB3.1 gen1/2 supported (5G/10G)	From Cable USB PD response. Ignored for TBT and DP
7	USB_Data_Role	0 – DFP (connects the internal xHCI) 1 - UFP (sets the USB3.1 passthru to the side port)	Ignored for TBT and DP
8	Dp_connection	0 – No DP connection[1,2] 1 – DP connected	
9	Dp_source_sink	0 – DP Source connection requested[1,2] 1 – DP Sink connection requested	
[11:10]	Dp_pin_assignment	00 – Pin assignments E/E'/F/F'[1,2] 01 – Pin assignments C/C'/C/C' 10 – Pin assignments A/A'/B/B' 11 – reserved	
12	Debug_Accessory_Mode	0 - Not in Debug Mode 1 - In Debug Accessory Mode	USB Type-C Debug accessory mode Set USB3 and USB2 if this is set
13	IRQ_ACKfmPD	0 - No IRQ GoodCRC Received 1 - IRQ GoodCRC Received	Device Only: Set after receiving GoodCRC from USB PD Attention message with IRQ_HPD.
14	IRQ_HPDStickyfmPD	0 - No IRQ_HPD 1 - IRQ_HPD received	Host Only: DPStatusVDO.IRQ_HPD from USB PD
15	HPD_LVLfmPD	0 - HPD_State Low 1 - HPD_State High	Host Only: DPStatusVDO.HPD_State from USB PD
16	Tbt_connection	0 – TBT not configured[1] 1 – TBT configured[2]	Host and Device
17	Tbt_type	0 – Type-C to Type-C Cable[1] 1 – Type-C Legacy TBT Adapter From DFP SOP TBT Enter Mode VDO B22	Host and Device
18	Cable Type	0 – Electrical Cable[1] 1 – Optical Cable From DFP SOP TBT Enter Mode VDO B21	Host and Device
19	VPro_Enabled	0 - No vPro Dock enabled 1 - vPro Dock enabled	Just reporting of vPro Support. No action.
20	TBT Active Link Training	0b – Active with bi-directional LSRX communication[1] 1b – Active with uni-directional LSRX communication From DFP SOP TBT Enter Mode VDO B25	Host and Device: Passive cable shall set to 0b
21	Debug_Alt_Mode_Connection	0 - Not in NIDnT Debug Alt mode 1 - NIDnT Debug Alt mode	NIDnT Alt mode defined in MIPI SVID = 0xFF03
22	Reserved	0	

Table 448. Data Status Register

Bit Number	Name	Description	Comments
23	Force_lsx	0 – Normal operation[1,2] 1 – Force LSTX/RX connection regardless of TBT connection state	Host and Device: Force a Host Connection. Used for debug only
24	Power Mismatch	0 - No USB PD power mismatch 1 - USB PD power mismatch. Not enough power for S0	Host and Device: Used only in TBT BPD
[27..25]	TBT_Cable_Speed_support	000b - No Functionality 001b - USB3.1 gen1 cable (Titan Ridge will function at 10Gb/s) 010b - 10Gb/s 011b -10Gb/s and 20Gb/s From DFP SOP TBT Enter Mode VDO B18..16	Host and Device: TBT only
[29..28]	TBT_Cable_Gen	00b - 3rd generation TBT (10.3125 and 20.625Gb/s)1,2 01b - 4th generation TBT (10.0, 10.3125, 20.0, 20.625) 10..11b - Reserved From DFP SOP TBT Enter Mode VDO B20..19	Host and Device: TBT only
30	Reserved	0	
31	Reserved	0	

Note: 1. Default at Initial cable connection for USB functionality; 2. Thunderbolt Operation

8.13 Titan Ridge I2C Slave Protocol

A write transaction consists of the following:

- 1st byte: DBR/BB port slave address with the R/W' bit cleared
- 2nd byte: register address
- 3rd byte: byte count N. DBR ignores this byte and acts on the actual byte count, up to the register's size.
- 4th to (N+3): N data bytes. Data bytes exceeding the implemented register size (4) shall be discarded

A read transaction consists of the following:

- 1st byte: DBR/BB port slave address with the R/W' bit cleared.
- 2nd byte: register address
- Repeated start
- 3rd byte: DBR/BB port slave address with the R/W' bit set.
- 4th byte: 1st response byte from DBR/BB port - register size. This is always the register's size. The master may read less (or more- in this case it will get 00's in the additional bytes).
- 5th byte until I2C master sends the stop bit: response from DBR/BB port slave - register data bytes LSB first. If the amount of data bytes attempted to read is greater that the implemented registers size (4), return 0x00 for the remaining bytes.

8.13.1 Slave Specific Registers

Titan Ridge I2C slave implements three copies of the slave register sets with each set assigned to a unique I2C address (might be required to be consecutive addresses). The address is a combination of NVM and hardware straps. The addresses can be configured to any address without dependency between chips sharing the flash. The address will be selected by the strap between two distinct NVM field values.

All registers in the set are 4 bytes in size. Registers will be mapped to target space to allow internal firmware to set or read the values.

Table 449. Titan Ridge I2C Slave Register Set

Register number	Name	I2C Slave Register Type (with respect to Titan Ridge)
0	Vendor ID	Read Only
1	Device ID	Read Only
2	Tar Data	Read/Write
3	Tar Command	Read/Write
4	Connection State	Read/Write
5	TBT Status	Read Only
6	Reserved	Read/Write
7	Debug Alternate Mode	Read/Write

8.13.2 I2C Slave Mode Behavior

Titan Ridge is directed to an operating mode by the embedded controller, EC, writing to the Connection State register, Table 450. Titan Ridge shall read this register to determine its operating mode.

Titan Ridge is expected to assert the Interrupt on any change to the TBT Status Register, Table 451. Titan Ridge is expected to de-assert the Interrupt when the Interrupt_Ack bit in the Connection State register, Table 450, is written by the EC. Any TBT Status register change which occurs after the initial interrupt but before writing Interrupt_Ack may cause an interrupt re-assertion.

Table 450. Connection State Register (Address 0x04 for I2C Slave, RW)

Bit Number	Name	Description	Comments
0	Data_connection_present	0 – no connection present. Other bits in this register should be ignored. 1 – connection present. Connection type defined by other bits in this register[1,2]	
1	Connection_orientation	0 – normal. 1 – reversed.	Used for indicating cable orientation to retimer.
2	Active_cable	0 – Passive cable[1] 1 – TBT Active cable From DFP SOP TBT Enter Mode VDO B22	

Table 450. Connection State Register (Address 0x04 for I2C Slave, RW)

Bit Number	Name	Description	Comments
3	OverCurrentorTemp	0 - An over-current/over-temperature event has not occurred[1,2] 1 – An over-current/overtemperature event has occurred	Used for xHCI controller to present over current event.
4	Usb_2_connection	0 – No USB2 connection 1 - USB2 connection. Can be in the TBT Mode with a USB2 connection to read the billboard[1]	Titan Ridge will determine if USB2 is xHCI or external path in a TBT device
5	Usb_3_connection	0 – No USB3.1 connection[2] 1 – USB3.1 connected[1]	
6	Usb_3_speed	0 – USB3.1 is limited to gen1 (5G only)[2] 1 – USB3.1 gen1/2 supported (5G/ 10G)	From Cable USB PD response Ignored for TBT and DP
7	USB_Data_Role	0 – DFP (connects the internal xHCI) 1 - UFP (sets the USB3.1 passthru to the side port)	Ignored for TBT and DP
8	Dp_connection	0 – No DP connection[1,2] 1 – DP connected	
9	Dp_source_sink	0 – DP Source connection requested[1,2] 1 – DP Sink connection requested	
[11:10]	Dp_pin_assignment	00 – Pin assignments C/C'/E/E'[1,2] 01 – Pin assignments D/D'/F/F' 10 – Pin assignments A/A'/B/B' 11 – reserved	
12	Debug_Accessory_Mode	0 - Not in Debug Mode 1 - In Debug Accessory Mode	USB Type-C Debug accessory mode Ignored by Titan Ridge
13	IRQ_ACKfmPD	0 - No IRQ GoodCRC Received 1 - IRQ GoodCRC Received	Device Only: Set after receiving GoodCRC from USB PD Attention message with IRQ_HPD.
14	IRQ_HPDStickyfmPD	0 - No IRQ_HPD 1 - IRQ_HPD received	Host Only: DPStatusVDO.IRQ_HPD from USB PD
15	HPD_LVLfmPD	0 - HPD_State Low 1 - HPD_State High	Host Only: DPStatusVDO.HPD_State from USB PD
16	Tbt_connection	0 – TBT not configured[1] 1 – TBT configured[2]	
17	Tbt_type	0 – Type-C to Type-C Cable[1] 1 – Type-C Legacy TBT Adapter From DFP SOP TBT Enter Mode VDO B22	
18	Cable Type	0 – Electrical Cable[1] 1 – Optical Cable From DFP SOP TBT Enter Mode VDO B21	
19	vPro_Dock_Detected	0 - No vPro Dock detected 1 - vPro Dock detected	CSME reads and decides which port has vPro.

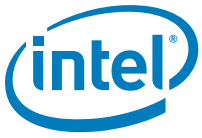


Table 450. Connection State Register (Address 0x04 for I2C Slave, RW)

Bit Number	Name	Description	Comments
20	TBT Active Link Training	0b – Active with bi-directional LSRX communication[1] 1b – Active with uni-directional LSRX communication From DFP SOP TBT Enter Mode VDO B25	Passive cable shall set to 0b
21	Debug_Alt_Mode_Connection	0 - Not in Intel Debug Alt mode 1 - Intel Debug Alt mode	Ignored by Titan Ridge
22	Debug_Alt _Mode_Type	0 - NIDnT 1 - IDO	Ignored by Titan Ridge
23	Force_lsx	0 – Normal operation[1,2] 1 – Force LSTX/RX connection regardless of TBT connection state	Force a Host Connection
24	S0_power_negotiated	0 - Sx power negotiated. Not enough power for S0 1 - S0 power negotiated (Hosts and SPD set to 1)	Used only in TBT BPD
[27..25]	TBT_Cable_Speed_support	000b - No Functionality 001b - USB3.1 gen1 cable (Titan Ridge will function at 10Gb/s) 010b - 10Gb/s 011b -10Gb/s and 20Gb/s From DFP SOP TBT Enter Mode VDO B18..16	TBT only
[29..28]	TBT_Cable_Gen	00b - 3rd generation TBT (10.3125 and 20.625Gb/s)[1,2] 01b - 4th generation TBT (10.0, 10.3125, 20.0, 20.625) 10..11b - Reserved From DFP SOP TBT Enter Mode VDO B20..19	TBT only
30	Reserved	0	
31	Interrupt_ACK	0 - Do Nothing 1 – EC acknowledge for the interrupt	Set by EC when in I2C slave Mode.

Table 451. TBT Status Register (Address 0x05 for I2C Slave, RW)

Bit Number	Name	Description	Comments
0	TBT_Host_Connected	0 – No Thunderbolt Host connected upstream 1- Thunderbolt Host Connected	Device Only: Indication to a downstream port a TBT Host is connected upstream.
1	Reserved	0	
2	Reserved	0	
3	InSafeState	0 - No in Safe State 1 - High speed in Safe State	Titan Ridge sets this after confirming high speed I/Os are in USB Type-C Safe State.

Table 451. TBT Status Register (Address 0x05 for I2C Slave, RW)

Bit Number	Name	Description	Comments
4	USB_Host_Connected	0 - No USB Host connected upstream 1 - USB Host connected upstream	Device Only: Indication to a downstream port a USB Host is connected upstream. (not a TBT Host).
5	DP_Host_Connected	0 - No DP Host connected upstream 1 - DP Host connected upstream	Device Only: Indication to a downstream port a DP Alt Mode Host is connected upstream. If DP multi-function with USB, also set USB_Host_Connected. Only valid for a TBT Device.
[13:6]	Reserved	0	
13	IRQ_ACKfmTR	0 - No IRQ 1 - IRQ	Host Only: Titan Ridge sets IRQ_ACKfmTR=1 in response to DataStatus.IRQ_HPD_StickyfmPD=1. Titan Ridge sets IRQ_ACKfmTR =0 in response to DataStatus.IRQ_HPD_StickyfmPD=0.
14	IRQ_HPDStickyfmTR	0 - No IRQ HPD 1- IRQ HPD Device may only set IRQ_HPD=1 when also setting HPD_LVL=1	Device Only: Titan Ridge sets IRQ_HPDStickyfmTR=1 in response to receiving a hardware IRQ HPD signal from a connected DP Sink. Titan Ridge sets IRQ_HPDStickyfmTR=0 in response to receiving a DataStatus.IRQ_ACKfmPD=1. Titan Ridge shall not set IRQ_HPDStickyfmTR=1 again until it has written an IRQ_HPDStickyfmTR=0. The PD Controller shall queue the IRQ_HPDStickyfmTR only on a 0 to 1 transition.
15	HPD_LVLfmTR	0 - HPD pin Low 1 - HPD pin High	Device Only: Titan Ridge sets HPD_LVLfmTR in response to receiving a hardware HPD high or low signal from a connected DP Sink.
[31:16]	Reserved	0	

Note: 1. Default at Initial cable connection for USB functionality; 2. Thunderbolt Operation

8.14 Display Port Type-C Pin Assignment

The mapping for the Display Port Type-C pin assignment is described in the table below.

Table 452. Display Port Type-C Pin Assignment

	DP (MFDP) Transmitter Normal	DP (MFDP) Transmitter Flip	DP (MFDP) Receiver Normal	DP (MFDP) Receiver Flip
ASSRX1	ML3 (USB)	ML0	ML2 (USB)	ML1
ASSTX1	ML2 (USB)	ML1	ML3 (USB)	ML0
ASSTX2	ML1	ML2 (USB)	ML0	ML3 (USB)
ASSRX2	ML0	ML3 (USB)	ML1	ML2 (USB)
BSSRX1	ML3 (USB)	ML0	ML2 (USB)	ML1
BSSTX1	ML2 (USB)	ML1	ML3 (USB)	ML0
BSSTX2	ML1	ML2 (USB)	ML0	ML3 (USB)
BSSRX2	ML0	ML3 (USB)	ML1	ML2 (USB)

8.15 Architectural Limitations

8.15.1 PCIE

PCIe peer-to-peer is not supported.

9.0 Testability

9.1 JTAG Test Active Point (TAP)

JTAG Test Active Point (TAP)

Titan Ridge JTAG TAP has a Main Tap (mTAP) with 8 bit Instruction register (IR) and some glue logic to connect to Legacy TAP of 6 bit IR. By default (after Power up) the mTAP is connected to JTAG pads of the Titan-Ridge device working with 8 bit IR.

Main TAP supports the following commands:

Public commands IEEE Std.1149.1 (used for BSDL testing):

BYPASS (11111111)

EXTEST (00001001)

EXTEST_PULSE (00001110)

SAMPLE (00000001)

PRELOAD (00000001)

IDCODE (00000010)

EXTEST_TRAIN (00001111)

User defined commands:

MTAP DISABLE (00110000), Shift DR one bit value 1'b1.

This command can be used to connect Legacy TAP to Titan Ridge JTAG pins. Once this command is completed, Titan Ridge JTAG is working in legacy mode with 6 bit IR, except public BSDL command.

The following procedure can be done by external JTAG agent to recognize Legacy Titan Ridge JTAG:

1. Apply MTAP DISABLE command.

2. Apply Legacy DEVID 6-bit command (010101) and Shift DR 16 bit value 0x0. Check received 16 bit data on TDO. If known 16-bit IDCODE recognized (Titan Ridge DD - 0x15EA), the corresponding chip is recognized and legacy 6-bit JTAG TAP is available.

End of procedure.

In this mode 6 bit IR should be used.

MTAP_NETWORK (00010010) Shift DR 16 bit value 16'h0001

This command used to Access legacy JTAG TAP (6-bit) via TAP network. Once this command is completed, each JTAG instruction has 14 bits length, first 6 bits relates to Legacy TAP and last 8'bFF bypass mTAP, also Data Register need additional 1 bit shifting. This mode used by Tenlira tool.

In this mode 14 bit IR should be used.

9.2 Boundary-Scan Description Language (BSDL) file

Chip supports BSDL and appropriate bsdl file can be provided to customer.

9.3 XOR tree

XOR tree chain:

Activation of XOR testing by JTAG command: set instruction register to 6'b101010

Toggle XOR inputs and sample GPIO_9.

TDF file is available and can be provided to customer.

9.4 Thermal Junction 1mA Curve

In order to measure the Tj (Junction Temperature) a thermal diode is implemented in Titan Ridge DD. See Figure 42.

A DMM should be used in the setup shown in Figure 43. The DMM should be connected using the jumper and the V8 ball for 10.7x10.7 (Titan Ridge DD).

Figure 42. Thermal Diode Implementation

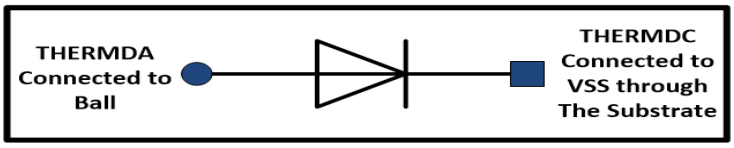
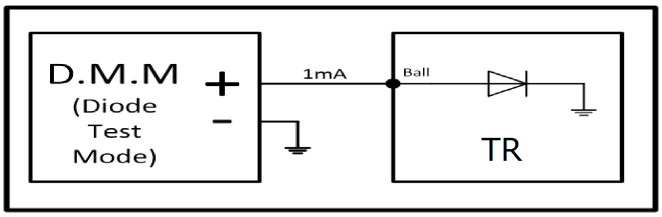


Figure 43. Tj Measurement Setup



9.5 Thermal Diode Equation for Titan Ridge DD

The following formula should be used to calculate Titan Ridge DD Tj temperature, assuming measurement current of 1mA:

Tj [Deg] = 517.42 – 642.17 * V [v]

Appendix A. External Connection Manager Guidelines

A.1. Sx Entry/ Exit Flow - Implementation Details

Registers relevant for Sx flow:

LC_SX_STATUS

See Table 31 for details.

LC_SX_CTRL

See Table 31 for details.

LC_SX_TIMERS

See Table 31 for details.

POC_MAILBOX (informative. Handled by LC)

[31:16] Reserved

[15] System state at power down: 0=S0, 1=Sx.

[14:12] State before Sx entry: 100 = downstream cio, 101 = upstream cio, 110 = interdomain cio, 010 = dpp, 000 = disconnected.

[11:9] Reserved

[8:0] Sx wake enables. Preserve the latest wake settings.

Connection Manager Responsibilities:

After Sending a Go2Sx Command through the PCIE2TBT Mailbox, CM should back-trace all switches within the domain from the leafs up to the HR (HR is last) and set LC_SX_CTRL[31] (other fields in this register should not be changed) in each of the LCs. CM should then wait for a Ok2Go2Sx approval from the TBT2PCIE Mailbox before proceeding with the Sx flow.

Upon every CIO Port plug event, after CIO enumeration of the plugged switch is complete, CM should set "plugged and configured" bit in respective LC_SX_CTRL[16]/[20] (depending on the port/lane) of both link ends (i.e. father and child switches). CM should also update "Port is upstream" for the upstream port. Upon every CIO Port unplug event, before CIO tunnels teardown of the un-plugged switch is complete, CM has to clear "plugged and configured" bit in respective LC_SX_CTRL[24]/[20] (depending on the port/lane) of both link ends (i.e. father and child switches), if accessible.

After starting the Sx flow, CM should not handle any plug/unplug events (until system is back to S0).

Interdomain considerations:

By default, a port entering Sx with an inter-domain link will be treated as a disconnected port, without any wake event. Titan Ridge DD will drive LSTX low in this case.

In order to allow an inter-domain link to enter Sx similar to a regular TBT link, SW should first disable the default functionality by clearing CHICKEN_BITS[5]. SW should also make sure not to enable any lsrx toggle related wake event on the inter-domain port, in order to avoid false wake of the topology.

The non sleeping partner must keep the interdomain plugged and configured bits set (despite the unplug events).

In order to wake the interdomain link, the non sleeping partner should simulate an unplug using SW_FW_MAILBOX_IN[6] (sw_force_lstx_low).

Upon Sx exit, if the interdomain partner is still sleeping, CM must reconfigure the interdomain plugged and configured bits (despite that there won't be any plug events).

A.1.1. A.3.4 Flash read through LC/IECS

Titan Ridge DD Flash read can be done through dedicated LC registers: LC_FLASH_ACCESS_DATA, LC_FLASH_ACCESS_CTRL. These registers are accessible either through target as two 32b registers, or through IECS as a single 64b register at offset 0x11.

Flash accesses through these registers are done in DWs (32b), to DW aligned addresses. To Read a DW, SW should set LC_FLASH_ACCESS_CTRL/byte_address, start1_done0. When the start1_done0 bit is cleared (by LC FW), read data is ready at LC_FLASH_ACCESS_DATA. SW must verify that the read_error indication is clear.

Flash access also supports up to 64B read operations, by setting LC_FLASH_ACCESS_CTRL/ data_register_select to 1 and LC_FLASH_ACCESS_CTRL/access_length to the required read length. MSG_OUT_RDATA is used as the read data buffer in this case. The rest of the read flow is as described above. Note that it is SW responsibility to ensure the accessed Flash supports such read bursts.

A.2. Accessing IECS Cmd/Data registers from SW

Several general purpose registers were assigned for communication between CM and LC:

SW_FW_MAILBOX_IN, SW_FW_MAILBOX_DATA_IN0..3 - are used for commands/data from CM to LC.

SW_FW_MAILBOX_OUT, SW_FW_MAILBOX_DATA_OUT0..3 - are used for commands/data from LC to CM.

Sending IECS commands from CM should be done through the SW_FW_MAILBOX, and not through direct access to the IECS register. The IECS register should be used only for UART access.

SW should write the IECS command to SW_FW_MAILBOX_DATA_IN0 and related data (if applicable) to SW_FW_MAILBOX_DATA_IN1..3. Then it should set SW_FW_MAILBOX_IN[0]. LC will clear this bit to indicate it received the command. Output data (if applicable) will be valid at SW_FW_MAILBOX_DATA_OUT0..3, once SW_FW_MAILBOX_DATA_IN0 (the command) is cleared.

A.3. Supported IECS Commands

The IECS Commands (4CC encoded) supported by Titan Ridge DD are listed in Table 453. Unless otherwise stated, the commands are supported though both IECS or SW_FW_MAILBOX.

Table 453. IECS Commands

Command	Description	Data
'Lnk0'	disable both lanes	NA
'Lnk1'	enable lane 0, disable lane 1	NA
'Lnk2'	enable lane 1, disable lane 0	NA
'Lnk3'	enable both lanes	NA
'I2CW'	I2C master write. Write data must be ready before the command is issued	MSG_OUT_RDATA0..15 = write data (first byte transmitted is MSG_OUT_RDATA0[7:0]) SW_FW_MAILBOX_DATA_IN1/IECS_DATA[6:0] = i2c address SW_FW_MAILBOX_DATA_IN1/IECS_DATA[7] = no stop (to allow repeated start transactions). SW_FW_MAILBOX_DATA_IN1/IECS_DATA[15:8] = write length (max 64B) 1 – transaction failed/nack'ed. 2 – transaction completed successfully
'I2CR'	I2C master read	SW_FW_MAILBOX_DATA_IN1/IECS_DATA[6:0] = i2c address SW_FW_MAILBOX_DATA_IN1/IECS_DATA[15:8] = read length (max 64B) MSG_OUT_RDATA = read data (first byte received is MSG_OUT_RDATA0[7:0]) 1 – transaction failed/nack'ed. 2 – transaction completed successfully
'I2CF'	I2C frequency change	SW_FW_MAILBOX_DATA_IN1/IECS_DATA[15:0] = value to store in I2C_PRER register
'PPSW'	Write to Port Power Switch	MSG_OUT_RDATA0..15 = write data (first byte transmitted is MSG_OUT_RDATA0[7:0]) SW_FW_MAILBOX_DATA_IN1/IECS_DATA[15:8] = write length (max 64B) SW_FW_MAILBOX_DATA_IN1/IECS_DATA[23:16] = PPS register offset Result in SW_FW_MAILBOX_DATA_OUT0/IECS_DATA: [7:0] return value: 1 - transaction failed/nack'ed. 2 - transaction completed successfully
'PPSR'	Read from Port Power Switch	SW_FW_MAILBOX_DATA_IN1/IECS_DATA[15:8] = read length (max 64B) SW_FW_MAILBOX_DATA_IN1/IECS_DATA[23:16] = PPS register offset MSG_OUT_RDATA0..15 = returns the read data (first byte transmitted is MSG_OUT_RDATA0[7:0]) Result in SW_FW_MAILBOX_DATA_OUT0/IECS_DATA: [7:0] return value: 1 - transaction failed/nack'ed. 2 - transaction completed successfully [15:8] register true length (as reported by the PPS)

A.4. Supported IECS registers

The supported IECS registers are listed in Table 454.

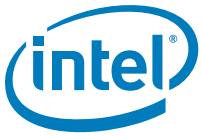


Table 454. Supported IECS Registers

IECS offset	Name	Length (Bytes)	Access (from IECS)	Description	Target offset (within each LC, Table 32)
0	VID	4	RO	As defined in TBT spec	0x0
1	DID	4	RO	As defined in TBT spec	0x1
2	ProtoVer	4	RO	As defined in TBT spec	0x2
3	Mode	4	RO	As defined in TBT spec	0x3
4	Type	4	RO	As defined in TBT spec	0x4
5	UID	16	RO	As defined in TBT spec	0x5-0x8
6	oUID	16	RW	As defined in TBT spec	0x9-0xc
7	Reserved	1	RO	As defined in TBT spec	0x8c[7:0]
8	Cmd	4	RW	As defined in TBT spec	0xe
9	Data	16	RW	As defined in TBT spec	0xa1-0xa4
10	HVREq	1	RO	As defined in TBT spec	0x62[7:0]
11	DescriptorHead	2	RO	As defined in TBT spec	0x11[15:0]
12	LinkEnable	2	RO	As defined in TBT spec	0x8d[15:0]
13	IECS_TXFEE	4	RO	As defined in TBT spec	0x8e
14	Reserved	4	RW	As defined in TBT spec	0x90
15	Version	4	RO	As defined in TBT spec	0x15
16	TargetAccess	8	RW	Vendor specific - Refer to registers LC_TARGET_ACCESS_DATA, LC_TARGET_ACCESS_CTRL for details.	0x9f-0xa0
17	FlashAccess	8	RW	Vendor specific - Refer to A.3.4 FLASH Burning for details.	0x9b-0x9c
18	MSG_OUT_RDATA	64	RW	Vendor specific - General purpose buffer (used by I2C commands, FLASH Access). Also used by the MSG_OUT mechanism	0x74-0x83

A.5. Useful Internal FW registers, for debug purposes

The following internal registers are available for LC/POC/IECS debug. The offsets are likely to change in future projects. Use for debug purpose only.

Table 455. Internal FW registers

Name	Offset	Bits	description
DEBUG_IECS_0	0x1de / 0x2de (PA / PB)	7..0	Iecs handshake state: 0x40=INIT 0x41=READ_O_VENDOR_ID 0x42=WRITE_oUUID 0x43=READ_O_HV_REQ 0x44=READ_CM_HV_CAP 0x45=WAIT_FOR_LT_RISE 0x46=READ_O_LANE_EN 0x4f=FINALIZE
DEBUG_O_VENDOR_ID	0x1da / 0x2da	31..0	Partner's vendor ID (iecs 0)

Table 455. Internal FW registers

Name	Offset	Bits	description
DEBUG_O_LANE_EN	0x1db / 0x2db	7..0 15..8	Partner's lane_en status Partner's lane_en available (iecs 12)
DEBUG_O_HV	0x1dc / 0x2dc	7..0 31..8	Partner's hv request Cable hv capability (iecs 10)
DEBUG_O_LC_TYPE	0x1dd / 0x2dd	31..0	Partner's LC type (EM/ECM)
DEBUG_POC_CSR_LOW	0x1e9 / 0x2e9	31..0	POC_CSR_IN_LOW at last power on
DEBUG_POC_CSR_HIGH	0x1ea / 0x2ea	31..0	POC_CSR_IN_HIGH at last power on
DEBUG_POC_MAILBOX	0x1eb / 0x2eb	31..0	POC_CSR_MAILBOX at last power on
DEBUG_POC_CSR_COMMON	0x1e8 / 0x2e8	31..0	POC_CSR_COMMON at last power on

Appendix B. HDP Configuration Procedures

B.1. DP IN Configuration from Flash Memory

DP tunnel setup requires configuring GPU SSC parameter into DP OUT TMU SSC_PPM_Shift register. As this parameter is GPU dependant, it is bound to DP IN and reported in VSEC_DP_CS_50. CM software is expected to read it, and if GPU is present (VSEC_DP_CS_50. GPU_present), configure DP OUT accordingly. EE2TAR should initialize VSEC_DP_CS_50 depending on system build.

B.2. Forcing HPD high on PA/PB for DP debug

The following flow should be used in order to force hpd high in PA/PB:

1 Connect dp cable, see monitor.

2 Set the relevant IO CTRL REG bits (refer to Table 23). To avoid glitches, first write the required value and then write the required sustain bits.

3 Disconnect the display, connect the test equipment.

When done, in order to restore the system to normal state, either power cycle or clear the relevant IO CTRL REG sustain bits. Do not change the data bits.

B.3. Controlling VS/PE for HDP Tx

The transmit control for all 3 DP transmitters is the same. It is controlled through 3 registers, TX_SW_INV, DP_TX_POST & TX_SW_PRE. In order to fully understand the mechanism and those registers effect, refer to section Transmitter Equalization (TXFFE) for full description. The default (and recommended) values of the above registers are located in the NVM, at the DP_OUT Region. The DP OUT controller uses those NVM settings according to mode of operation and VSPE requested by the monitor the DP_OUT Region is part of the DP_OUT uCode and starts at offset 0x22 from the start of the uCode section. The exact location is referred by a pointer in the digital section HDP_OUT Region fields.

Table 456. DP OUT Region structure and TXFEE recommended settings for DP

Mode	VS	PE	Offset	TX_SW_INV	TX_SW_PRE	TX_SW_POST
DP	(400mV)	(0dB)	0x3	7	0	0
DP	(400mV)	(3.5 dB)	0x6	4	0	3
DP	(400mV)	(6 dB)	0x9	1	0	6
DP	(600mV)	(0dB)	0xC	5	0	0
DP	(600mV)	(3.5 dB)	0xF	3	0	2
DP	(600mV)	(6 dB)	0x12	0	0	5
DP	(800mV)	(0dB)	0x15	3	0	0
DP	(800mV)	(3.5 dB)	0x18	0	0	3

B.4. DP Transmitter/Receiver Testing Procedure

Titan Ridge DD supplies an ability to transmit various DP patterns from its DP Sources and count mismatches/errors of these patterns on its DP Sink side.

The patterns that can be transmitted are:

- TPS1/TPS2/TPS3/TPS4
- PRBS7
- Symbol error rate measurement pattern
- Eye pattern. (configurable)
- 80bit configurable pattern

The patterns that can be checked for errors in Titan Ridge DD Sink are:

- TPS1/TPS2/TPS3/TPS4
- PRBS7
  - — Counts either symbol or bit errors
- 80bit configurable pattern
- Eye pattern
  - — Configurable
  - — Counts either symbol or bit errors
  - — Requires preceding link training

  Symbol error counter of any stream
  - — Requires preceding link training

Checking the DP Sources could be accomplished in 2 ways:

1. Stand alone:
   - — Set up the transmitter to generate the desired frequency with no reference clock to track from receiver. Those steps are described in Table 457.
   - — Activate the desired test pattern by the Source. Those steps are described in Table 458.
2. Redriver:
   - — Activate the system by plugging a monitor.
   - — Activate the desired test pattern by the Source. Those steps are described in Table 458.

Checking the DP Sinks for Integrity of some patterns, link training (only TPS2/TPS3/TPS4 stage) should be preceded in this sink. The steps needed to configure the Sink are described in Table 459.

Table 457. DP Tx Standalone configuration

Register space	Register Name	Write Value	Description
Raise SRC HPD			
Device configuration space	Address 0x49 bits [7:6] PA: Address 0x3D bits [31:30] PB: Address 0x49 bits [5:4]	11b	SRC HPD

Table 457. DP Tx Standalone configuration (Continued)

Register space	Register Name	Write Value	Description
Choose Phy operation mode			
Misc2	"HDP_CTRL_2" on page 482	0x00	Clear leg_phy_en
Force Tx Termination			
DP 8051 (Src)	"CM_TX_RESTUNE_SET - Tx termination resistor settings in bypass mode" on page 606	0x2	
DP 8051 (Src)	"CM_MISC_CTRL- Misc. Phy Common control" on page 606	0x1	
Enable Tx Phy			
DP 8051 (Src)	"CM_DPPLL_CTRL - PLL Misc Control" on page 609	0x0	
Wait 5u Sec Set Tx VSPE			
DP 8051 (Src)	"TX_SW_INV - Lane 0/1/2/3 TX CID swing control" on page 605	0x3	
DP 8051 (Src)	"TX_SW_PRE - Lane 0/1/2/3 TX 1st pre-cursor swing control" on page 606	0x0	
DP 8051 (Src)	"TX_SW_POST - Lane 0/1/2/3 TX 1st post-cursor swing controlSwizzle_1020_EN - Swizzle data towards Phy" on page 606	0x0	
Jumpstart the PLL			
DP 8051 (Src)	"Allow_RTL_DPPLL_CTRL - Switch control over PLL interface" on page 608	0x0	
DP 8051 (Src)	"CM_DPPLL_CTRL - PLL Misc Control" on page 609	0x4	
DP 8051 (Src)	"CM_DPPLL_LOOP_CTRL - PLL third loop control" on page 608	0x0	
DP 8051 (Src)	"CM_DPPLL_CTRL - PLL Misc Control" on page 609	0x0	
Configure PLL params			
DP 8051 (Src)	"CM_DPPLL_CP_RES_SEL - PLL Resistor Select Control" on page 609	0x0A	
Per Speed Control			
DP 8051 (Src)	"Allow_RTL_DPPLL_CTRL - Switch control over PLL interface" on page 608	DP 1.62 0x84 DP 2.7 0x44 DP 5.4 0xB0 DP 8.1 0x44	

Table 457. DP Tx Standalone configuration (Continued)

Register space	Register Name	Write Value	Description
DP 8051 (Src)	"CM_DPPLL_POSTDIVSEL - PLL post divider settings" on page 609	DP 1.62 0x05 DP 2.7 0x03 DP 5.4 0x02 DP 8.1 0x00	
DP 8051 (Src)	"CM_DPPLL_F_L - PLL fractional multiplication factor, low" on page 608	DP 1.62 0xFC DP 2.7 0xFF DP 5.4 0xFE DP 8.1 0xFF	
DP 8051 (Src)	"CM_DPPLL_F_M - PLL fractional multiplication factor, med" on page 608	DP 1.62 0xFF DP 2.7 0xFF DP 5.4 0xFF DP 8.1 0xFF	
DP 8051 (Src)	"CM_DPPLL_F_H - PLL fractional multiplication factor, high" on page 608	DP 1.62 0x3F DP 2.7 0x3F DP 5.4 0x3F DP 8.1 0x3F	
DP 8051 (Src)	"CM_DPPLL_RST_B - PLL reset" on page 608	0x1	
DP 8051 (Src)	"CM_DPPLL_CTRL - PLL Misc Control" on page 609	0x4	
DP 8051 (Src)	"CM_DPPLL_CTRL - PLL Misc Control" on page 609	0x2	
DP 8051 (Src)	"CM_DPPLL_CTRL - PLL Misc Control" on page 609	0x0	
At this stage "CM_DPPLL_CTRL - PLL Misc Control" on page 609 bit 7 should be high (CM_PLL_LOCK) Wait 1u Sec Set D10.2			
Misc	"Register 0h -- LS_RST -- ls_rst setting/resetting. Polarity: positive" on page 595	0x00	
Wait 1u Sec Enable Tx			
DP 8051 (Src)	"TX_SW_POST - Lane 0/1/2/3 TX 1st post-cursor swing controlSwizzle_1020_EN - Swizzle data towards Phy" on page 608	0x0F	
Misc2	"CAR CTRL" on page 562	0x40	Clock ungating
DP 8051 (Src)	"DP_SPEED - Misc. Phy Common control 2" on page 606	0xF	
DP 8051 (Src)	"TX_SYNC_CTRL- Tx Sync control" on page 610	0x0F	
DP 8051 (Src)	"TX_SYNC_CTRL- Tx Sync control" on page 610	0xFF	

Table 457. DP Tx Standalone configuration (Continued)

Register space	Register Name	Write Value	Description

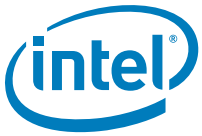
Table 458. DP Tx D10.2/Eye pattern/PRBS/80bit configuration

For Eye pattern transmissio			
DP 8051 (Src)	"TST_PTTRN_SR_1" on page 494	0x3C	Set the 2nd symbol of SR sequence to be K28.1
DP 8051 (Src)	"TST_PTTRN_SR_2" on page 494	0x3C	Set the 3rd symbol of SR sequence to be K28.1
DP 8051 (Src)	"TST_PTTRN_BS_RATIO_0" on page 495	0xFC	Set Eye pattern length to be 252
DP 8051 (Src)	"TST_PTTRN_BS_RATIO_1" on page 495	0x0	
DP 8051 (Src)	"TST_PTTRN_SR_RATIO_0" on page 495	0x0	Send only SR sequences (no BS sequences)
DP 8051 (Src)	"TST_PTTRN_SR_RATIO_1" on page 495	0x0	
DP 8051 (Src)	"TST_PTTRN_CTRL_2" on page 494	0x3	SR sequence length is 4 symbols + count bit errors
DP 8051 (Src)	"TST_PTTRN_CTRL_0" on page 493	(1 << lane_count) – 1	Send Eye pattern on all of the activated lanes.
For PRBS transmission			
DP 8051 (Src)	"TST_PTTRN_CTRL_0" on page 493	((1 << lane_count) – 1)<<4	Send PRBS pattern on all of the activated lanes.
For 80bit pattern transmission			
DP 8051 (Src)	"Register 80h -- SHIFT_PATTERN_IN0" on page 606	80bit_pattern	Configure 10 registers of 80bit pattern
DP 8051 (Src)	"TST_PTTRN_CTRL_1" on page 493	(1 << lane_count) – 1	Send 80bit pattern on all of the activated lanes.

Different lanes can be configured to transmit different test patterns - using TST_PTTRN_CTRL_0 and TST_PTTRN_CTRL_1.

B.5. Pseudo-Macro Script for DP Transmitted Pattern

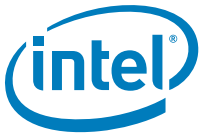
```
proc Raise SRC HPD // This is for PA. For SRC0 it's 0x49 bits 6-7; For PB it's 0x49 bits 4-5
{
write IO_CTRL[31:30] (0x3D,[31:30], 0x3)
 }

proc enable DP1.2 //
{
write_src(0xC806[7:0], 0x0)
}

proc Force Tx Termination //
{
write_src(0xD67A,[7:0], 0x2)
write_src(0xD67B,[7:0], 0x1)
write_src(0xD67C,[7:0], 0x0)
}

proc Kill VSPE //
{
write_src(0xD600,[7:0], 0x0)
write_src(0xD601,[7:0], 0x0)
write_src(0xD602,[7:0], 0x0)
}

proc Jumpstart the PLL
{
write_src(0xD767,[7:0], 0x0)
write_src(0xD77F,[7:0], 0x4)
write_src(0xD77C,[7:0], 0x0)
write_src(0xD77F,[7:0], 0x0)
write_src(0xD76D,[7:0], 0x1)
write_src(0xD77F,[7:0], 0x04)
write_src(0xD77F,[7:0], 0x02)
write_src(0xD77F,[7:0], 0x00)
write_src(0xC200,[7:0], 0x3)
write_src(0xCC00,[7:0], 0x1)
}

proc Enable Tx
```



```
{
write_src(0xD672,[7:0], 0x0F)
write_src(0xC80F,[7:0], 0x40)
write_src(0xD67E,[7:0], 0x0F)
write_src(0xD67F,[7:0], 0x0F)
write_src(0xD67F,[7:0], 0xFF)
}

proc SetPRBS7 // As example SnkPort 110, Port 11, BitRate
{
  ReleaseFromPLTPAT // $Port        #Transmit in all 4 lanes
  write_src(0xD87E,[7:0], 0x01) //  #Transmit PRBS7
  write_src(0xC870,[7:0], 0xf0)
}

proc ReleaseFromPLTPAT // As example Port 11
{
 write_src(0xC871,[7:0], 0x00)
}


proc SetD10.2 // As example SnkPort 110, Port 11, BitRate
{
                ReleaseFromPLTPAT $Port            #Transmit in all 4 lanes
                write_src(0xD87E,[7:0], 0x01)//   #Configuring D10.2
                write_src(0xC870,[7:0], 0x00)
                write_snk(0xC200,[7:0], 0x09)// # This is for re-drive
                write_src(0xD202,[7:0], 0x02)// #This is for Tunneling
                write_snk(0xC200,[7:0], 0x03)
                write_src(0xC600,[7:0], 0x01)
}

proc HBR2CPAT // As example Port 11, BitRate
{
                ReleaseFromPLTPAT// $Port       #Transmit in all 4 lanes
                write_src(0xD87E,[7:0], 0x01)// #Configuring HBR2CPAT
                write_snk(0xC200,[7:0], 0x09)// # This is for re-drive
                write_src(0xD202,[7:0], 0x02)// #This is for Tunneling
                write_src(0xC879,[7:0], 0x3C)
                write_src(0xC87a,[7:0], 0x3c)
```

```
                write_src(0xC87c,[7:0], 0xfc)
                write_src(0xC87d,[7:0], 0x00)
                write_src(0xC87e,[7:0], 0x00)
                write_src(0xC87f,[7:0], 0x00)
                write_src(0xC872,[7:0], 0x03)
                write_src(0xC870,[7:0], 0x0f)
}


proc PLTPAT // As example Port 11, BitRate
{
                write_src(0xD674,[7:0], 0x0)// #Configuring 80 bits pattern
                write_src(0xCe80,[7:0], 0xf8)
                write_src(0xCe81,[7:0], 0x3e)
                write_src(0xCe82,[7:0], 0x0f)
                write_src(0xCe83,[7:0], 0x83)
                write_src(0xCe84,[7:0], 0xe0)
                write_src(0xCe85,[7:0], 0xf8)
                write_src(0xCe86,[7:0], 0x3e)
                write_src(0xCe87,[7:0], 0x0f)
                write_src(0xCe88,[7:0], 0x83)
                write_src(0xCe89,[7:0], 0xe0)
                write_src(0xC871,[7:0], 0x0f)
}
```

Table 459. DP Rx Eye pattern/PRBS Startup



Space	Register Name	DP 5.4	DP 2.7	DP 1.62	DP 8.1	Description
MISC2	HDP_CTRL_0	80	80	80	80	
CMN	DP_RATE	2	1	0	3	
AN_IF						
MISC	LS_RST	1	1	1	1	Reset
CMN	SIPO_RST_N	0	0	0	0	
CMN	RX_RST_N	0	0	0	0	
CMN						
CMN	RX_EN	0	0	0	0	
MISC2	HDP_CTRL_0	80	80	80	80	
CMN						
CMN						
CMN		80	80	80		
LANE		0	1	1		Prepare datapath
CMN		0	0	0		
CMN		0	55	55		
CMN		0	55	55		
CMN		f0	f0	f0		
CMN	DP_RATE	2	1	0	3	
LANE		7	7	3	7	
LANE		2	4	8	2	Set Phy rate
LANE		7	7	f	7	
LANE		2	2	1	2	

Space	Register Name	DP 5.4	DP 2.7	DP 1.62	DP 8.1	Description
CMN	RX_EN	f	f	f	F	Phy out of reset (bit per lane)
CMN	RX_EYEMON_CTRL	f	f	f	F	
CMN	RX_RST_N	f	f	f	F	
CMN	SIPO_RST_N	f	f	f	F	
CMN	RX_EN	f	f	f		PI calibration start
CMN	RX_EYEMON_CTRL	80	80	80		
LANE	EYEMON_MASK_SEL0	0	0	0		
CMN	RX_EYEMON_CTRL	0	0	0		
CMN	RESET_PI_FSMS	ff	ff	ff		
CMN	RESET_PI_FSMS	0	0	0		
CMN	RTL_IN_CTRL_PI0_CTLE1	0	0	0		
CMN	ALLOW_RTL_CTLE_CTRL	0	0	0		
CMN	RX_PLL_MODE_CTRL0/1/2/3	ff	ff	ff		
CMN	PI_PD_EN	f	f	f		
CMN	FINE_SCAN_WIDTH	1e	1e	1e		
CMN	PI_CAL_CTRL	2f	2f	2f		
CMN	PI_CAL_CTRL	20	20	20		
CMN	PI_CAL_EN	f	f	f		
while ((PHY_DIG_CMN[PI_CAL_DONE_ADR] & 0xf) != (PHY_DIG_CMN[PI_PD_EN] & 0xf));						Wait for PI calibration to end

Space	Register Name	DP 5.4	DP 2.7	DP 1.62	DP 8.1	Description
CMN	PI_CAL_EN	0	0	0		CTLE selection
CMN	PI_PD_EN	0	0	0		
CMN	CACHE_CTRL1	f	f	f		
CMN	RX_PLL_MODE_CTRL0/1/2/3	f	f	f		
CMN	RTL_IN_CTRL_PI0_CTLE1	f	f	f		
CMN	ALLOW_RTL_CTLE_CTRL	f	f	f		
CMN	SELECT_CTLE	f	f	f		
tmp = ((~PHY_DIG_CMN[RX_EN]) & 0xf0)>>4; while ((PHY_DIG_CMN[CTLE_SELECTED] & tmp) != tmp)						Wait for CTLE to be selected
CMN	RX_EYEMON_CTRL	0	0	0		
MISC2	HDP_CTRL2	0	0	0		
MISC2	RX_STATE	3	2	2		
MISC2	CAR_CONTROL	0	0	0		
MISC	LS_RST	0	0	0		

Table 460. DP Rx Eye pattern/PRBS configuration

Register space	Register Name	Write Value	Description
Wait a couple of msec, or until PHY_CONFIG_REG6.SYMB_LOCKED is set for all of the active lanes in order to verify that the symbol-lock is achieved			
DP 8051 (Snk)	"HDP_CTRL_0" on page 482	0x4	Set DP_STATE to Active
	"TST_PTTRN_SR_1" on page 567	0x80	Enable counter-B to count the errors
Start sending the test pattern to this Sink at this stage			
To **check** Eye pattern			
DP 8051 (Snk)	"TST_PTTRN_SR_1" on page 567	0x3C	Set the 2nd symbol of SR sequence to be K28.1
DP 8051 (Snk)	"TST_PTTRN_SR_2" on page 568	0x3C	Set the 3rd symbol of SR sequence to be K28.1
DP 8051 (Snk)	"TST_PTTRN_BS_RATIO_0" on page 568	0xFC	Set Eye pattern length to be 252

Table 460. DP Rx Eye pattern/PRBS configuration

Register space	Register Name	Write Value	Description
DP 8051 (Snk)	"TST_PTTRN_BS_RATIO_1" on page 568	0x0	
DP 8051 (Snk)	"TST_PTTRN_SR_RATIO_0" on page 568	0x0	Send only SR sequences (no BS sequences)
DP 8051 (Snk)	"TST_PTTRN_SR_RATIO_1" on page 568	0x0	
DP 8051 (Snk)	"TST_PTTRN_CTRL_2" on page 492	0x3	SR sequence length is 4 symbols + count bit errors
DP 8051 (Snk)	"TST_PTTRN_CTRL_0" on page 491	(1 << lane_count) – 1	Enable Eye pattern check on the activated lanes
To check PRBS			
DP 8051 (Snk)	"TST_PTTRN_CTRL_0" on page 491	((1 << lane_count) – 1)<<4	Enable PRBS pattern check on the activated lanes
Start sending Eye/PRBS pattern			
DP 8051 (Snk)	"ERR_LOCK_COUNT_B" on page 531	0xF	Clear the error counter
After a while, verify TST_PTTRN_STATUS . TST_PTTRN_LOCK is set for the activated lanes			
DP 8051 (Snk)	"ERR_LOCK_COUNT_B" on page 531	0xF	Sample the error counter-B
Read ERR_COUNT_STD_(0-3)B_(LO,MD,HI)			

Different lanes can be configured to check different test patterns - using "TST_PTTRN_CTRL_0" on page 491.

The counter can be configured to count in resolution of the bit errors - using "TST_PTTRN_CTRL_2" on page 492.

DP Compliance Spec. defines 3 different Eye patterns -verify that the correct one is configured in "TST_PTTRN_SR_1" on page 492/"TST_PTTRN_SR_2" on page 492.

In order to count 8b10b errors (for example during normal operation):

Register space	Register Name	Write Value	Description
DP 8051 (Snk)	"ERR_LOCK_COUNT_B" on page 531	0xF	Clear the error counter
DP 8051 (Snk)	"ERR_LOCK_COUNT_B" on page 531	0xF	Sample the error counter-B
Read "ERR_COUNT_STD_0B_LO" on page 533			

B.6. DPCD Handling

See Table 461 for DPCD registers implemented in DisplayPort Sinks.

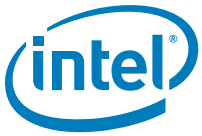


Table 461. DPCD registers Legacy Mode

Address	Configuration Register	R/W over AUX	Notes
0000h	DPCD_REV	RO	Pass through, but the reply is overwritten not to surpass 1.1/1.2 in tunneling/redriver mode (respectively)
00001h	MAX_LINK_RATE	RO	Pass through. Reads to this register are passed through to the DisplayPort Sink until training complete notification is received from the DisplayPort OUT. If DisplayPort OUT obtained lower link rate or failed to obtain the link, this register starts being local in order to advertise lower capability and the link is retrained.
00002h	MAX_LANE_COUNT	RO	Pass through, but the reply of TPS3_SUPPORTED field is overwritten to 1 to enable better equalization.
0000Eh	TRAINING_AUX_RD_INTERVAL	RO	For DisplayPort IN it is configurable from flash. DisplayPort OUT reads this DPCD from DisplayPort Sink after HPD plug and uses it during the link training.
00005h	TPS4Supported	RO	For DisplayPort Out reading from Screen For DisplayPort In overwritten to 1 for enable better equalization
00021h	MSTM_CAP	RO	Pass through. Use for inform tunnel MST mode, may overwrite to 0 to support Legacy Ridge chip
00054h-00057h	RX_GTC_VALUE	RO	Pass through, but the value is updated by the delay through TBT chip
00060h	DSC Support	RO	Pass through, use inform tunnel of possibility DSC Overwrite to 0 with legacy Ridge chip
00062h - 0006Fh	DSC register	RO	Pass through, Overwrite to 0 with legacy Ridge chip
00090h	FEC Capability	RO	Pass through, use inform tunnel of possibility FEC, overwrite to 0 with legacy Ridge Chip.
00100h	LINK_BW_SET	R/W	Accesses to this register are always terminated at the DisplayPort IN.
00101h	LANE_COUNT_SET	R/W	Accesses to this register are always terminated at the DisplayPort IN.
00102h	TRAINING_PATTERN_SET	R/W	Accesses to this register are always terminated at the DisplayPort IN.
00103h	TRAINING_LANE0_SET	R/W	Accesses to this register are always terminated at the DisplayPort IN.
00104h	TRAINING_LANE1_SET	R/W	Accesses to this register are always terminated at the DisplayPort IN.
00105h	TRAINING_LANE2_SET	R/W	Accesses to this register are always terminated at the DisplayPort IN.
00106h	TRAINING_LANE3_SET	R/W	Accesses to this register are always terminated at the DisplayPort IN.
00107h	DOWNSPREAD_CTRL	R/W	Accesses to this register are always terminated at the DisplayPort IN.
00108h	MAIN_LINK_CHANNEL_CODING_SET	R/W	Accesses to this register are always terminated at the DisplayPort IN.

Table 461. DPCD registers Legacy Mode

Address	Configuration Register	R/W over AUX	Notes
0010Bh-0010Eh	LINK_QUAL_LANEx_SET	R/W	Pass through, but the value is influencing the configuration in DisplayPort IN and DisplayPort OUT.
0010Fh-00110h	TRAINING_LANEx_y_SET2	R/W	Accesses to this register are always terminated at the DisplayPort IN.
00120h	FEC Configuration	R/W	FEC ready pass through, when 1 data has latency for FEC data correct. Overwrite to 0 with Legacy Ridge chip.
00154h-00157h	TX_GTC_VALUE	WO	Pass through, but the value is updated by the delay through TBT chip
00202h/0200Ch	LANE0_1_STATUS	RO	Accesses to this register are always terminated at the DisplayPort IN.
00203h/0200Dh	LANE2_3_STATUS	RO	Accesses to this register are always terminated at the DisplayPort IN.
00204h/0200Eh	LANE_ALIGN_STATUS_UPDATED	RO	Accesses to this register are always terminated at the DisplayPort IN.
00206h	ADJUST_REQUEST_LANE0_1	RO	Accesses to this register are always terminated at the DisplayPort IN.
00207h	ADJUST_REQUEST_LANE2_3	RO	Accesses to this register are always terminated at the DisplayPort IN.
0020Ch	ADJUST_REQUEST_POST_CURSOR2	RO	Accesses to this register are always terminated at the DisplayPort IN replying 0.
00210h-00211h	SYMBOL_ERROR_COUNT_LANE0	RO	This register is configurable (using implementation-defined mechanisms) as pass through to DisplayPort Sink or terminated locally at the DisplayPort IN.
00212h-00213h	SYMBOL_ERROR_COUNT_LANE0	RO	This register is configurable (using implementation-defined mechanisms) as pass through to DisplayPort Sink or terminated locally at the DisplayPort IN.
00214h-00215h	SYMBOL_ERROR_COUNT_LANE0	RO	This register is configurable (using implementation-defined mechanisms) as pass through to DisplayPort Sink or terminated locally at the DisplayPort IN.
00216h-00217h	SYMBOL_ERROR_COUNT_LANE0	RO	This register is configurable (using implementation-defined mechanisms) as pass through to DisplayPort Sink or terminated locally at the DisplayPort IN.
0024Ah-0024Bh	HBR2_COMPLIANCE_SCRAMBLER_RESET	RO	Pass through, but the replied value is influencing the configuration in DisplayPort OUT.
00250h – 00259h	TEST_80BIT_CUSTOM_PATTERN	RO	Pass through, but the replied value is influencing the configuration in DisplayPort OUT.

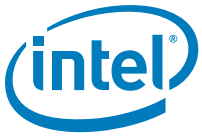


Table 461. DPCD registers Legacy Mode

Address	Configuration Register	R/W over AUX	Notes
0600h	SET_POWER	R/W	Accesses to this register are always terminated at the DisplayPort IN. All Write transactions are mirrored by DisplayPort OUT. Also, Whenever DisplayPort OUT initiates training, it first initiates a Write transaction, setting the DisplayPort Sink to D0. When DisplayPort IN is in D0 state, a Read transaction will cause a Write transaction by DisplayPort OUT, setting the DisplayPort Sink to D0.
E0000h	TBT_IEEE_OUI_0	RO	Accesses to this register are always terminated at the DisplayPort IN with value 0x98
E0001h	TBT_IEEE_OUI_1	RO	Accesses to this register are always terminated at the DisplayPort IN with value 0x4F
E0002h	TBT_IEEE_OUI_2	RO	Accesses to this register are always terminated at the DisplayPort IN with value 0xEE
E0003h	TBT_DEVICE_IDENTIFICATION_STRING_0	RO	Accesses to this register are always terminated at the DisplayPort IN with value T
E0004h	TBT_DEVICE_IDENTIFICATION_STRING_1	RO	Accesses to this register are always terminated at the DisplayPort IN with value R
E0005h	TBT_DEVICE_IDENTIFICATION_STRING_2	RO	Accesses to this register are always terminated at the DisplayPort IN with value 0x0
E0006h	TBT_DEVICE_IDENTIFICATION_STRING_3	RO	Accesses to this register are always terminated at the DisplayPort IN with value 0x0
E0007h	TBT_DEVICE_IDENTIFICATION_STRING_4	RO	Accesses to this register are always terminated at the DisplayPort IN with value 0x0
E0008h	TBT_DEVICE_IDENTIFICATION_STRING_5	RO	Accesses to this register are always terminated at the DisplayPort IN with value 0x0
E0009h	TBT_HW_REVISION	RO	Accesses to this register are always terminated at the DisplayPort IN with value 0xA0
E000Ah	TBT_FW_MAJOR_REVISION	RO	Accesses to this register are always terminated at the DisplayPort IN with value 0x01
E000Bh	TBT_FW_MINOR_REVISION	RO	Accesses to this register are always terminated at the DisplayPort IN with value 0x01
E000Ch	TBT_REMOTE_LT_STATUS	RO	Accesses to this register are always terminated at the DisplayPort IN with values: 0x04 - LU 0x10 - LF 0x40 - LFalt
E000Dh - E00FFh	RESERVED for TBT	RO	Reserved

B.7. DP tunneling

Introducing DP1.2 and 2x10 TBT link requires making some additions to the existing DP tunnel establishment.

DP_IN and DP_OUT have to know the capabilities of each other in order to avoid incompatibility, e.g. DP_IN that supports 5.4GHz and MST should prevent activation of these features in the system if it is paired with a legacy DP_OUT that doesn't support these features. The exchange of the capabilities between DP_IN and DP_OUT should be performed by the Connection Manager.

Having 20Gbps TBT link allows driving more than one DP1.1 stream through such a link. Knowing the status of the existing DP tunnels and the ability to configure DP capabilities allow Connection Manager to better control TBT resource allocation.

The flow:

- Monitor connection ' HPD assertion
- After de-bouncing of 100ms DP_OUT reads the monitor capabilities (DPCD Rev, link-rate, lane-count, enhanced framing and TPS3 support) and updates its DP_LOCAL_CAP. (DP_LOCAL_CAP reflects the minimal values between its eeprom/flash and the monitor capabilities)
- Plug event is triggered towards CM
- CM exchanges the capabilities of DP_IN and DP_OUT by copying DP_LOCAL_CAP of DP_IN/ DP_OUT to DP_REMOTE_CAP of DP_OUT/DP_IN (respectively):
  - If needed, CM can downgrade the read value of DP_OUT(DP_LOCAL_CAP) before writing it to DP_IN(DP_REMOTE_CAP), e.g. in order to prevent overbooking of TBT link resources
- Continue with the tunnel building

Note:

- The only field in DP_REMOTE_CAP that interests DP_OUT is "Remote DP Capability ID", i.e. DP Capability ID of DP_IN
- "DP Capability ID" should be copied by CM as is, without changing it
- DP_REMOTE_CAP is zeroed upon aux_enable clearing (i.e. parking the capabilities of its remote DP partner in the legacy mode)
- Without making this exchange DP adapters will work in the legacy mode, i.e. DP_IN won't advertise to GPU capabilities higher than DP1.1
- Reading DP_LOCAL_CAP from a legacy device will return value of 0, that will cause the new adapter to realize that it has a legacy DP remote partner.
- CM can check the status of the existing DP tunnel in DP_STATUS register of the new adapter

Figure 44. DP tunneling