=== DEVICE INFORMATION ==========

PCI Address: 0x00000000 (Bus 0 -> Device 0 -> Function 0)
Vendor: 8086h | Intel Corporation
Status: 0044h | Core Processor DRAM Controller

=== GENERAL ==========

--- DESCRIPTION ----------

Classcode: 060000h
Revision: 02h
Class: Bridge
Detail: Host bridge
P/I: n/a

--- STATUS ----------

Value: 0006h
I/O Space: disabled
Memory Space: enabled
Bus Master: yes
Special Cycles: no
Memory Write Invalidate: disabled
VGA Palette Snoop: disabled
Parity Error Response: no
Stepping Control: no
SERR: disabled
Back-to-Back: disabled
Interrupt: enabled

--- COMMAND ----------

Value: 2090h
Error: none
Master abort: received
Target abort: none
Data Parity: ok
Back-to-back: fast
Features: standard
66 MHz: no
Capability List: yes
DEVSEL-Timing: fast
IRQ signaled: no

--- INFORMATION ----------

Cacheline: 0 * 32 bit
Latency: 0 + 8 Cycles
Header: 00h
Unit type: single function
Self-test: not built-in

--- IRQ ----------

IRQ: 00h
IRQ pin: none
Latency: 0 / 0

=== BARS & ROM ==========

--- BAR 0 ---

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 1 ---

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 2 ---

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 3 ---

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 4 ---

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 5 ---

Type: n/a
Address:: n/a
Size:: n/a

--- ROM ---

Type: n/a
Address:: n/a
Size:: n/a

=== CAPABILITIES ==========

--- CAPABILITY 1 ---

ID: 09h
Name: Vendor specific capability register set
Offset: E0h

=== CONFIGURATION SPACE ==

```
00          86 80 44 00 06 00 90 20 02 00 00 06 00 00 00 00    D...  ........
10          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
20          00 00 00 00 00 00 00 00 00 00 00 00 3C 10 2A 17  ............<.*.
30          00 00 00 00 E0 00 00 00 00 00 00 00 00 00 00 00  ....à...........
40          01 90 D1 FE 00 00 00 00 01 00 D1 FE 00 00 00 00  . Ñþ......Ñþ....
50          00 00 50 0B 09 00 00 00 00 00 00 00 00 00 00 00  ..P.............
60          00 00 00 00 00 00 00 00 01 B0 D1 FE 00 00 00 00  .........°Ñþ....
70          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
80          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
90          00 00 00 00 00 00 00 00 7F 00 8E 00 00 00 00 00  .......... .....
A0          80 00 C0 23 00 00 00 BE 00 00 C0 BD 00 00 80 BB   .À#...¾..À½.. »
B0          00 C0 00 00 00 00 00 00 00 00 00 00 00 00 00 00  .À..............
C0          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
D0          00 00 00 00 03 03 00 00 00 00 00 00 00 00 00 82  ................
E0          09 00 0C 01 26 61 21 00 88 00 00 00 00 00 00 00  ....&a!. .......
F0          00 00 00 00 0D 00 00 00 AB 0F 18 00 00 00 00 00  ........«.......
```

=== DEVICE INFORMATION ==========

PCI Address: 0x00001c00 (Bus 0 -> Device 28 -> Function 0)
Vendor: 8086h | Intel Corporation
Status: 3B42h | 5 Series/3400 Series Chipset PCI Express Root Port 1

=== GENERAL ==========

--- DESCRIPTION ----------

Classcode: 060400h
Revision: 05h
Class: Bridge
Detail: PCI bridge
P/I: Normal decode

--- STATUS ----------

Value: 0007h
I/O Space: enabled
Memory Space: enabled
Bus Master: yes
Special Cycles: no
Memory Write Invalidate: disabled
VGA Palette Snoop: disabled
Parity Error Response: no
Stepping Control: no
SERR: disabled
Back-to-Back: disabled
Interrupt: enabled

--- COMMAND ----------

Value: 0010h
Error: none
Master abort: none
Target abort: none
Data Parity: ok
Back-to-back: normal
Features: standard
66 MHz: no
Capability List: yes
DEVSEL-Timing: fast
IRQ signaled: no

--- INFORMATION ----------

Cacheline: 16 * 32 bit
Latency: 0 + 8 Cycles
Header: 01h
Unit type: multi function
Self-test: not built-in

--- IRQ ----------

IRQ: 0Bh
IRQ pin: INTA
Latency: 0 / 0

=== BARS & ROM ==========

--- BAR 0 ----------

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 1 ----------

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 2 ----------

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 3 ----------

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 4 ----------

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 5 ----------

Type: n/a
Address:: n/a
Size:: n/a

--- ROM ----------

Type: n/a
Address:: n/a
Size:: n/a

=== CAPABILITIES ==========

--- CAPABILITY 1 ----------

ID: 10h
Name: PCI Express Capability register set
Offset: 40h

--- CAPABILITY 2 ----------

ID: 05h
Name: Message Signaled Interrupts
Offset: 80h

--- CAPABILITY 3 ----------

ID: 0Dh
Name: P2P SSID
Offset: 90h

--- CAPABILITY 4 ----------

ID: 01h
Name: PCI Power Management Interface
Offset: A0h

=== PCI EXPRESS ==========

--- CAPABILITY REGISTER ----------

Version: 02h
Device Port Type: Root Port
Slot Implemented: yes
Interrupt Message Number: 00h

--- DEVICE CAPABILITIES ----------

Max Payload Size Supported: 128 B
Phantom Functions: not available
Extended Tag Field: 5-bit Tag Field supported
Endpoint L0 Acceptable Latency: x < 64 ns
Endpoint L1 Acceptable Latency: x < 1 s
Attention Indicator: none
Power Indicator: no
Role-Based Error Reporting: not supported
Captured Slot Power: 0 W
Function Level Reset Capability: not supported
Completion Timeout Ranges Supported: Range B, C
Completion Timeout Disable: supported
ARI Forwarding: not supported
AtomicOp Routing: not supported
32-bit AtomicOp Completer: not supported
64-bit AtomicOp Completer: not supported
128-bit CAS Completer: not supported
No RO-enabled PR-PR Passing: no
LTR Mechanism: not supported
TPH Completer Supported: none
OBFF Supported: not supported
Extended Fmt Field: not supported
End-End TLP Prefix: not supported
Max End-End TLP Prefixes: 4

--- DEVICE CONTROL ---

```
Correctable Error Reporting:   disabled
Non-Fatal Error Reporting:     disabled
Fatal Error Reporting:         disabled
Unsupported Request Reporting: disabled
Relaxed Ordering:              disabled
Max Payload Size:              128 B
Extended Tag Field:            5-bit Tag Field enabled
Phantom Functions:             disabled
Aux Power PM:                  disabled
No snoop:                      disabled
Max read request size:         128 B
Initiate Function Level Reset: disabled
Initiate Function Level Reset: n/a
Completion Timeout Value:      50  s - 50 ms
Completion Timeout:            enabled
ARI Forwarding:                disabled
AtomicOp Requester:            disabled
AtomicOp Egress Blocking:      no
IDO Request:                   disabled
IDO Completion:                disabled
LTR Mechanism:                 disabled
OBFF Enable:                   disabled
End-End TLP Prefix Blocking:   forwarding enabled
```

--- DEVICE STATUS ---

```
Correctable Error:    not detected
Non-Fatal Error:      not detected
Fatal Error:          not detected
Unsupported Request:  not detected
Aux Power:            detected
Transactions Pending: no
```

--- LINK CAPABILITIES ---

```
Maximum Link Speed:                   2.5 GT/s
Maximum Link Width:                   x1
Active State Link PM:                 L0 & L1 Entry Supported
L0 Exit Latency:                      512 ns <= t < 1  s
L1 Exit Latency:                      2  s <= t < 4  s
Clock Power Management:               not supported
Surprise Down Error Reporting:        not capable
Data Link Layer Link Active Reporting: capable
Link Bandwidth Notification:          not capable
ASPM Optionality Compliance:          no
Port Number:                          1h
Supported Link Speeds:                reserved (0h)
Crosslink:                            not supported
```

--- LINK CONTROL ---

Active State PM Control:	disabled
Read Completion Boundary Control:	64 B
Link:	enabled
Retrain Link:	no
Common Clock Configuration:	separate reference clocks
Extended Sync:	no
Clock Power Management:	disabled
Hardware Autonomous Width:	enabled
Link Bandwidth Management Interrupt:	disabled
Link Autonomous Bandwidth Interrupt:	disabled
Target Link Speed:	5.0 GT/s
Enter Compliance:	no
Hardware Autonomous Speed:	enabled
Selectable De-emphasis:	-6 dB
Transmit Margin:	000h
Enter Modified Compliance:	no
Compliance SOS:	no
Compliance Preset/De-emphasis:	0h

--- LINK STATUS ---

Speed:	2.5 GT/s
Negotiated Width:	reserved (0h)
Training Error:	no
Training:	no
Slot Clock Configuration:	platform reference clock
Data Link Layer Link:	not active
Link Bandwidth Management Status:	not asserted
Link Autonomous Bandwidth Status:	not asserted
Current De-emphasis Level:	-3.5 dB
Equalization Complete:	no
Equalization Phase 1:	not successful
Equalization Phase 2:	not successful
Equalization Phase 3:	not successful
Link Equalization Request:	no

--- SLOT CAPABILITIES ---

Attention Button:	no
Power Controller:	no
MRL Sensor Present:	no
Attention Indicator:	no
Power Indicator:	no
Hot-Plug:	surprise
Slot Power:	10000 mW
Electromechanical Interlock:	no
No Command Completed:	supported
Physical Slot Number:	0h

--- SLOT CONTROL ---

```
Attention Button Pressed:            disabled
Power Fault Detected:                disabled
MRL Sensor Changed:                  disabled
Presence Detect Changed:             disabled
Command Completed Interrupt:         disabled
Hot Plug Interrupt:                  disabled
Attention Indicator Control:         reserved (0h)
Power Indicator Control:             reserved (0h)
Power Controller Control:            power on
Electromechanical Interlock Control: not initiated
Data Link Layer State Changed:       disabled
```

--- SLOT STATUS ---

```
Attention Button Pressed:      no
Power Fault Detected:          no
MRL Sensor Changed:            no
Presence Detect Changed:       no
Command Completed:             no
MRL Sensor State:              closed
Presence Detect State:         card present
Electromechanical Interlock:   not active
Data Link Layer State Changed: no
```

--- ROOT CONTROL ---

```
SERR on Correctable Error: disabled
SERR on Non-Fatal Error:   disabled
SERR on Fatal Error:       disabled
PME Interrupt:             disabled
CRS Software Visibility:   disabled
```

--- ROOT CAPABILITIES ---

```
CRS Software Visibility: no
```

--- ROOT STATUS ---

```
PME Requester ID: 0h
PME Status:       not asserted
PME Pending:      no
```

=== CONFIGURATION SPACE ==

```
00          86 80 42 3B 07 00 10 00 05 00 04 06 10 00 81 00    B;.......... .
10          00 00 00 00 00 00 00 00 00 01 01 00 F0 00 00 20  ............ð..
20          60 D4 60 D4 F1 FF 01 00 FF FF FF FF 00 00 00 00  `Ô`Ôñÿ..ÿÿÿÿ....
30          00 00 00 00 40 00 00 00 00 00 00 00 0B 01 00 00  ....@...........
40          10 80 42 01 00 80 00 00 00 00 10 00 11 4C 11 01  . B.. .......L..
50          00 00 01 10 20 B2 04 00 00 00 00 00 00 00 00 00  .... ².........
60          00 00 00 00 16 00 00 00 00 00 00 00 00 00 00 00  ................
70          01 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
80          05 90 00 00 00 00 00 00 00 00 00 00 00 00 00 00  . ..............
90          0D A0 00 00 3C 10 2A 17 00 00 00 00 00 00 00 00  . ..<.*.........
A0          01 00 02 C8 00 00 00 00 00 00 00 00 00 00 00 00  ...È............
B0          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
C0          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
D0          00 10 00 00 02 00 00 00 00 00 11 00 00 00 00 00  ................
E0          00 00 00 00 06 07 08 00 30 00 00 00 00 00 00 00  ........0.......
F0          00 00 00 00 00 00 00 00 87 0F 07 08 00 00 00 00  ........ .......
```

=== DEVICE INFORMATION ==========

PCI Address: 0x00001c01 (Bus 0 -> Device 28 -> Function 1)
Vendor: 8086h | Intel Corporation
Status: 3B44h | 5 Series/3400 Series Chipset PCI Express Root Port 2

=== GENERAL ==========

--- DESCRIPTION ----------

Classcode: 060400h
Revision: 05h
Class: Bridge
Detail: PCI bridge
P/I: Normal decode

--- STATUS ----------

Value: 0007h
I/O Space: enabled
Memory Space: enabled
Bus Master: yes
Special Cycles: no
Memory Write Invalidate: disabled
VGA Palette Snoop: disabled
Parity Error Response: no
Stepping Control: no
SERR: disabled
Back-to-Back: disabled
Interrupt: enabled

--- COMMAND ----------

Value: 0010h
Error: none
Master abort: none
Target abort: none
Data Parity: ok
Back-to-back: normal
Features: standard
66 MHz: no
Capability List: yes
DEVSEL-Timing: fast
IRQ signaled: no

--- INFORMATION ----------

Cacheline: 16 * 32 bit
Latency: 0 + 8 Cycles
Header: 01h
Unit type: multi function
Self-test: not built-in

--- IRQ ----------

IRQ: 0Ah
IRQ pin: INTB
Latency: 0 / 0

=== BARS & ROM ==========

--- BAR 0 ----------

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 1 ----------

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 2 ----------

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 3 ----------

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 4 ----------

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 5 ----------

Type: n/a
Address:: n/a
Size:: n/a

--- ROM ----------

Type: n/a
Address:: n/a
Size:: n/a

=== CAPABILITIES ==========

--- CAPABILITY 1 ----------

ID: 10h
Name: PCI Express Capability register set
Offset: 40h

--- CAPABILITY 2 ----------

ID: 05h
Name: Message Signaled Interrupts
Offset: 80h

--- CAPABILITY 3 ----------

ID: 0Dh
Name: P2P SSID
Offset: 90h

--- CAPABILITY 4 ----------

ID: 01h
Name: PCI Power Management Interface
Offset: A0h

=== PCI EXPRESS ==========

--- CAPABILITY REGISTER ----------

Version: 02h
Device Port Type: Root Port
Slot Implemented: yes
Interrupt Message Number: 00h

--- DEVICE CAPABILITIES ----------

Max Payload Size Supported: 128 B
Phantom Functions: not available
Extended Tag Field: 5-bit Tag Field supported
Endpoint L0 Acceptable Latency: x < 64 ns
Endpoint L1 Acceptable Latency: x < 1 s
Attention Indicator: none
Power Indicator: no
Role-Based Error Reporting: not supported
Captured Slot Power: 0 W
Function Level Reset Capability: not supported
Completion Timeout Ranges Supported: Range B, C
Completion Timeout Disable: supported
ARI Forwarding: not supported
AtomicOp Routing: not supported
32-bit AtomicOp Completer: not supported
64-bit AtomicOp Completer: not supported
128-bit CAS Completer: not supported
No RO-enabled PR-PR Passing: no
LTR Mechanism: not supported
TPH Completer Supported: none
OBFF Supported: not supported
Extended Fmt Field: not supported
End-End TLP Prefix: not supported
Max End-End TLP Prefixes: 4

--- DEVICE CONTROL ---

```
Correctable Error Reporting:   disabled
Non-Fatal Error Reporting:     disabled
Fatal Error Reporting:         disabled
Unsupported Request Reporting: disabled
Relaxed Ordering:              disabled
Max Payload Size:              128 B
Extended Tag Field:            5-bit Tag Field enabled
Phantom Functions:             disabled
Aux Power PM:                  disabled
No snoop:                      disabled
Max read request size:         128 B
Initiate Function Level Reset: disabled
Initiate Function Level Reset: n/a
Completion Timeout Value:      50  s - 50 ms
Completion Timeout:            enabled
ARI Forwarding:                disabled
AtomicOp Requester:            disabled
AtomicOp Egress Blocking:      no
IDO Request:                   disabled
IDO Completion:                disabled
LTR Mechanism:                 disabled
OBFF Enable:                   disabled
End-End TLP Prefix Blocking:   forwarding enabled
```

--- DEVICE STATUS ---

```
Correctable Error:    not detected
Non-Fatal Error:      not detected
Fatal Error:          not detected
Unsupported Request:  not detected
Aux Power:            detected
Transactions Pending: no
```

--- LINK CAPABILITIES ---

```
Maximum Link Speed:                   2.5 GT/s
Maximum Link Width:                   x1
Active State Link PM:                 L0 & L1 Entry Supported
L0 Exit Latency:                      512 ns <= t < 1  s
L1 Exit Latency:                      2  s <= t < 4  s
Clock Power Management:               not supported
Surprise Down Error Reporting:        not capable
Data Link Layer Link Active Reporting: capable
Link Bandwidth Notification:          not capable
ASPM Optionality Compliance:          no
Port Number:                          2h
Supported Link Speeds:                reserved (0h)
Crosslink:                            not supported
```

--- LINK CONTROL ---

```
Active State PM Control:             disabled
Read Completion Boundary Control:    64 B
Link:                                enabled
Retrain Link:                        no
Common Clock Configuration:          separate reference clocks
Extended Sync:                       no
Clock Power Management:              disabled
Hardware Autonomous Width:           enabled
Link Bandwidth Management Interrupt: disabled
Link Autonomous Bandwidth Interrupt: disabled
Target Link Speed:                   5.0 GT/s
Enter Compliance:                    no
Hardware Autonomous Speed:           enabled
Selectable De-emphasis:              -6 dB
Transmit Margin:                     000h
Enter Modified Compliance:           no
Compliance SOS:                      no
Compliance Preset/De-emphasis:       0h
```

--- LINK STATUS ---

```
Speed:                           2.5 GT/s
Negotiated Width:                reserved (0h)
Training Error:                  no
Training:                        no
Slot Clock Configuration:        platform reference clock
Data Link Layer Link:            not active
Link Bandwidth Management Status: not asserted
Link Autonomous Bandwidth Status: not asserted
Current De-emphasis Level:       -3.5 dB
Equalization Complete:           no
Equalization Phase 1:            not successful
Equalization Phase 2:            not successful
Equalization Phase 3:            not successful
Link Equalization Request:       no
```

--- SLOT CAPABILITIES ---

```
Attention Button:            no
Power Controller:            no
MRL Sensor Present:          no
Attention Indicator:         no
Power Indicator:             no
Hot-Plug:                    surprise & capable
Slot Power:                  10000 mW
Electromechanical Interlock: no
No Command Completed:        supported
Physical Slot Number:        1h
```

--- SLOT CONTROL ---

```
Attention Button Pressed:            disabled
Power Fault Detected:                disabled
MRL Sensor Changed:                  disabled
Presence Detect Changed:             enabled
Command Completed Interrupt:         disabled
Hot Plug Interrupt:                  disabled
Attention Indicator Control:         reserved (0h)
Power Indicator Control:             reserved (0h)
Power Controller Control:            power on
Electromechanical Interlock Control: not initiated
Data Link Layer State Changed:       disabled
```

--- SLOT STATUS ---

```
Attention Button Pressed:      no
Power Fault Detected:          no
MRL Sensor Changed:            no
Presence Detect Changed:       no
Command Completed:             no
MRL Sensor State:              closed
Presence Detect State:         card present
Electromechanical Interlock:   not active
Data Link Layer State Changed: no
```

--- ROOT CONTROL ---

```
SERR on Correctable Error: disabled
SERR on Non-Fatal Error:   disabled
SERR on Fatal Error:       disabled
PME Interrupt:             disabled
CRS Software Visibility:   disabled
```

--- ROOT CAPABILITIES ---

```
CRS Software Visibility: no
```

--- ROOT STATUS ---

```
PME Requester ID: 0h
PME Status:       not asserted
PME Pending:      no
```

=== CONFIGURATION SPACE ==

```
00          86 80 44 3B 07 00 10 00 05 00 04 06 10 00 81 00    D;.......... .
10          00 00 00 00 00 00 00 00 00 02 42 00 30 40 00 20  ..........B.0@.
20          60 D0 50 D4 F1 FF 01 00 FF FF FF FF 00 00 00 00  `ÐPÔñÿ..ÿÿÿÿ....
30          00 00 00 00 40 00 00 00 00 00 00 00 0A 02 00 00  ....@...........
40          10 80 42 01 00 80 00 00 00 00 10 00 11 4C 11 02  . B.. .......L..
50          00 00 01 10 60 B2 0C 00 08 00 00 00 00 00 00 00  ....`².........
60          00 00 00 00 16 00 00 00 00 00 00 00 00 00 00 00  ................
70          01 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
80          05 90 00 00 00 00 00 00 00 00 00 00 00 00 00 00  . ..............
90          0D A0 00 00 3C 10 2A 17 00 00 00 00 00 00 00 00  . ..<.*.........
A0          01 00 02 C8 00 00 00 00 00 00 00 00 00 00 00 00  ...È............
B0          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
C0          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
D0          00 10 00 00 02 00 00 00 00 00 11 40 00 00 00 00  ...........@....
E0          00 0F 00 00 06 07 08 00 31 00 00 00 00 00 00 00  ........1.......
F0          00 00 00 00 00 00 00 00 87 0F 07 08 00 00 00 00  ........ .......
```

=== DEVICE INFORMATION ==========

PCI Address: 0x00001c03 (Bus 0 -> Device 28 -> Function 3)
Vendor: 8086h | Intel Corporation
Status: 3B48h | 5 Series/3400 Series Chipset PCI Express Root Port 4

=== GENERAL ==========

--- DESCRIPTION ----------

Classcode: 060400h
Revision: 05h
Class: Bridge
Detail: PCI bridge
P/I: Normal decode

--- STATUS ----------

Value: 0007h
I/O Space: enabled
Memory Space: enabled
Bus Master: yes
Special Cycles: no
Memory Write Invalidate: disabled
VGA Palette Snoop: disabled
Parity Error Response: no
Stepping Control: no
SERR: disabled
Back-to-Back: disabled
Interrupt: enabled

--- COMMAND ----------

Value: 0010h
Error: none
Master abort: none
Target abort: none
Data Parity: ok
Back-to-back: normal
Features: standard
66 MHz: no
Capability List: yes
DEVSEL-Timing: fast
IRQ signaled: no

--- INFORMATION ----------

Cacheline: 16 * 32 bit
Latency: 0 + 8 Cycles
Header: 01h
Unit type: multi function
Self-test: not built-in

--- IRQ ----------

IRQ: 05h
IRQ pin: INTD
Latency: 0 / 0

=== BARS & ROM ==========

--- BAR 0 ----------

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 1 ----------

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 2 ----------

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 3 ----------

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 4 ----------

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 5 ----------

Type: n/a
Address:: n/a
Size:: n/a

--- ROM ----------

Type: n/a
Address:: n/a
Size:: n/a

=== CAPABILITIES ==========

--- CAPABILITY 1 ----------

ID: 10h
Name: PCI Express Capability register set
Offset: 40h

--- CAPABILITY 2 ----------

ID: 05h
Name: Message Signaled Interrupts
Offset: 80h

--- CAPABILITY 3 ----------

ID: 0Dh
Name: P2P SSID
Offset: 90h

--- CAPABILITY 4 ----------

ID: 01h
Name: PCI Power Management Interface
Offset: A0h

=== PCI EXPRESS ==========

--- CAPABILITY REGISTER ----------

Version: 02h
Device Port Type: Root Port
Slot Implemented: yes
Interrupt Message Number: 00h

--- DEVICE CAPABILITIES ----------

Max Payload Size Supported: 128 B
Phantom Functions: not available
Extended Tag Field: 5-bit Tag Field supported
Endpoint L0 Acceptable Latency: x < 64 ns
Endpoint L1 Acceptable Latency: x < 1 s
Attention Indicator: none
Power Indicator: no
Role-Based Error Reporting: not supported
Captured Slot Power: 0 W
Function Level Reset Capability: not supported
Completion Timeout Ranges Supported: Range B, C
Completion Timeout Disable: supported
ARI Forwarding: not supported
AtomicOp Routing: not supported
32-bit AtomicOp Completer: not supported
64-bit AtomicOp Completer: not supported
128-bit CAS Completer: not supported
No RO-enabled PR-PR Passing: no
LTR Mechanism: not supported
TPH Completer Supported: none
OBFF Supported: not supported
Extended Fmt Field: not supported
End-End TLP Prefix: not supported
Max End-End TLP Prefixes: 4

--- DEVICE CONTROL ---

```
Correctable Error Reporting:   disabled
Non-Fatal Error Reporting:     disabled
Fatal Error Reporting:         disabled
Unsupported Request Reporting: disabled
Relaxed Ordering:              disabled
Max Payload Size:              128 B
Extended Tag Field:            5-bit Tag Field enabled
Phantom Functions:             disabled
Aux Power PM:                  disabled
No snoop:                      disabled
Max read request size:         128 B
Initiate Function Level Reset: disabled
Initiate Function Level Reset: n/a
Completion Timeout Value:      50  s - 50 ms
Completion Timeout:            enabled
ARI Forwarding:                disabled
AtomicOp Requester:            disabled
AtomicOp Egress Blocking:      no
IDO Request:                   disabled
IDO Completion:                disabled
LTR Mechanism:                 disabled
OBFF Enable:                   disabled
End-End TLP Prefix Blocking:   forwarding enabled
```

--- DEVICE STATUS ---

```
Correctable Error:    not detected
Non-Fatal Error:      not detected
Fatal Error:          not detected
Unsupported Request:  not detected
Aux Power:            detected
Transactions Pending: no
```

--- LINK CAPABILITIES ---

```
Maximum Link Speed:                   2.5 GT/s
Maximum Link Width:                   x1
Active State Link PM:                 L0 & L1 Entry Supported
L0 Exit Latency:                      128 ns <= t < 256 ns
L1 Exit Latency:                      2  s <= t < 4  s
Clock Power Management:               not supported
Surprise Down Error Reporting:        not capable
Data Link Layer Link Active Reporting: capable
Link Bandwidth Notification:          not capable
ASPM Optionality Compliance:          no
Port Number:                          4h
Supported Link Speeds:                reserved (0h)
Crosslink:                            not supported
```

--- LINK CONTROL ---

Active State PM Control:	L1 Entry enabled
Read Completion Boundary Control:	64 B
Link:	enabled
Retrain Link:	no
Common Clock Configuration:	common reference clock
Extended Sync:	no
Clock Power Management:	disabled
Hardware Autonomous Width:	enabled
Link Bandwidth Management Interrupt:	disabled
Link Autonomous Bandwidth Interrupt:	disabled
Target Link Speed:	5.0 GT/s
Enter Compliance:	no
Hardware Autonomous Speed:	enabled
Selectable De-emphasis:	-6 dB
Transmit Margin:	000h
Enter Modified Compliance:	no
Compliance SOS:	no
Compliance Preset/De-emphasis:	0h

--- LINK STATUS ---

Speed:	2.5 GT/s
Negotiated Width:	x1
Training Error:	no
Training:	no
Slot Clock Configuration:	platform reference clock
Data Link Layer Link:	active
Link Bandwidth Management Status:	not asserted
Link Autonomous Bandwidth Status:	not asserted
Current De-emphasis Level:	-3.5 dB
Equalization Complete:	no
Equalization Phase 1:	not successful
Equalization Phase 2:	not successful
Equalization Phase 3:	not successful
Link Equalization Request:	no

--- SLOT CAPABILITIES ---

Attention Button:	no
Power Controller:	no
MRL Sensor Present:	no
Attention Indicator:	no
Power Indicator:	no
Hot-Plug:	surprise
Slot Power:	10000 mW
Electromechanical Interlock:	no
No Command Completed:	supported
Physical Slot Number:	3h

--- SLOT CONTROL ---

```
Attention Button Pressed:            disabled
Power Fault Detected:                disabled
MRL Sensor Changed:                  disabled
Presence Detect Changed:             disabled
Command Completed Interrupt:         disabled
Hot Plug Interrupt:                  disabled
Attention Indicator Control:         reserved (0h)
Power Indicator Control:             reserved (0h)
Power Controller Control:            power on
Electromechanical Interlock Control: not initiated
Data Link Layer State Changed:       disabled
```

--- SLOT STATUS ---

```
Attention Button Pressed:      no
Power Fault Detected:          no
MRL Sensor Changed:            no
Presence Detect Changed:       yes
Command Completed:             no
MRL Sensor State:              closed
Presence Detect State:         slot empty
Electromechanical Interlock:   not active
Data Link Layer State Changed: yes
```

--- ROOT CONTROL ---

```
SERR on Correctable Error: disabled
SERR on Non-Fatal Error:   disabled
SERR on Fatal Error:       disabled
PME Interrupt:             disabled
CRS Software Visibility:   disabled
```

--- ROOT CAPABILITIES ---

```
CRS Software Visibility: no
```

--- ROOT STATUS ---

```
PME Requester ID: 0h
PME Status:       not asserted
PME Pending:      no
```

=== CONFIGURATION SPACE ==

```
00          86 80 48 3B 07 00 10 00 05 00 04 06 10 00 81 00    H;.......... .
10          00 00 00 00 00 00 00 00 00 43 43 00 F0 00 00 20  .........CC.ð..
20          50 D0 50 D0 F1 FF 01 00 FF FF FF FF 00 00 00 00  PÐPÐñÿ..ÿÿÿÿ....
30          00 00 00 00 40 00 00 00 00 00 00 00 00 05 04 00 00  ....@...........
40          10 80 42 01 00 80 00 00 00 00 10 00 11 2C 11 04  . B.. .......,..
50          42 00 11 30 20 B2 1C 00 00 00 48 01 00 00 00 00  B..0 ².....H.....
60          00 00 00 00 16 00 00 00 00 00 00 00 00 00 00 00  ................
70          01 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
80          05 90 00 00 00 00 00 00 00 00 00 00 00 00 00 00  . ..............
90          0D A0 00 00 3C 10 2A 17 00 00 00 00 00 00 00 00  . ..<.*.........
A0          01 00 02 C8 00 00 00 00 00 00 00 00 00 00 00 00  ...È............
B0          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
C0          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
D0          00 10 00 00 02 00 00 00 00 00 11 00 00 00 00 00  ................
E0          00 0F 00 00 06 07 08 00 31 00 00 00 00 00 00 00  ........1.......
F0          00 00 00 00 00 00 00 00 87 0F 07 08 00 00 00 00  ........ .......
```

=== DEVICE INFORMATION ==========

PCI Address: 0x00001e00 (Bus 0 -> Device 30 -> Function 0)
Vendor: 8086h | Intel Corporation
Status: 2448h | 82801 Mobile PCI Bridge

=== GENERAL ==========

--- DESCRIPTION ----------

Classcode: 060401h
Revision: A5h
Class: Bridge
Detail: PCI bridge
P/I: Subtractive decode

--- STATUS ----------

Value: 0107h
I/O Space: enabled
Memory Space: enabled
Bus Master: yes
Special Cycles: no
Memory Write Invalidate: disabled
VGA Palette Snoop: disabled
Parity Error Response: no
Stepping Control: no
SERR: enabled
Back-to-Back: disabled
Interrupt: enabled

--- COMMAND ----------

Value: 0010h
Error: none
Master abort: none
Target abort: none
Data Parity: ok
Back-to-back: normal
Features: standard
66 MHz: no
Capability List: yes
DEVSEL-Timing: fast
IRQ signaled: no

--- INFORMATION ----------

Cacheline: 0 * 32 bit
Latency: 0 + 8 Cycles
Header: 01h
Unit type: single function
Self-test: not built-in

--- IRQ ----------

IRQ: deactivated
IRQ pin: none
Latency: 0 / 0

=== BARS & ROM ==========

--- BAR 0 ---

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 1 ---

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 2 ---

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 3 ---

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 4 ---

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 5 ---

Type: n/a
Address:: n/a
Size:: n/a

--- ROM ---

Type: n/a
Address:: n/a
Size:: n/a

=== CAPABILITIES ==========

--- CAPABILITY 1 ---

ID: 0Dh
Name: P2P SSID
Offset: 50h

=== CONFIGURATION SPACE ==

```
00          86 80 48 24 07 01 10 00 A5 01 04 06 00 00 01 00    H$....¥.......
10          00 00 00 00 00 00 00 00 00 44 45 20 20 20 80 22  .........DE    "
20          40 D0 40 D0 F1 FF 01 00 FF FF FF FF 00 00 00 00  @Ð@Ðñÿÿÿÿ....
30          00 00 00 00 50 00 00 00 00 00 00 00 FF 00 02 00  ....P.......ÿ...
40          00 00 00 00 00 00 00 00 00 00 00 00 00 12 00 10  ................
50          0D 00 00 00 3C 10 2A 17 00 00 00 00 00 00 00 00  ....<.*.........
60          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
70          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
80          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
90          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
A0          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
B0          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
C0          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
D0          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
E0          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
F0          00 00 00 00 00 00 00 00 87 0F 07 08 00 00 00 00  ........ .......
```

=== DEVICE INFORMATION ==========

PCI Address: 0x00001f00 (Bus 0 -> Device 31 -> Function 0)
Vendor: 8086h | Intel Corporation
Status: 3B07h | QM57 Chipset LPC Interface Controller

=== GENERAL ==========

--- DESCRIPTION ----------

Classcode: 060100h
Revision: 05h
Class: Bridge
Detail: ISA bridge
P/I: n/a

--- STATUS ----------

Value: 0007h
I/O Space: enabled
Memory Space: enabled
Bus Master: yes
Special Cycles: no
Memory Write Invalidate: disabled
VGA Palette Snoop: disabled
Parity Error Response: no
Stepping Control: no
SERR: disabled
Back-to-Back: disabled
Interrupt: enabled

--- COMMAND ----------

Value: 0210h
Error: none
Master abort: none
Target abort: none
Data Parity: ok
Back-to-back: normal
Features: standard
66 MHz: no
Capability List: yes
DEVSEL-Timing: medium
IRQ signaled: no

--- INFORMATION ----------

Cacheline: 0 * 32 bit
Latency: 0 + 8 Cycles
Header: 00h
Unit type: multi function
Self-test: not built-in

--- IRQ ----------

IRQ: 00h
IRQ pin: none
Latency: 0 / 0

=== BARS & ROM ==========

--- BAR 0 ---

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 1 ---

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 2 ---

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 3 ---

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 4 ---

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 5 ---

Type: n/a
Address:: n/a
Size:: n/a

--- ROM ---

Type: n/a
Address:: n/a
Size:: n/a

=== CAPABILITIES ==========

--- CAPABILITY 1 ---

ID: 09h
Name: Vendor specific capability register set
Offset: E0h

=== CONFIGURATION SPACE ==

```
00          86 80 07 3B 07 00 10 02 05 00 01 06 00 00 80 00    .;.......... .
10          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
20          00 00 00 00 00 00 00 00 00 00 00 00 3C 10 2A 17  ............<.*.
30          00 00 00 00 E0 00 00 00 00 00 00 00 00 00 00 00  ....à...........
40          01 04 00 00 80 00 00 00 01 05 00 00 10 00 00 00  .... ...........
50          F8 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ø...............
60          0A 0B 0A 05 90 00 00 00 0A 0A 80 80 F8 00 00 00  .... .....  ø...
70          F8 00 F8 00 F8 00 F8 00 F8 00 F8 00 F8 00 F8 00  ø.ø.ø.ø.ø.ø.ø.ø.
80          10 00 0F 3F 01 02 7C 00 01 01 0C 00 01 FE FC 00  ...?..|......þü.
90          E9 02 04 00 00 0F 00 00 00 00 00 00 00 00 00 00  é...............
A0          04 02 00 00 F9 08 02 00 00 45 00 00 00 03 00 C0  ....ù....E.....À
B0          00 00 00 00 00 00 00 00 04 A0 14 00 00 00 00 00  ......... ......
C0          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
D0          33 22 11 00 67 45 00 00 00 FF 00 00 00 00 00 00  3"..gE...ÿ......
E0          09 00 10 11 91 00 E4 06 00 33 06 58 06 38 B8 02  .... .ä..3.X.8¸.
F0          01 C0 D1 FE 00 00 00 00 87 0F 07 08 00 00 00 00  .ÀÑþ.... .......
```

=== DEVICE INFORMATION ==========

PCI Address: 0x00440603 (Bus 68 -> Device 6 -> Function 3)
Vendor: 1180h | Ricoh Co Ltd
Status: 0476h | RL5c476 II

=== GENERAL ==========

--- DESCRIPTION ----------

Classcode: 060700h
Revision: BBh
Class: Bridge
Detail: CardBus bridge
P/I: n/a

--- STATUS ----------

Value: 0007h
I/O Space: enabled
Memory Space: enabled
Bus Master: yes
Special Cycles: no
Memory Write Invalidate: disabled
VGA Palette Snoop: disabled
Parity Error Response: no
Stepping Control: no
SERR: disabled
Back-to-Back: disabled
Interrupt: enabled

--- COMMAND ----------

Value: 2210h
Error: none
Master abort: received
Target abort: none
Data Parity: ok
Back-to-back: normal
Features: standard
66 MHz: no
Capability List: yes
DEVSEL-Timing: medium
IRQ signaled: no

--- INFORMATION ----------

Cacheline: 0 * 32 bit
Latency: 0 + 8 Cycles
Header: 02h
Unit type: multi function
Self-test: not built-in

--- IRQ ----------

IRQ: 0Bh
IRQ pin: INTB
Latency: 0 / 0

=== BARS & ROM ==

--- BAR 0 --

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 1 --

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 2 --

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 3 --

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 4 --

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 5 --

Type: n/a
Address:: n/a
Size:: n/a

--- ROM --

Type: n/a
Address:: n/a
Size:: n/a

=== CONFIGURATION SPACE ==

```
00          80 11 76 04 07 00 10 22 BB 00 07 06 00 00 82 00   .v...."».....  .
10          00 00 40 D0 DC 00 00 02 44 45 45 00 00 30 40 D0  ..@ÐÜ...DEE..0@Ð
20          00 30 40 D0 00 00 40 D0 00 F0 3F D0 00 21 00 00  .0@Ð..@Ð.ð?Ð.!..
30          FC 21 00 00 00 20 00 00 FC 20 00 00 0B 02 80 00  ü!... ..ü .... .
40          3C 10 2A 17 01 00 00 00 00 00 00 00 00 00 00 00  <.*.............
50          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
60          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
70          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
80          01 00 00 30 00 00 00 00 63 04 63 04 00 00 00 00  ...0....c.c.....
90          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
A0          08 00 60 80 00 00 00 00 00 00 00 00 00 00 00 00  ..` ............
B0          00 00 00 00 00 00 00 00 3C 10 2A 17 00 00 00 00  ........<.*.....
C0          00 30 00 00 00 00 00 30 00 00 00 90 00 00 00 00  .0.....0... ....
D0          00 00 00 00 40 00 00 00 00 00 00 00 01 00 0A FE  ....@..........þ
E0          00 40 C0 24 00 00 00 00 00 00 00 00 00 00 00 00  .@À$............
F0          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
```

=== DEVICE INFORMATION ==========

PCI Address: 0x00000200 (Bus 0 -> Device 2 -> Function 0)
Vendor: 8086h | Intel Corporation
Status: 0046h | Core Processor Integrated Graphics Controller

=== GENERAL ==========

--- DESCRIPTION ----------

Classcode: 030000h
Revision: 02h
Class: Display controller
Detail: VGA compatible controller
P/I: VGA controller

--- STATUS ----------

Value: 0007h
I/O Space: enabled
Memory Space: enabled
Bus Master: yes
Special Cycles: no
Memory Write Invalidate: disabled
VGA Palette Snoop: disabled
Parity Error Response: no
Stepping Control: no
SERR: disabled
Back-to-Back: disabled
Interrupt: enabled

--- COMMAND ----------

Value: 0090h
Error: none
Master abort: none
Target abort: none
Data Parity: ok
Back-to-back: fast
Features: standard
66 MHz: no
Capability List: yes
DEVSEL-Timing: fast
IRQ signaled: no

--- INFORMATION ----------

Cacheline: 0 * 32 bit
Latency: 0 + 8 Cycles
Header: 00h
Unit type: single function
Self-test: not built-in

--- IRQ ----------

IRQ: 0Ah
IRQ pin: INTA
Latency: 0 / 0

=== BARS & ROM ==========

--- BAR 0 ----------

Type: Memory (64 bit, no prefetch)
Address:: 00000000D0000000h - 00000000D03FFFFFh
Size:: 400000h

--- BAR 1 ----------

Type: Memory (64 bit, prefetch, part 2)
Address:: see BAR 0
Size:: see BAR 0

--- BAR 2 ----------

Type: Memory (64 bit, prefetch)
Address:: 00000000C0000000h - 00000000CFFFFFFFh
Size:: 10000000h

--- BAR 3 ----------

Type: Memory (64 bit, prefetch, part 2)
Address:: see BAR 2
Size:: see BAR 2

--- BAR 4 ----------

Type: I/O space
Address:: 5050h - 5057h
Size:: 8h

--- BAR 5 ----------

Type: n/a
Address:: n/a
Size:: n/a

--- ROM ----------

Type: n/a
Address:: n/a
Size:: n/a

=== CAPABILITIES ==========

--- CAPABILITY 1 ----------

ID: 05h
Name: Message Signaled Interrupts
Offset: 90h

--- CAPABILITY 2 ----------

ID: 01h
Name: PCI Power Management Interface
Offset: D0h

--- CAPABILITY 3 ----------

ID: 13h
Name: Advanced Features
Offset: A4h

=== CONFIGURATION SPACE ==========

```
00          86 80 46 00 07 00 90 00 02 00 00 03 00 00 00 00    F... .........
10          04 00 00 D0 00 00 00 00 0C 00 00 C0 00 00 00 00  ...Đ.......À....
20          51 50 00 00 00 00 00 00 00 00 00 00 3C 10 2A 17  QP..........<.*.
30          00 00 00 00 90 00 00 00 00 00 00 00 0A 01 00 00  .... ............
40          09 00 0C 01 26 61 21 00 88 00 00 00 0F 17 17 17  ....&a!. ........
50          00 00 50 0B 09 00 00 00 00 00 00 00 00 00 00 BE  ..P............¾
60          00 00 02 02 00 00 00 00 00 00 00 00 00 00 00 00  ................
70          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
80          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
90          05 D0 00 00 00 00 00 00 00 00 00 00 00 00 00 00  .Đ..............
A0          11 11 11 00 13 00 06 03 00 00 14 60 25 04 3A 30  ...........`%.:0
B0          00 00 00 00 00 00 00 00 00 02 00 00 00 00 00 00  ................
C0          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
D0          01 A4 22 00 00 00 00 00 00 00 00 00 00 01 02 00  .¤".............
E0          00 00 00 00 00 00 00 00 00 80 00 00 00 00 00 00  ......... ......
F0          00 00 00 00 00 00 00 00 AB 0F 18 00 18 D0 6F BB  ........«....Đo»
```

=== DEVICE INFORMATION ==========

PCI Address: 0x00001600 (Bus 0 -> Device 22 -> Function 0)
Vendor: 8086h | Intel Corporation
Status: 3B64h | 5 Series/3400 Series Chipset HECI Controller

=== GENERAL ==========

--- DESCRIPTION ----------

Classcode: 078000h
Revision: 06h
Class: Communication controller
Detail: Communication controller
P/I: n/a

--- STATUS ----------

Value: 0006h
I/O Space: disabled
Memory Space: enabled
Bus Master: yes
Special Cycles: no
Memory Write Invalidate: disabled
VGA Palette Snoop: disabled
Parity Error Response: no
Stepping Control: no
SERR: disabled
Back-to-Back: disabled
Interrupt: enabled

--- COMMAND ----------

Value: 0010h
Error: none
Master abort: none
Target abort: none
Data Parity: ok
Back-to-back: normal
Features: standard
66 MHz: no
Capability List: yes
DEVSEL-Timing: fast
IRQ signaled: no

--- INFORMATION ----------

Cacheline: 0 * 32 bit
Latency: 0 + 8 Cycles
Header: 00h
Unit type: multi function
Self-test: not built-in

--- IRQ ----------

IRQ: 0Ah
IRQ pin: INTA
Latency: 0 / 0

=== BARS & ROM ==========

--- BAR 0 ----------

Type: Memory (64 bit, no prefetch)
Address:: 00000000D4724000h - 00000000D472400Fh
Size:: 10h

--- BAR 1 ----------

Type: Memory (64 bit, prefetch, part 2)
Address:: see BAR 0
Size:: see BAR 0

--- BAR 2 ----------

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 3 ----------

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 4 ----------

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 5 ----------

Type: n/a
Address:: n/a
Size:: n/a

--- ROM ----------

Type: n/a
Address:: n/a
Size:: n/a

=== CAPABILITIES ==========

--- CAPABILITY 1 ----------

ID: 01h
Name: PCI Power Management Interface
Offset: 50h

--- CAPABILITY 2 ----------

ID: 05h
Name: Message Signaled Interrupts
Offset: 8Ch

=== CONFIGURATION SPACE ==

```
00          86 80 64 3B 06 00 10 00 06 00 80 07 00 00 80 00    d;...... ... .
10          04 40 72 D4 00 00 00 00 00 00 00 00 00 00 00 00  .@rÔ............
20          00 00 00 00 00 00 00 00 00 00 00 00 3C 10 2A 17  ............<.*.
30          00 00 00 00 50 00 00 00 00 00 00 00 0A 01 00 00  ....P...........
40          45 02 00 00 20 00 01 80 00 00 00 60 00 00 00 00  E... .. ...`....
50          01 8C 03 C8 08 00 00 00 00 00 00 00 00 00 00 00  . .È............
60          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
70          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
80          00 00 00 00 00 00 00 00 00 00 00 00 05 00 80 00  ............. .
90          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
A0          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
B0          00 00 00 00 00 00 00 00 00 00 00 00 02 00 00 C0  ...............À
C0          8E 05 74 90 98 49 FA 31 9F 67 85 D2 32 E2 F1 15   .t  Iú1 g Ò2âñ.
D0          91 7A 8B ED 19 14 09 18 CC 19 35 5D 2E F8 63 F6   z í....Ì.5].øcö
E0          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
F0          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
```

=== DEVICE INFORMATION ==========

PCI Address: 0x00001900 (Bus 0 -> Device 25 -> Function 0)
Vendor: 8086h | Intel Corporation
Status: 10EAh | 82577LM Gigabit Network Connection

=== GENERAL ==========

--- DESCRIPTION ----------

Classcode: 020000h
Revision: 05h
Class: Network controller
Detail: Ethernet controller
P/I: n/a

--- STATUS ----------

Value: 0007h
I/O Space: enabled
Memory Space: enabled
Bus Master: yes
Special Cycles: no
Memory Write Invalidate: disabled
VGA Palette Snoop: disabled
Parity Error Response: no
Stepping Control: no
SERR: disabled
Back-to-Back: disabled
Interrupt: enabled

--- COMMAND ----------

Value: 0010h
Error: none
Master abort: none
Target abort: none
Data Parity: ok
Back-to-back: normal
Features: standard
66 MHz: no
Capability List: yes
DEVSEL-Timing: fast
IRQ signaled: no

--- INFORMATION ----------

Cacheline: 0 * 32 bit
Latency: 0 + 8 Cycles
Header: 00h
Unit type: single function
Self-test: not built-in

--- IRQ ----------

IRQ: 0Ah
IRQ pin: INTA
Latency: 0 / 0

=== BARS & ROM ==========

--- BAR 0 ----------

Type: Memory (32 bit, no prefetch)
Address:: D4700000h - D471FFFFh
Size:: 20000h

--- BAR 1 ----------

Type: Memory (32 bit, no prefetch)
Address:: D472A000h - D472AFFFh
Size:: 1000h

--- BAR 2 ----------

Type: I/O space
Address:: 5020h - 503Fh
Size:: 20h

--- BAR 3 ----------

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 4 ----------

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 5 ----------

Type: n/a
Address:: n/a
Size:: n/a

--- ROM ----------

Type: n/a
Address:: n/a
Size:: n/a

=== CAPABILITIES ==========

--- CAPABILITY 1 ----------

ID: 01h
Name: PCI Power Management Interface
Offset: C8h

--- CAPABILITY 2 ----------

ID: 05h
Name: Message Signaled Interrupts
Offset: D0h

--- CAPABILITY 3 ----------

ID: 13h
Name: Advanced Features
Offset: E0h

=== CONFIGURATION SPACE ==========

```
00          86 80 EA 10 07 00 10 00 05 00 00 02 00 00 00 00    ê.............
10          00 00 70 D4 00 A0 72 D4 21 50 00 00 00 00 00 00  ..pÔ. rÔ!P......
20          00 00 00 00 00 00 00 00 00 00 00 00 3C 10 2A 17  ............<.*.
30          00 00 00 00 C8 00 00 00 00 00 00 00 0A 01 00 00  ....È...........
40          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
50          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
60          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
70          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
80          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
90          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
A0          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
B0          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
C0          00 00 00 00 00 00 00 00 01 D0 22 C8 00 20 00 07  .........Đ"È. ..
D0          05 E0 80 00 00 00 00 00 00 00 00 00 00 00 00 00  .à ..............
E0          13 00 06 03 00 00 00 00 00 00 00 00 00 00 00 00  ................
F0          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
```

=== DEVICE INFORMATION ==========

PCI Address: 0x00430000 (Bus 67 -> Device 0 -> Function 0)
Vendor: 14E4h | Broadcom Corporation
Status: 4315h | BCM4312 802.11b/g LP-PHY

=== GENERAL ==========

--- DESCRIPTION ----------

Classcode: 028000h
Revision: 01h
Class: Network controller
Detail: Network controller
P/I: n/a

--- STATUS ----------

Value: 0006h
I/O Space: disabled
Memory Space: enabled
Bus Master: yes
Special Cycles: no
Memory Write Invalidate: disabled
VGA Palette Snoop: disabled
Parity Error Response: no
Stepping Control: no
SERR: disabled
Back-to-Back: disabled
Interrupt: enabled

--- COMMAND ----------

Value: 0010h
Error: none
Master abort: none
Target abort: none
Data Parity: ok
Back-to-back: normal
Features: standard
66 MHz: no
Capability List: yes
DEVSEL-Timing: fast
IRQ signaled: no

--- INFORMATION ----------

Cacheline: 16 * 32 bit
Latency: 0 + 8 Cycles
Header: 00h
Unit type: single function
Self-test: not built-in

--- IRQ ----------

IRQ: 05h
IRQ pin: INTA
Latency: 0 / 0

=== BARS & ROM ==========

--- BAR 0 ---

Type: Memory (64 bit, no prefetch)
Address:: 00000000D0500000h - 00000000D0503FFFh
Size:: 4000h

--- BAR 1 ---

Type: Memory (64 bit, prefetch, part 2)
Address:: see BAR 0
Size:: see BAR 0

--- BAR 2 ---

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 3 ---

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 4 ---

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 5 ---

Type: n/a
Address:: n/a
Size:: n/a

--- ROM ---

Type: n/a
Address:: n/a
Size:: n/a

=== CAPABILITIES ==========

--- CAPABILITY 1 ---

ID: 01h
Name: PCI Power Management Interface
Offset: 40h

--- CAPABILITY 2 ---

ID: 09h
Name: Vendor specific capability register set
Offset: 58h

--- CAPABILITY 3 ----------

ID: 05h
Name: Message Signaled Interrupts
Offset: E8h

--- CAPABILITY 4 ----------

ID: 10h
Name: PCI Express Capability register set
Offset: D0h

=== PCI EXPRESS ==========

--- CAPABILITY REGISTER ----------

Version:	01h
Device Port Type:	PCI Express Endpoint
Slot Implemented:	no
Interrupt Message Number:	00h

--- DEVICE CAPABILITIES ----------

Max Payload Size Supported:	128 B
Phantom Functions:	not available
Extended Tag Field:	8-bit Tag Field supported
Endpoint L0 Acceptable Latency:	2 s <= t < 4 s
Endpoint L1 Acceptable Latency:	t >= 64 s
Attention Indicator:	none
Power Indicator:	no
Role-Based Error Reporting:	not supported
Captured Slot Power:	10000 mW
Function Level Reset Capability:	not supported
Completion Timeout Ranges Supported:	n/a
Completion Timeout Disable:	n/a
ARI Forwarding:	n/a
AtomicOp Routing:	n/a
32-bit AtomicOp Completer:	n/a
64-bit AtomicOp Completer:	n/a
128-bit CAS Completer:	n/a
No RO-enabled PR-PR Passing:	n/a
LTR Mechanism:	n/a
TPH Completer Supported:	n/a
OBFF Supported:	n/a
Extended Fmt Field:	n/a
End-End TLP Prefix:	n/a
Max End-End TLP Prefixes:	n/a

--- DEVICE CONTROL ---

```
Correctable Error Reporting:   disabled
Non-Fatal Error Reporting:     disabled
Fatal Error Reporting:         disabled
Unsupported Request Reporting: disabled
Relaxed Ordering:              disabled
Max Payload Size:              128 B
Extended Tag Field:            5-bit Tag Field enabled
Phantom Functions:             disabled
Aux Power PM:                  disabled
No snoop:                      disabled
Max read request size:         128 B
Initiate Function Level Reset: no
Initiate Function Level Reset: n/a
Completion Timeout Value:      n/a
Completion Timeout:            n/a
ARI Forwarding:                n/a
AtomicOp Requester:            n/a
AtomicOp Egress Blocking:      n/a
IDO Request:                   n/a
IDO Completion:                n/a
LTR Mechanism:                 n/a
OBFF Enable:                   n/a
End-End TLP Prefix Blocking:   n/a
```

--- DEVICE STATUS ---

```
Correctable Error:    detected
Non-Fatal Error:      not detected
Fatal Error:          not detected
Unsupported Request:  detected
Aux Power:            not detected
Transactions Pending: no
```

--- LINK CAPABILITIES ---

```
Maximum Link Speed:                   2.5 GT/s
Maximum Link Width:                   x1
Active State Link PM:                 L0 & L1 Entry Supported
L0 Exit Latency:                      2  s <= t < 4  s
L1 Exit Latency:                      32  s <= t < 64  s
Clock Power Management:               supported
Surprise Down Error Reporting:        not capable
Data Link Layer Link Active Reporting: not capable
Link Bandwidth Notification:          not capable
ASPM Optionality Compliance:          no
Port Number:                          0h
Supported Link Speeds:                n/a
Crosslink:                            n/a
```

--- LINK CONTROL ---

Active State PM Control:	L1 Entry enabled
Read Completion Boundary Control:	64 B
Link:	enabled
Retrain Link:	no
Common Clock Configuration:	common reference clock
Extended Sync:	no
Clock Power Management:	enabled
Hardware Autonomous Width:	enabled
Link Bandwidth Management Interrupt:	disabled
Link Autonomous Bandwidth Interrupt:	disabled
Target Link Speed:	n/a
Enter Compliance:	n/a
Hardware Autonomous Speed:	n/a
Selectable De-emphasis:	n/a
Transmit Margin:	n/a
Enter Modified Compliance:	n/a
Compliance SOS:	n/a
Compliance Preset/De-emphasis:	n/a

--- LINK STATUS ---

Speed:	2.5 GT/s
Negotiated Width:	x1
Training Error:	no
Training:	no
Slot Clock Configuration:	platform reference clock
Data Link Layer Link:	not active
Link Bandwidth Management Status:	not asserted
Link Autonomous Bandwidth Status:	not asserted
Current De-emphasis Level:	n/a
Equalization Complete:	n/a
Equalization Phase 1:	n/a
Equalization Phase 2:	n/a
Equalization Phase 3:	n/a
Link Equalization Request:	n/a

--- SLOT CAPABILITIES ---

Attention Button:	no
Power Controller:	no
MRL Sensor Present:	no
Attention Indicator:	no
Power Indicator:	no
Hot-Plug:	none
Slot Power:	0 W
Electromechanical Interlock:	no
No Command Completed:	not supported
Physical Slot Number:	0h

--- SLOT CONTROL ---

```
Attention Button Pressed:           enabled
Power Fault Detected:               disabled
MRL Sensor Changed:                 enabled
Presence Detect Changed:            disabled
Command Completed Interrupt:        disabled
Hot Plug Interrupt:                 disabled
Attention Indicator Control:        reserved (0h)
Power Indicator Control:            reserved (0h)
Power Controller Control:           power on
Electromechanical Interlock Control: not initiated
Data Link Layer State Changed:      enabled
```

--- SLOT STATUS ---

```
Attention Button Pressed:     no
Power Fault Detected:         no
MRL Sensor Changed:           no
Presence Detect Changed:      no
Command Completed:            no
MRL Sensor State:             closed
Presence Detect State:        card present
Electromechanical Interlock:  active
Data Link Layer State Changed: no
```

--- ROOT CONTROL ---

```
SERR on Correctable Error: disabled
SERR on Non-Fatal Error:   disabled
SERR on Fatal Error:       disabled
PME Interrupt:             disabled
CRS Software Visibility:   disabled
```

--- ROOT CAPABILITIES ---

```
CRS Software Visibility: no
```

--- ROOT STATUS ---

```
PME Requester ID: 0h
PME Status:       not asserted
PME Pending:      no
```

=== CONFIGURATION SPACE ==

```
00          E4 14 15 43 06 00 10 00 01 00 80 02 10 00 00 00  ä..C...... .....
10          04 00 50 D0 00 00 00 00 00 00 00 00 00 00 00 00  ..PÐ............
20          00 00 00 00 00 00 00 00 00 00 00 00 3C 10 08 15  ............<...
30          00 00 00 00 40 00 00 00 00 00 00 00 00 05 01 00  ....@...........
40          01 58 03 06 08 40 00 00 00 00 00 00 00 00 00 00  .X...@..........
50          00 00 00 00 00 00 00 00 09 E8 78 00 09 00 00 00  .........èx.....
60          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
70          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
80          00 10 00 18 00 00 00 00 81 00 00 00 03 00 00 00  ........ .......
90          00 00 00 00 00 01 00 00 00 00 00 00 00 00 00 00  ................
A0          00 00 00 00 00 00 00 00 00 00 01 00 00 00 00 00  ................
B0          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
C0          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
D0          10 00 01 00 A0 8F 90 05 00 00 09 00 11 6C 07 00  ....   ......l..
E0          42 01 11 10 00 00 00 00 05 D0 80 00 00 00 00 00  B........Ð .....
F0          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
```

=== DEVICE INFORMATION ==========

PCI Address: 0x00001a00 (Bus 0 -> Device 26 -> Function 0)
Vendor: 8086h | Intel Corporation
Status: 3B3Ch | 5 Series/3400 Series Chipset USB2 Enhanced Host Controller

=== GENERAL ==========

--- DESCRIPTION ----------

Classcode: 0C0320h
Revision: 05h
Class: Serial bus controller
Detail: USB controller
P/I: EHCI

--- STATUS ----------

Value: 0006h
I/O Space: disabled
Memory Space: enabled
Bus Master: yes
Special Cycles: no
Memory Write Invalidate: disabled
VGA Palette Snoop: disabled
Parity Error Response: no
Stepping Control: no
SERR: disabled
Back-to-Back: disabled
Interrupt: enabled

--- COMMAND ----------

Value: 0290h
Error: none
Master abort: none
Target abort: none
Data Parity: ok
Back-to-back: fast
Features: standard
66 MHz: no
Capability List: yes
DEVSEL-Timing: medium
IRQ signaled: no

--- INFORMATION ----------

Cacheline: 0 * 32 bit
Latency: 0 + 8 Cycles
Header: 00h
Unit type: single function
Self-test: not built-in

--- IRQ ----------

IRQ: 0Ah
IRQ pin: INTA
Latency: 0 / 0

=== BARS & ROM ==========

--- BAR 0 ---

Type: Memory (32 bit, no prefetch)
Address:: D4729000h - D47293FFh
Size:: 400h

--- BAR 1 ---

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 2 ---

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 3 ---

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 4 ---

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 5 ---

Type: n/a
Address:: n/a
Size:: n/a

--- ROM ---

Type: n/a
Address:: n/a
Size:: n/a

=== CAPABILITIES ==========

--- CAPABILITY 1 ---

ID: 01h
Name: PCI Power Management Interface
Offset: 50h

--- CAPABILITY 2 ---

ID: 0Ah
Name: Debug Port
Offset: 58h

--- CAPABILITY 3 ----------

ID: 13h
Name: Advanced Features
Offset: 98h

=== CONFIGURATION SPACE ==========

```
00          86 80 3C 3B 06 00 90 02 05 20 03 0C 00 00 00 00    <;.. .. ......
10          00 90 72 D4 00 00 00 00 00 00 00 00 00 00 00 00  . rÔ............
20          00 00 00 00 00 00 00 00 00 00 00 00 3C 10 2A 17  ............<.*.
30          00 00 00 00 50 00 00 00 00 00 00 00 0A 01 00 00  ....P...........
40          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
50          01 58 C2 C9 00 80 00 00 0A 98 A0 20 00 00 00 00  .XÂÉ. ...   ....
60          20 20 03 06 00 00 00 00 01 00 00 01 00 00 00 00    ..............
70          01 00 DF 3F 00 00 00 00 00 00 00 00 00 00 00 00  ..ß?............
80          00 00 80 00 11 89 0C 13 A0 00 00 00 00 00 00 00  .. .. .. .......
90          00 00 00 00 00 00 00 00 13 00 06 03 00 01 00 00  ................
A0          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
B0          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
C0          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
D0          00 00 00 00 00 AA FF 00 00 00 00 00 00 00 00 00  .....ªÿ.........
E0          00 00 00 00 00 00 00 00 00 00 00 00 8C AA AA 47  ............ ªªG
F0          00 00 00 00 88 85 80 00 87 0F 07 08 08 17 1B 20  ....   . ......
```

=== DEVICE INFORMATION ==========

PCI Address: 0x00001d00 (Bus 0 -> Device 29 -> Function 0)
Vendor: 8086h | Intel Corporation
Status: 3B34h | 5 Series/3400 Series Chipset USB2 Enhanced Host Controller

=== GENERAL ==========

--- DESCRIPTION ----------

Classcode: 0C0320h
Revision: 05h
Class: Serial bus controller
Detail: USB controller
P/I: EHCI

--- STATUS ----------

Value: 0006h
I/O Space: disabled
Memory Space: enabled
Bus Master: yes
Special Cycles: no
Memory Write Invalidate: disabled
VGA Palette Snoop: disabled
Parity Error Response: no
Stepping Control: no
SERR: disabled
Back-to-Back: disabled
Interrupt: enabled

--- COMMAND ----------

Value: 0290h
Error: none
Master abort: none
Target abort: none
Data Parity: ok
Back-to-back: fast
Features: standard
66 MHz: no
Capability List: yes
DEVSEL-Timing: medium
IRQ signaled: no

--- INFORMATION ----------

Cacheline: 0 * 32 bit
Latency: 0 + 8 Cycles
Header: 00h
Unit type: single function
Self-test: not built-in

--- IRQ ----------

IRQ: 0Ah
IRQ pin: INTA
Latency: 0 / 0

=== BARS & ROM ==========

--- BAR 0 ---

Type: Memory (32 bit, no prefetch)
Address:: D4728000h - D47283FFh
Size:: 400h

--- BAR 1 ---

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 2 ---

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 3 ---

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 4 ---

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 5 ---

Type: n/a
Address:: n/a
Size:: n/a

--- ROM ---

Type: n/a
Address:: n/a
Size:: n/a

=== CAPABILITIES ==========

--- CAPABILITY 1 ---

ID: 01h
Name: PCI Power Management Interface
Offset: 50h

--- CAPABILITY 2 ---

ID: 0Ah
Name: Debug Port
Offset: 58h

--- CAPABILITY 3 ----------

ID: 13h
Name: Advanced Features
Offset: 98h

=== CONFIGURATION SPACE ==========

```
00          86 80 34 3B 06 00 90 02 05 20 03 0C 00 00 00 00    4;.. .. ......
10          00 80 72 D4 00 00 00 00 00 00 00 00 00 00 00 00  . rÔ............
20          00 00 00 00 00 00 00 00 00 00 00 00 3C 10 2A 17  ............<.*.
30          00 00 00 00 50 00 00 00 00 00 00 00 0A 01 00 00  ....P...........
40          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
50          01 58 C2 C9 00 80 00 00 0A 98 A0 20 00 00 00 00  .XÂÉ. ...   ....
60          20 20 03 06 00 00 00 00 01 00 00 00 00 00 08 80    ............
70          01 00 DF 3F 00 00 00 00 00 00 00 00 00 00 00 00  ..ß?............
80          00 00 80 00 11 89 0C 13 A0 00 00 00 00 00 00 00  .. .. .. .......
90          00 00 00 00 00 00 00 00 13 00 06 03 00 01 00 00  ................
A0          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
B0          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
C0          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
D0          00 00 00 00 00 AA FF 00 00 00 00 00 00 00 00 00  .....ªÿ.........
E0          00 00 00 00 00 00 00 00 00 00 00 00 28 70 08 22  ............(p."
F0          00 00 00 00 88 85 80 00 87 0F 07 08 08 17 1B 20  ....   . ......
```

=== DEVICE INFORMATION ==========

PCI Address: 0x00440600 (Bus 68 -> Device 6 -> Function 0)
Vendor: 1180h | Ricoh Co Ltd
Status: 0832h | R5C832 IEEE 1394 Controller

=== GENERAL ==========

--- DESCRIPTION ----------

Classcode: 0C0010h
Revision: 06h
Class: Serial bus controller
Detail: FireWire (IEEE 1394)
P/I: OHCI

--- STATUS ----------

Value: 0006h
I/O Space: disabled
Memory Space: enabled
Bus Master: yes
Special Cycles: no
Memory Write Invalidate: disabled
VGA Palette Snoop: disabled
Parity Error Response: no
Stepping Control: no
SERR: disabled
Back-to-Back: disabled
Interrupt: enabled

--- COMMAND ----------

Value: 2210h
Error: none
Master abort: received
Target abort: none
Data Parity: ok
Back-to-back: normal
Features: standard
66 MHz: no
Capability List: yes
DEVSEL-Timing: medium
IRQ signaled: no

--- INFORMATION ----------

Cacheline: 16 * 32 bit
Latency: 0 + 8 Cycles
Header: 00h
Unit type: multi function
Self-test: not built-in

--- IRQ ----------

IRQ: 0Ah
IRQ pin: INTA
Latency: 2 / 4

=== BARS & ROM ==========

--- BAR 0 ---

Type: Memory (32 bit, no prefetch)
Address:: D0401000h - D04017FFh
Size:: 800h

--- BAR 1 ---

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 2 ---

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 3 ---

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 4 ---

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 5 ---

Type: n/a
Address:: n/a
Size:: n/a

--- ROM ---

Type: n/a
Address:: n/a
Size:: n/a

=== CAPABILITIES ==========

--- CAPABILITY 1 ---

ID: 01h
Name: PCI Power Management Interface
Offset: DCh

=== CONFIGURATION SPACE ==

```
00          80 11 32 08 06 00 10 22 06 10 00 0C 10 00 80 00   .2...."...... .
10          00 10 40 D0 00 00 00 00 00 00 00 00 00 00 00 00  ..@Ð............
20          00 00 00 00 00 00 00 00 00 00 00 00 3C 10 2A 17  ............<.*.
30          00 00 00 00 DC 00 00 00 00 00 00 00 0A 01 02 04  ....Ü...........
40          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
50          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
60          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
70          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
80          00 00 80 16 00 00 00 00 00 20 00 00 66 66 32 12  .. ...... ..ff2.
90          48 60 66 10 00 00 02 00 03 00 00 00 00 01 18 00  H`f.............
A0          00 00 00 00 00 00 00 00 30 00 00 00 3C 10 2A 17  ........0...<.*.
B0          00 00 00 00 00 00 00 00 00 00 00 00 00 00 02 04  ................
C0          00 30 00 00 00 00 00 30 00 00 00 90 00 00 00 00  .0.....0... ....
D0          00 00 00 00 40 00 00 00 00 00 00 00 00 01 00 02 FE  ....@..........þ
E0          00 C0 00 48 00 00 00 00 00 00 00 00 00 00 00 00  .À.H............
F0          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
```

=== DEVICE INFORMATION ==========

PCI Address: 0x00001b00 (Bus 0 -> Device 27 -> Function 0)
Vendor: 8086h | Intel Corporation
Status: 3B56h | 5 Series/3400 Series Chipset High Definition Audio

=== GENERAL ==========

--- DESCRIPTION ----------

Classcode: 040300h
Revision: 05h
Class: Multimedia controller
Detail: Audio device
P/I: n/a

--- STATUS ----------

Value: 0006h
I/O Space: disabled
Memory Space: enabled
Bus Master: yes
Special Cycles: no
Memory Write Invalidate: disabled
VGA Palette Snoop: disabled
Parity Error Response: no
Stepping Control: no
SERR: disabled
Back-to-Back: disabled
Interrupt: enabled

--- COMMAND ----------

Value: 0010h
Error: none
Master abort: none
Target abort: none
Data Parity: ok
Back-to-back: normal
Features: standard
66 MHz: no
Capability List: yes
DEVSEL-Timing: fast
IRQ signaled: no

--- INFORMATION ----------

Cacheline: 16 * 32 bit
Latency: 0 + 8 Cycles
Header: 00h
Unit type: single function
Self-test: not built-in

--- IRQ ----------

IRQ: 0Ah
IRQ pin: INTA
Latency: 0 / 0

=== BARS & ROM ==========

--- BAR 0 ---

Type: Memory (64 bit, no prefetch)
Address:: 00000000D4720000h - 00000000D4723FFFh
Size:: 4000h

--- BAR 1 ---

Type: Memory (64 bit, prefetch, part 2)
Address:: see BAR 0
Size:: see BAR 0

--- BAR 2 ---

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 3 ---

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 4 ---

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 5 ---

Type: n/a
Address:: n/a
Size:: n/a

--- ROM ---

Type: n/a
Address:: n/a
Size:: n/a

=== CAPABILITIES ==========

--- CAPABILITY 1 ---

ID: 01h
Name: PCI Power Management Interface
Offset: 50h

--- CAPABILITY 2 ---

ID: 05h
Name: Message Signaled Interrupts
Offset: 60h

--- CAPABILITY 3 ----------

ID: 10h
Name: PCI Express Capability register set
Offset: 70h

=== PCI EXPRESS ==========

--- CAPABILITY REGISTER ----------

Version:	01h
Device Port Type:	Root Complex Integrated Endpoint
Slot Implemented:	no
Interrupt Message Number:	00h

--- DEVICE CAPABILITIES ----------

Max Payload Size Supported:	128 B
Phantom Functions:	not available
Extended Tag Field:	5-bit Tag Field supported
Endpoint L0 Acceptable Latency:	x < 64 ns
Endpoint L1 Acceptable Latency:	x < 1 s
Attention Indicator:	none
Power Indicator:	no
Role-Based Error Reporting:	not supported
Captured Slot Power:	0 W
Function Level Reset Capability:	supported
Completion Timeout Ranges Supported:	n/a
Completion Timeout Disable:	n/a
ARI Forwarding:	n/a
AtomicOp Routing:	n/a
32-bit AtomicOp Completer:	n/a
64-bit AtomicOp Completer:	n/a
128-bit CAS Completer:	n/a
No RO-enabled PR-PR Passing:	n/a
LTR Mechanism:	n/a
TPH Completer Supported:	n/a
OBFF Supported:	n/a
Extended Fmt Field:	n/a
End-End TLP Prefix:	n/a
Max End-End TLP Prefixes:	n/a

--- DEVICE CONTROL ---

```
Correctable Error Reporting:   disabled
Non-Fatal Error Reporting:     disabled
Fatal Error Reporting:         disabled
Unsupported Request Reporting: disabled
Relaxed Ordering:              disabled
Max Payload Size:              128 B
Extended Tag Field:            5-bit Tag Field enabled
Phantom Functions:             disabled
Aux Power PM:                  disabled
No snoop:                      enabled
Max read request size:         128 B
Initiate Function Level Reset: no
Initiate Function Level Reset: n/a
Completion Timeout Value:      n/a
Completion Timeout:            n/a
ARI Forwarding:                n/a
AtomicOp Requester:            n/a
AtomicOp Egress Blocking:      n/a
IDO Request:                   n/a
IDO Completion:                n/a
LTR Mechanism:                 n/a
OBFF Enable:                   n/a
End-End TLP Prefix Blocking:   n/a
```

--- DEVICE STATUS ---

```
Correctable Error:    not detected
Non-Fatal Error:      not detected
Fatal Error:          not detected
Unsupported Request:  not detected
Aux Power:            detected
Transactions Pending: no
```

--- LINK CAPABILITIES ---

```
Maximum Link Speed:                   reserved (0h)
Maximum Link Width:                   reserved (0h)
Active State Link PM:                 reserved (0h)
L0 Exit Latency:                      x < 64 ns
L1 Exit Latency:                      x < 1  s
Clock Power Management:               not supported
Surprise Down Error Reporting:        not capable
Data Link Layer Link Active Reporting: not capable
Link Bandwidth Notification:          not capable
ASPM Optionality Compliance:          no
Port Number:                          0h
Supported Link Speeds:                n/a
Crosslink:                            n/a
```

--- LINK CONTROL ---

Active State PM Control:	disabled
Read Completion Boundary Control:	64 B
Link:	enabled
Retrain Link:	no
Common Clock Configuration:	separate reference clocks
Extended Sync:	no
Clock Power Management:	disabled
Hardware Autonomous Width:	enabled
Link Bandwidth Management Interrupt:	disabled
Link Autonomous Bandwidth Interrupt:	disabled
Target Link Speed:	n/a
Enter Compliance:	n/a
Hardware Autonomous Speed:	n/a
Selectable De-emphasis:	n/a
Transmit Margin:	n/a
Enter Modified Compliance:	n/a
Compliance SOS:	n/a
Compliance Preset/De-emphasis:	n/a

--- LINK STATUS ---

Speed:	reserved (0h)
Negotiated Width:	reserved (0h)
Training Error:	no
Training:	no
Slot Clock Configuration:	independant clock
Data Link Layer Link:	not active
Link Bandwidth Management Status:	not asserted
Link Autonomous Bandwidth Status:	not asserted
Current De-emphasis Level:	n/a
Equalization Complete:	n/a
Equalization Phase 1:	n/a
Equalization Phase 2:	n/a
Equalization Phase 3:	n/a
Link Equalization Request:	n/a

--- SLOT CAPABILITIES ---

Attention Button:	no
Power Controller:	no
MRL Sensor Present:	no
Attention Indicator:	no
Power Indicator:	no
Hot-Plug:	none
Slot Power:	0 W
Electromechanical Interlock:	no
No Command Completed:	not supported
Physical Slot Number:	0h

--- SLOT CONTROL ---

```
Attention Button Pressed:           disabled
Power Fault Detected:               disabled
MRL Sensor Changed:                 disabled
Presence Detect Changed:            disabled
Command Completed Interrupt:        disabled
Hot Plug Interrupt:                 disabled
Attention Indicator Control:        reserved (0h)
Power Indicator Control:            reserved (0h)
Power Controller Control:           power on
Electromechanical Interlock Control: not initiated
Data Link Layer State Changed:      disabled
```

--- SLOT STATUS ---

```
Attention Button Pressed:     no
Power Fault Detected:         no
MRL Sensor Changed:           no
Presence Detect Changed:      no
Command Completed:            no
MRL Sensor State:             closed
Presence Detect State:        card present
Electromechanical Interlock:  not active
Data Link Layer State Changed: no
```

--- ROOT CONTROL ---

```
SERR on Correctable Error: disabled
SERR on Non-Fatal Error:   disabled
SERR on Fatal Error:       disabled
PME Interrupt:             disabled
CRS Software Visibility:   disabled
```

--- ROOT CAPABILITIES ---

```
CRS Software Visibility: no
```

--- ROOT STATUS ---

```
PME Requester ID: 0h
PME Status:       not asserted
PME Pending:      no
```

=== CONFIGURATION SPACE ==

```
00          86 80 56 3B 06 00 10 00 05 00 03 04 10 00 00 00    V;............
10          04 00 72 D4 00 00 00 00 00 00 00 00 00 00 00 00  ..rÔ............
20          00 00 00 00 00 00 00 00 00 00 00 00 3C 10 2A 17  ............<.*.
30          00 00 00 00 50 00 00 00 00 00 00 00 0A 01 00 00  ....P...........
40          01 00 00 47 01 00 00 00 00 00 00 00 00 00 00 00  ...G............
50          01 60 42 C8 00 00 00 00 00 00 00 00 00 00 00 00  .`BÈ............
60          05 70 80 00 00 00 00 00 00 00 00 00 00 00 00 00  .p .............
70          10 00 91 00 00 00 00 10 00 08 10 00 00 00 00 00  .. .............
80          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
90          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
A0          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
B0          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
C0          00 04 00 01 02 00 00 00 05 00 09 02 10 70 30 16  .............p0.
D0          0B 00 91 06 10 00 31 16 00 00 00 00 00 00 00 00  .. ...1.........
E0          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
F0          00 00 00 00 00 00 00 00 87 0F 07 08 00 00 00 00  ........ .......
```

=== DEVICE INFORMATION ==========

PCI Address: 0x00001f02 (Bus 0 -> Device 31 -> Function 2)
Vendor: 8086h | Intel Corporation
Status: 3B2Fh | 5 Series/3400 Series Chipset 6 port SATA AHCI Controller

=== GENERAL ==========

--- DESCRIPTION ----------

Classcode: 010601h
Revision: 05h
Class: Mass storage controller
Detail: SATA controller
P/I: AHCI 1.0

--- STATUS ----------

Value: 0007h
I/O Space: enabled
Memory Space: enabled
Bus Master: yes
Special Cycles: no
Memory Write Invalidate: disabled
VGA Palette Snoop: disabled
Parity Error Response: no
Stepping Control: no
SERR: disabled
Back-to-Back: disabled
Interrupt: enabled

--- COMMAND ----------

Value: 02B0h
Error: none
Master abort: none
Target abort: none
Data Parity: ok
Back-to-back: fast
Features: standard
66 MHz: yes
Capability List: yes
DEVSEL-Timing: medium
IRQ signaled: no

--- INFORMATION ----------

Cacheline: 0 * 32 bit
Latency: 0 + 8 Cycles
Header: 00h
Unit type: single function
Self-test: not built-in

--- IRQ ----------

IRQ: 0Ah
IRQ pin: INTA
Latency: 0 / 0

=== BARS & ROM ==========

--- BAR 0 ---

Type: I/O space
Address:: 5048h - 504Fh
Size:: 8h

--- BAR 1 ---

Type: I/O space
Address:: 505Ch - 505Fh
Size:: 4h

--- BAR 2 ---

Type: I/O space
Address:: 5040h - 5047h
Size:: 8h

--- BAR 3 ---

Type: I/O space
Address:: 5058h - 505Bh
Size:: 4h

--- BAR 4 ---

Type: I/O space
Address:: 5000h - 501Fh
Size:: 20h

--- BAR 5 ---

Type: Memory (32 bit, no prefetch)
Address:: D4727000h - D47277FFh
Size:: 800h

--- ROM ---

Type: n/a
Address:: n/a
Size:: n/a

=== CAPABILITIES ==========

--- CAPABILITY 1 ---

ID: 05h
Name: Message Signaled Interrupts
Offset: 80h

--- CAPABILITY 2 ---

ID: 01h
Name: PCI Power Management Interface
Offset: 70h

--- CAPABILITY 3 ----------

ID: 12h
Name: S-ATA
Offset: A8h

--- CAPABILITY 4 ----------

ID: 13h
Name: Advanced Features
Offset: B0h

=== CONFIGURATION SPACE ==========

```
00          86 80 2F 3B 07 00 B0 02 05 01 06 01 00 00 00 00    /;..°.........
10          49 50 00 00 5D 50 00 00 41 50 00 00 59 50 00 00  IP..]P..AP..YP..
20          01 50 00 00 00 70 72 D4 00 00 00 00 3C 10 2A 17  .P...prÔ....<.*.
30          00 00 00 00 80 00 00 00 00 00 00 00 0A 01 00 00  .... ............
40          00 80 00 80 00 00 00 00 00 00 00 00 00 00 00 00  . . ............
50          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
60          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
70          01 A8 03 40 08 00 00 00 00 00 00 00 00 00 00 00  .¨.@............
80          05 70 00 00 00 00 00 00 00 00 00 00 00 00 00 00  .p..............
90          60 08 37 83 83 01 00 08 00 02 59 00 00 00 00 00  `.7  .....Y.....
A0          D4 00 00 00 00 00 00 10 12 B0 10 00 48 00 00 00  Ô........°..H...
B0          13 00 06 03 00 00 00 00 00 00 00 00 00 00 00 00  ................
C0          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
D0          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
E0          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
F0          00 00 00 00 00 00 00 00 87 0F 07 08 00 00 00 00  ........ .......
```

=== DEVICE INFORMATION ==========

PCI Address: 0x00001f06 (Bus 0 -> Device 31 -> Function 6)
Vendor: 8086h | Intel Corporation
Status: 3B32h | 5 Series/3400 Series Chipset Thermal Subsystem

=== GENERAL ==========

--- DESCRIPTION ----------

Classcode: 118000h
Revision: 05h
Class: Signal processing controller
Detail: Signal processing controller
P/I: n/a

--- STATUS ----------

Value: 0006h
I/O Space: disabled
Memory Space: enabled
Bus Master: yes
Special Cycles: no
Memory Write Invalidate: disabled
VGA Palette Snoop: disabled
Parity Error Response: no
Stepping Control: no
SERR: disabled
Back-to-Back: disabled
Interrupt: enabled

--- COMMAND ----------

Value: 0010h
Error: none
Master abort: none
Target abort: none
Data Parity: ok
Back-to-back: normal
Features: standard
66 MHz: no
Capability List: yes
DEVSEL-Timing: fast
IRQ signaled: no

--- INFORMATION ----------

Cacheline: 0 * 32 bit
Latency: 0 + 8 Cycles
Header: 00h
Unit type: single function
Self-test: not built-in

--- IRQ ----------

IRQ: 0Ah
IRQ pin: INTC
Latency: 0 / 0

=== BARS & ROM ==========

--- BAR 0 ---

Type: Memory (64 bit, no prefetch)
Address:: 00000000D4726000h - 00000000D4726FFFh
Size:: 1000h

--- BAR 1 ---

Type: Memory (64 bit, prefetch, part 2)
Address:: see BAR 0
Size:: see BAR 0

--- BAR 2 ---

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 3 ---

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 4 ---

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 5 ---

Type: n/a
Address:: n/a
Size:: n/a

--- ROM ---

Type: n/a
Address:: n/a
Size:: n/a

=== CAPABILITIES ==========

--- CAPABILITY 1 ---

ID: 01h
Name: PCI Power Management Interface
Offset: 50h

--- CAPABILITY 2 ---

ID: 05h
Name: Message Signaled Interrupts
Offset: 80h

=== CONFIGURATION SPACE ==

```
00          86 80 32 3B 06 00 10 00 05 00 80 11 00 00 00 00    2;...... .....
10          04 60 72 D4 00 00 00 00 00 00 00 00 00 00 00 00  .`rÔ............
20          00 00 00 00 00 00 00 00 00 00 00 00 3C 10 2A 17  ............<.*.
30          00 00 00 00 50 00 00 00 00 00 00 00 0A 03 00 00  ....P...........
40          05 00 80 D4 00 00 00 00 00 00 00 00 00 00 00 00  .. Ô............
50          01 80 23 00 08 00 00 00 00 00 00 00 00 00 00 00  . #.............
60          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
70          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
80          05 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
90          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
A0          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
B0          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
C0          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
D0          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
E0          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
F0          00 00 00 00 00 00 00 00 87 0F 07 08 00 00 00 00  ........ .......
```

=== DEVICE INFORMATION ==========

PCI Address: 0x00440601 (Bus 68 -> Device 6 -> Function 1)
Vendor: 1180h | Ricoh Co Ltd
Status: 0822h | R5C822 SD/SDIO/MMC/MS/MSPro Host Adapter

=== GENERAL ==========

--- DESCRIPTION ----------

Classcode: 080500h
Revision: 25h
Class: Generic system peripheral
Detail: SD Host controller
P/I: n/a

--- STATUS ----------

Value: 0006h
I/O Space: disabled
Memory Space: enabled
Bus Master: yes
Special Cycles: no
Memory Write Invalidate: disabled
VGA Palette Snoop: disabled
Parity Error Response: no
Stepping Control: no
SERR: disabled
Back-to-Back: disabled
Interrupt: enabled

--- COMMAND ----------

Value: 2210h
Error: none
Master abort: received
Target abort: none
Data Parity: ok
Back-to-back: normal
Features: standard
66 MHz: no
Capability List: yes
DEVSEL-Timing: medium
IRQ signaled: no

--- INFORMATION ----------

Cacheline: 16 * 32 bit
Latency: 0 + 8 Cycles
Header: 00h
Unit type: multi function
Self-test: not built-in

--- IRQ ----------

IRQ: 0Bh
IRQ pin: INTB
Latency: 0 / 0

=== BARS & ROM ==========

--- BAR 0 ---

Type: Memory (32 bit, no prefetch)
Address:: D0403000h - D04030FFh
Size:: 100h

--- BAR 1 ---

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 2 ---

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 3 ---

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 4 ---

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 5 ---

Type: n/a
Address:: n/a
Size:: n/a

--- ROM ---

Type: n/a
Address:: n/a
Size:: n/a

=== CAPABILITIES ==========

--- CAPABILITY 1 ---

ID: 01h
Name: PCI Power Management Interface
Offset: 80h

=== CONFIGURATION SPACE ==

```
00          80 11 22 08 06 00 10 22 25 00 05 08 10 00 80 00   ."....."%..... .
10          00 30 40 D0 00 00 00 00 00 00 00 00 00 00 00 00  .0@Ð............
20          00 00 00 00 00 00 00 00 00 00 00 00 3C 10 2A 17  ............<.*.
30          00 00 00 00 80 00 00 00 00 00 00 00 0B 02 00 00  .... ............
40          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
50          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
60          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
70          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
80          01 00 02 FE 00 40 00 48 00 00 00 00 00 00 00 00  ...þ.@.H........
90          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
A0          00 00 00 00 00 00 00 00 00 00 00 00 3C 10 2A 17  ............<.*.
B0          04 00 02 00 00 00 00 00 00 00 00 00 A0 00 00 00  ............ ...
C0          00 30 00 00 00 00 00 30 00 00 00 90 00 00 00 00  .0.....0... ....
D0          00 00 00 00 40 00 00 00 00 00 00 00 00 00 00 00  ....@...........
E0          A1 21 80 01 00 00 00 00 40 00 00 00 00 00 00 00  ¡! .....@.......
F0          00 00 00 00 00 00 00 00 C1 00 20 00 00 00 00 00  ........Á. .....
```

=== DEVICE INFORMATION ==========

PCI Address: 0x00440602 (Bus 68 -> Device 6 -> Function 2)
Vendor: 1180h | Ricoh Co Ltd
Status: 0843h | R5C843 MMC Host Controller

=== GENERAL ==========

--- DESCRIPTION ----------

Classcode: 088000h
Revision: 14h
Class: Generic system peripheral
Detail: System peripheral
P/I: n/a

--- STATUS ----------

Value: 0006h
I/O Space: disabled
Memory Space: enabled
Bus Master: yes
Special Cycles: no
Memory Write Invalidate: disabled
VGA Palette Snoop: disabled
Parity Error Response: no
Stepping Control: no
SERR: disabled
Back-to-Back: disabled
Interrupt: enabled

--- COMMAND ----------

Value: 2210h
Error: none
Master abort: received
Target abort: none
Data Parity: ok
Back-to-back: normal
Features: standard
66 MHz: no
Capability List: yes
DEVSEL-Timing: medium
IRQ signaled: no

--- INFORMATION ----------

Cacheline: 16 * 32 bit
Latency: 0 + 8 Cycles
Header: 00h
Unit type: multi function
Self-test: not built-in

--- IRQ ----------

IRQ: 0Bh
IRQ pin: INTB
Latency: 0 / 0

=== BARS & ROM ==========

--- BAR 0 ---

Type: Memory (32 bit, no prefetch)
Address:: D0402000h - D04020FFh
Size:: 100h

--- BAR 1 ---

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 2 ---

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 3 ---

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 4 ---

Type: n/a
Address:: n/a
Size:: n/a

--- BAR 5 ---

Type: n/a
Address:: n/a
Size:: n/a

--- ROM ---

Type: n/a
Address:: n/a
Size:: n/a

=== CAPABILITIES ==========

--- CAPABILITY 1 ---

ID: 01h
Name: PCI Power Management Interface
Offset: 80h

=== CONFIGURATION SPACE ==

```
00          80 11 43 08 06 00 10 22 14 00 80 08 10 00 80 00   .C....".. ... .
10          00 20 40 D0 00 00 00 00 00 00 00 00 00 00 00 00  . @Ð............
20          00 00 00 00 00 00 00 00 00 00 00 00 3C 10 2A 17  ............<.*.
30          00 00 00 00 80 00 00 00 00 00 00 00 0B 02 00 00  .... ............
40          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
50          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
60          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
70          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
80          01 00 02 FE 00 40 00 48 00 00 00 00 00 00 00 00  ...þ.@.H........
90          00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
A0          00 00 00 00 00 00 00 00 00 00 00 00 3C 10 2A 17  ............<.*.
B0          00 00 02 00 00 00 00 00 00 00 00 00 A0 00 00 00  ............ ...
C0          00 30 00 00 00 00 00 30 00 00 00 90 00 00 00 00  .0.....0... ....
D0          00 00 00 00 40 00 00 00 00 00 00 00 00 00 00 00  ....@...........
E0          80 02 04 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
F0          00 00 00 00 00 00 00 00 C0 00 20 00 00 00 00 00  ........À. .....
```