OpenCore Sammelthread (Hilfe und Diskussion)

Beitrag von „JimSalabim“ vom 19. März 2020, 02:44

Kann mir jemand sagen, ob folgende Patches überhaupt notwendig sind?

Hardware etc. siehe Profilangaben/Signatur.

- SSDT-HPET.aml (mit SSDTTime erstellt) mitsamt _CRS to XCRS Rename
- RTC IRQ 8 Patch
- TIMR IRQ 0 Patch

Falls ja: Ist es sinnvoll, die SSDT-HPET nur auf Darwin festzulegen?

Original:

Code

```
/*
* Intel ACPI Component Architecture
* AML/ASL+ Disassembler version 20180427 (64-bit version)(RM)
* Copyright (c) 2000 - 2018 Intel Corporation
*
* Disassembling to non-symbolic legacy ASL operators
*
* Disassembly of iASLLHQJil.aml, Thu Mar 19 02:43:01 2020
*
* Original Table Header:
* Signature "SSDT"
```

```
12. * Length 0x00000066 (102)
13. * Revision 0x02
14. * Checksum 0x44
15. * OEM ID "hack"
16. * OEM Table ID "HPET"
17. * OEM Revision 0x00000000 (0)
18. * Compiler ID "INTL"
19. * Compiler Version 0x20180427 (538444839)
20. */
21. DefinitionBlock ("", "SSDT", 2, "hack", "HPET", 0x00000000)
22. {
23. External (_SB_.PCI0.LPCB, DeviceObj) // (from opcode)
24.
25. Name (\_SB.PCI0.LPCB.HPET._CRS, ResourceTemplate () // _CRS: Current Resource Settings
26. {
27. IRQNoFlags ()
28. {0,8,11}
29. Memory32Fixed (ReadWrite,
30. 0xFED00000, // Address Base
31. 0x00000400, // Address Length
32. )
33. })
34. }
```

Alles anzeigen

geändert:

Code

```
1. /*
2. * Intel ACPI Component Architecture
3. * AML/ASL+ Disassembler version 20180427 (64-bit version)(RM)
4. * Copyright (c) 2000 - 2018 Intel Corporation
5. *
6. * Disassembling to non-symbolic legacy ASL operators
7. *
8. * Disassembly of iASLhcUrAi.aml, Thu Mar 19 02:43:32 2020
9. *
10. * Original Table Header:
11. * Signature "SSDT"
12. * Length 0x0000007C (124)
13. * Revision 0x02
14. * Checksum 0x9A
```

```
15. * OEM ID "hack"
16. * OEM Table ID "HPET"
17. * OEM Revision 0x00000000 (0)
18. * Compiler ID "INTL"
19. * Compiler Version 0x20180427 (538444839)
20. */
21. DefinitionBlock ("", "SSDT", 2, "hack", "HPET", 0x00000000)
22. {
23. External (_SB_.PCI0.LPCB, DeviceObj) // (from opcode)
24.
25. If (_OSI ("Darwin"))
26. {
27. Name (\_SB.PCI0.LPCB.HPET._CRS, ResourceTemplate () // _CRS: Current Resource Settings
28. {
29. IRQNoFlags ()
30. {0,8,11}
31. Memory32Fixed (ReadWrite,
32. 0xFED00000, // Address Base
33. 0x00000400, // Address Length
34. )
35. })
36. }
37. Else
38. {
39. Return (_OSI (Arg0))
40. }
41. }
```

Alles anzeigen